Features

- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

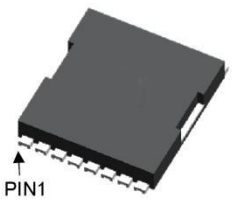
Application

- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications

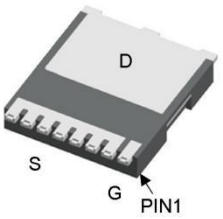
Product Summary

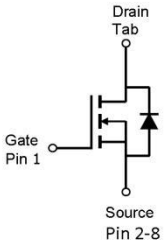
	TOLL
V_{DS}	60V
$R_{DS(on)@VGS=10V}$	0.65mΩ
I_D	454A

TOLL Top View



TOLL Bottom View





Package Marking and Ordering Information

Type	Package	Marking	Reel Size	Tape Width	Packing	Qty
LR008N06SM10	TOLL	LR008N06SM10	330*28.5mm	24mm	Reel&Tape	2000

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	60	V
Continuous drain current T_C = 25°C (Package limit) T_C = 100°C (Silicon limit)	I_D	 454 287	A
Pulsed drain current, T_C = 25°C	$I_{D\ pulse}$	1861	
Avalanche energy, single pulse (L=0.5mH,Rg=25Ω)	E_{AS}	2916	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation T_C = 25°C	P_D	278	W
Operating junction and storage temperature	T_j , T_{stg}	-55~150	℃

Thermal Resistance

	Symbol	Value	Unit
Thermal resistance, junction – case. Max	R_{thJC}	0.45	℃/W
Thermal resistance, junction – ambient. Max	R_{thJA}	62	

Electrical Characteristic, at Tj = 25 °C, unless otherwise specified

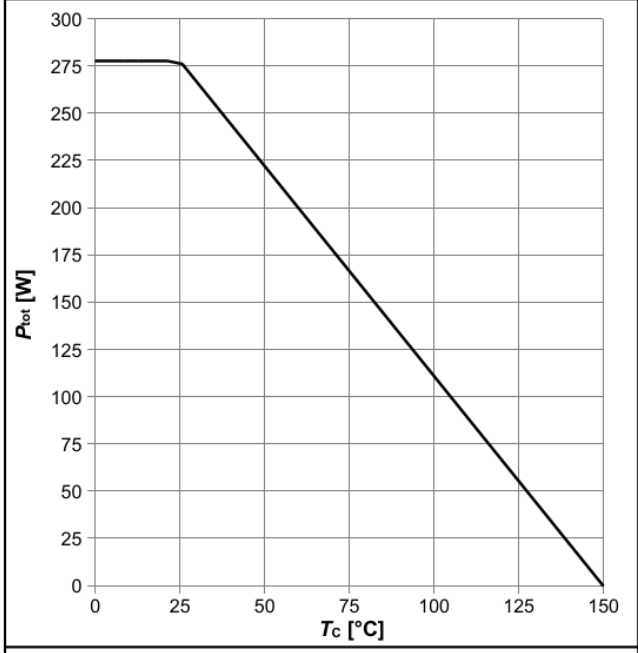
Parameter	Symbol	Test Condition	Value			Unit
			min.	typ.	max.	
Static Characteristic						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA T_j=25°C	2	3	4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60V,V_{GS}=0V T_j=25°C	-	-	1	μA
Gate-source leakage current	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=40A, T_j=25°C	-	0.65	0.8	mΩ
Transconductance	g_{fs}	V_{DS}=5V,I_D=50A	-	88	-	S
Dynamic Characteristic						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=30V, f=1MHz	-	13929	-	pF
Output Capacitance	C_{oss}		-	2995	-	
Reverse Transfer Capacitance	C_{rss}		-	737	-	
Gate Total Charge	Q_G	V_{GS}=10V, V_{DS}=30V, I_D=50A	-	87	-	nC
Gate-Source charge	Q_{gs}		-	30	-	
Gate-Drain charge	Q_{gd}		-	15	-	
Turn-on delay time	$t_{d(on)}$	T_j=25°C, V_{GS}=10V, V_{DS}=30V, R_L=6Ω	-	7	-	ns
Rise time	t_r		-	26	-	
Turn-off delay time	$t_{d(off)}$		-	63	-	
Fall time	t_f		-	77	-	
Gate resistance	R_G	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	1	-	Ω

Body Diode Characteristic

Body Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_{SD}=40A	-	0.78	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=30A, dI/dt=500A/μs	-	44	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=30A, dI/dt=100A/μs	-	198	-	nC

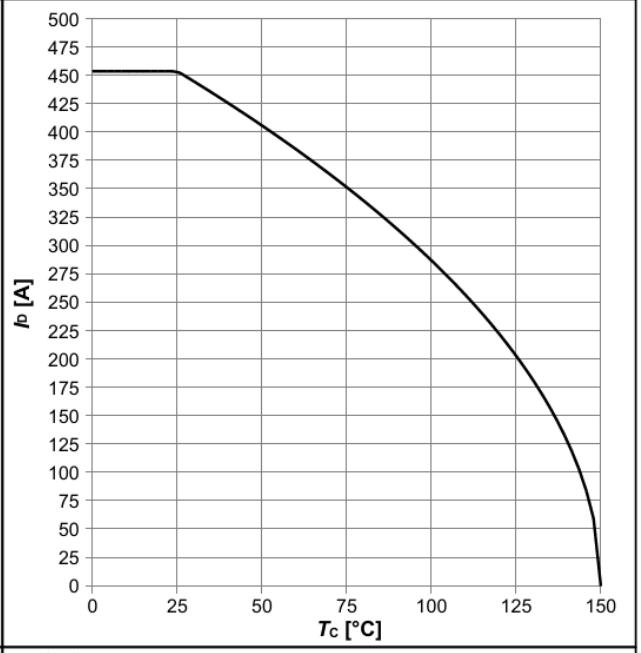
Typical Performance Characteristics

Diagram 1: Power dissipation



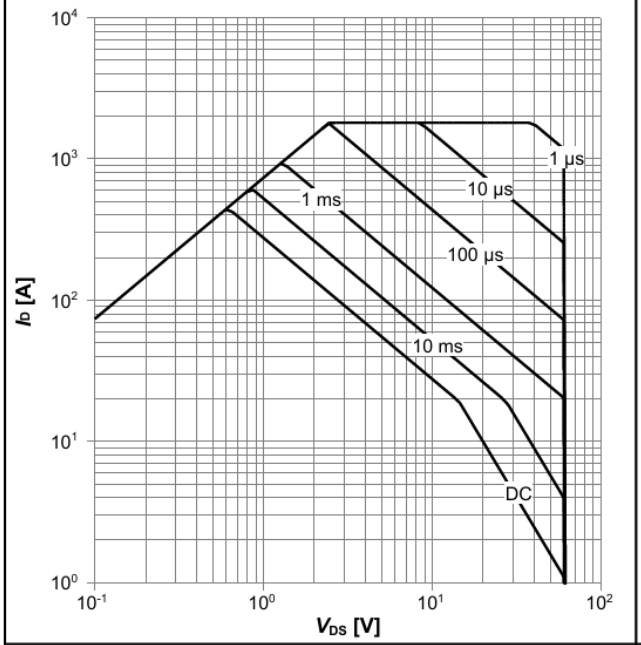
$P_{tot}=f(T_C)$

Diagram 2: Drain current



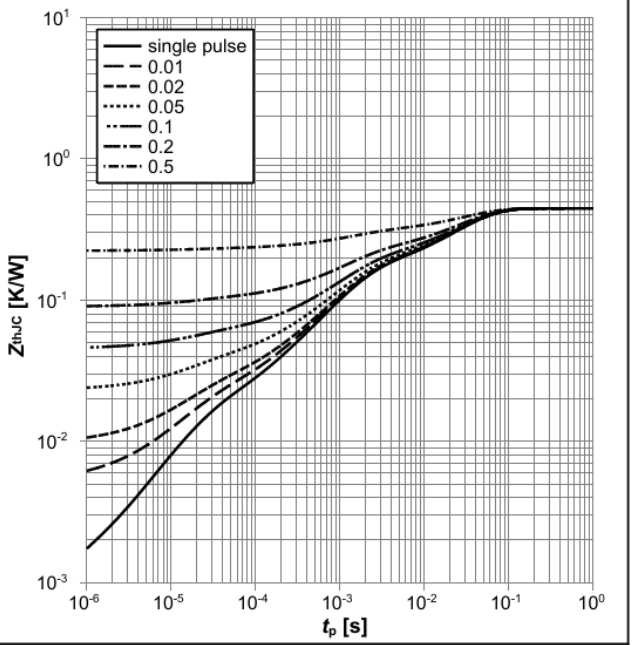
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



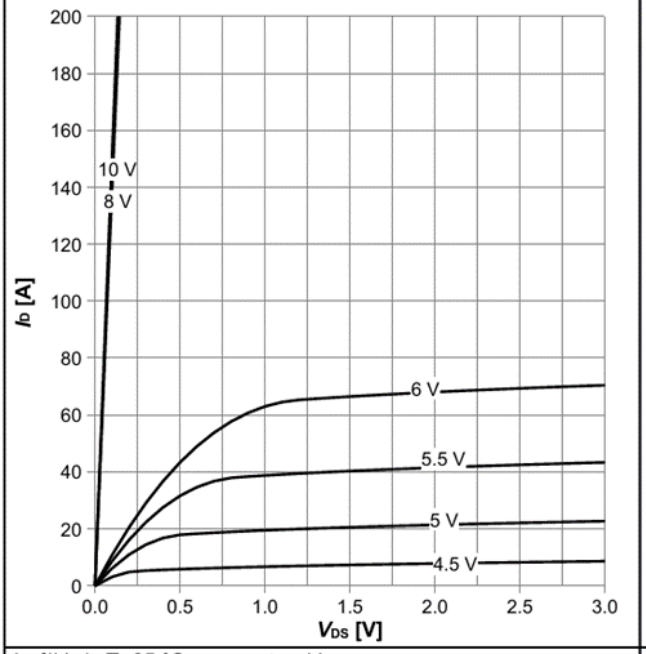
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



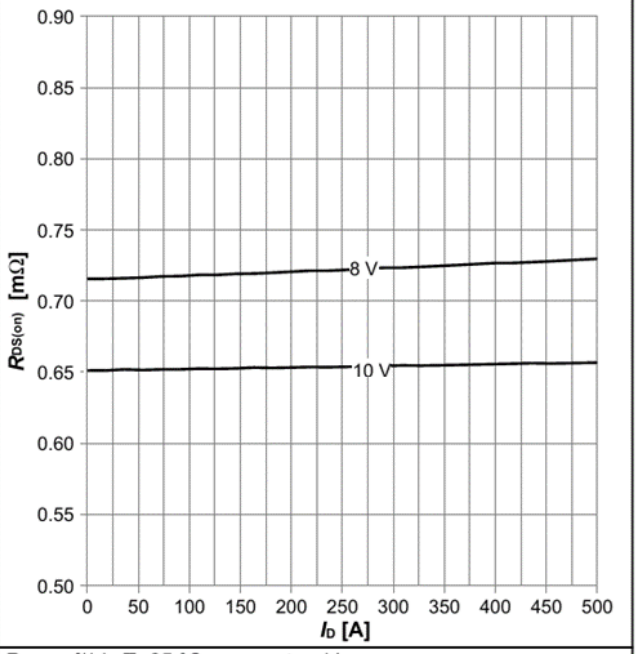
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



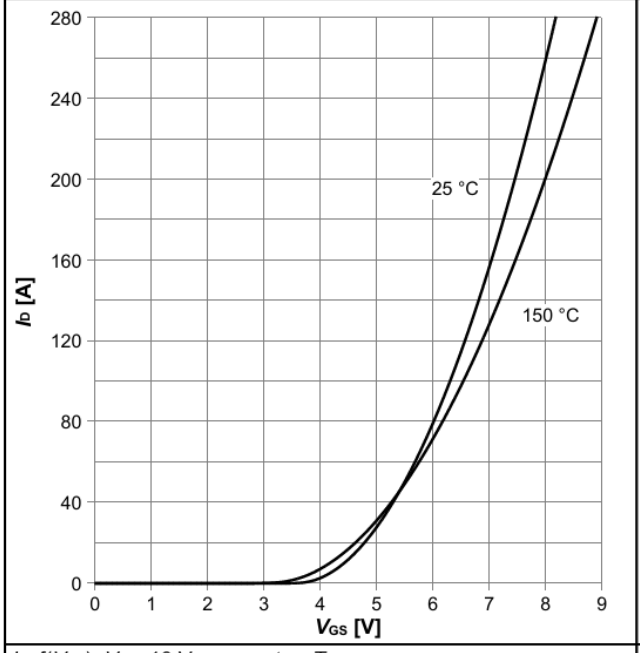
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



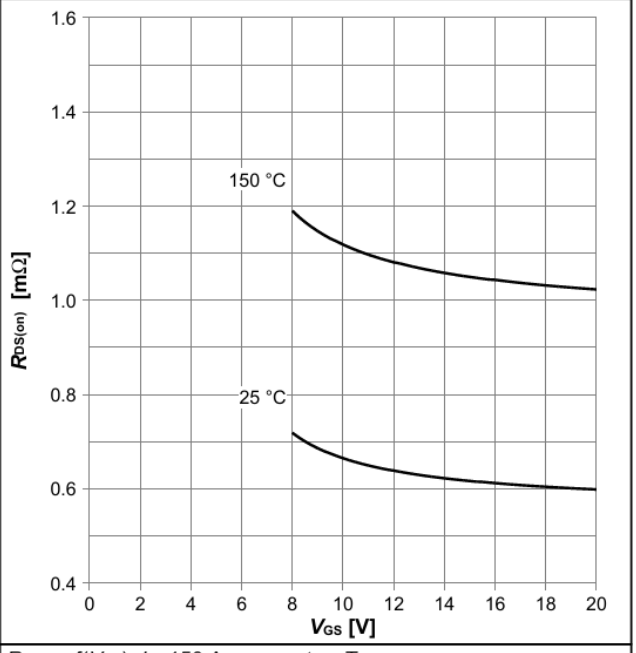
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



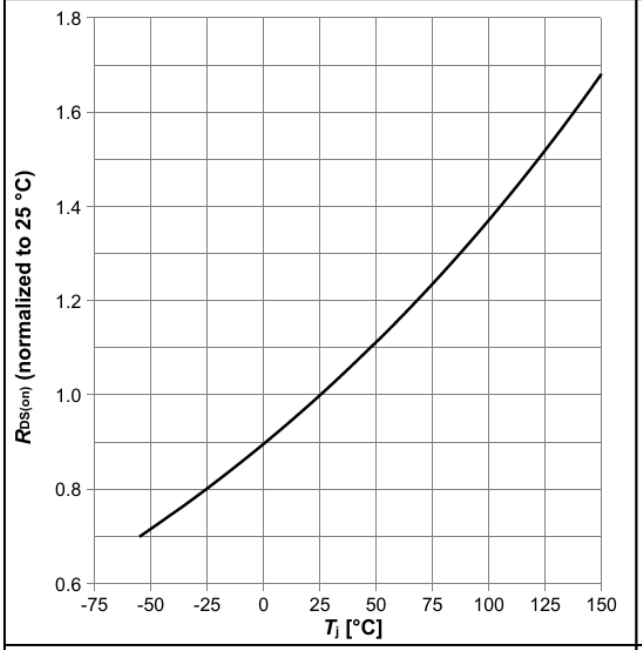
$I_D=f(V_{GS})$, $V_{DS}=10$ V; parameter: T_j

Diagram 8: Typ. drain-source on resistance



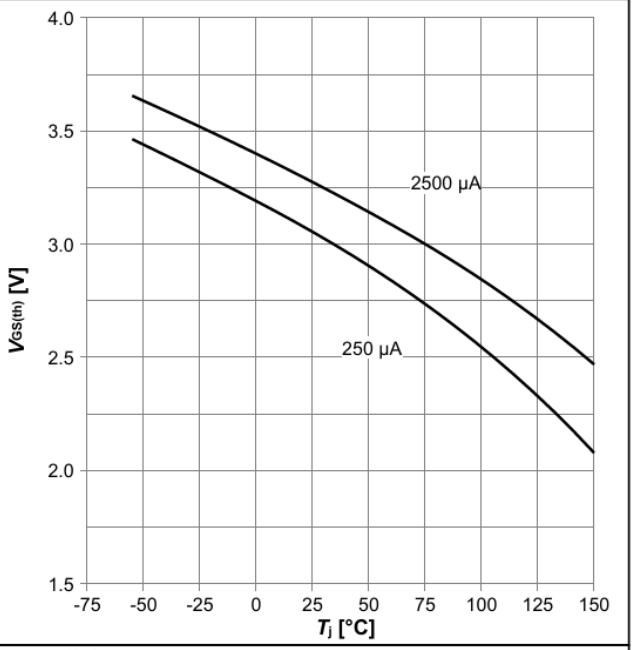
$R_{DS(on)}=f(V_{GS})$, $I_D=150$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



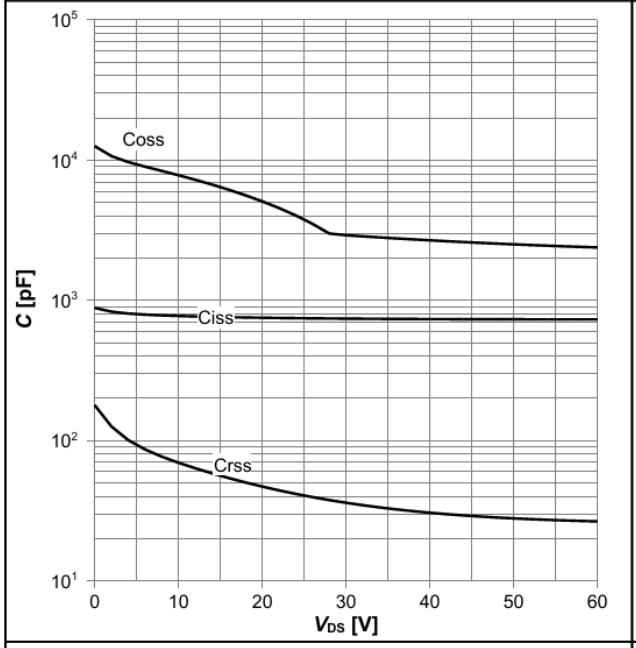
$R_{DS(on)}$=f(T_j), I_D=150 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



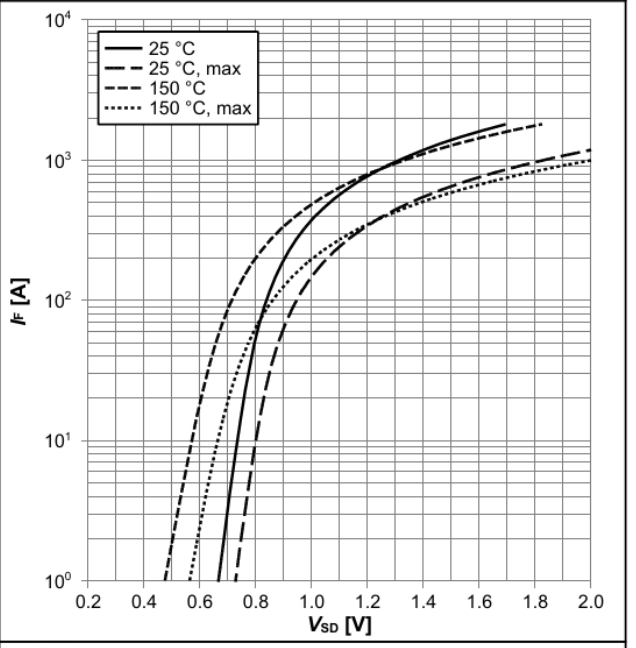
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



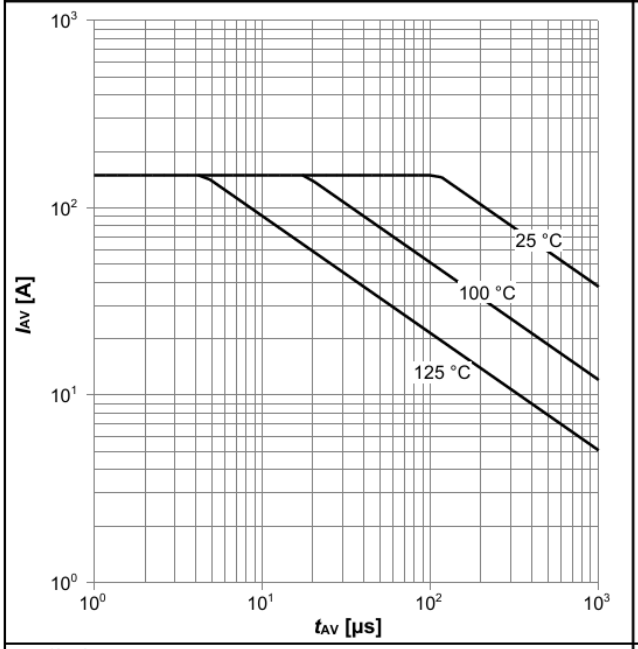
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



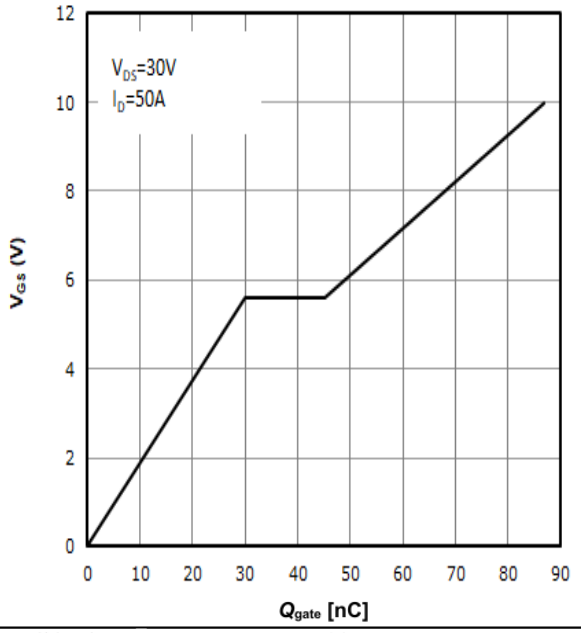
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



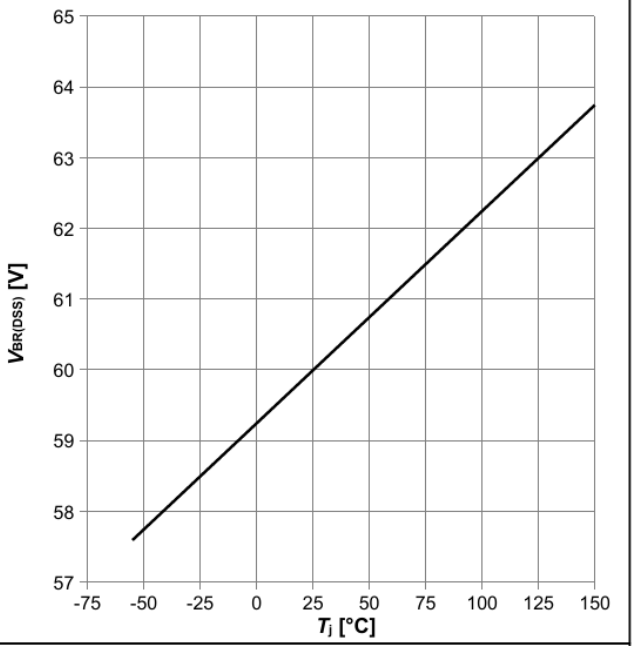
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate})$, I_D= 50 A pulsed, T_j=25 °C; parameter: V_{DD}

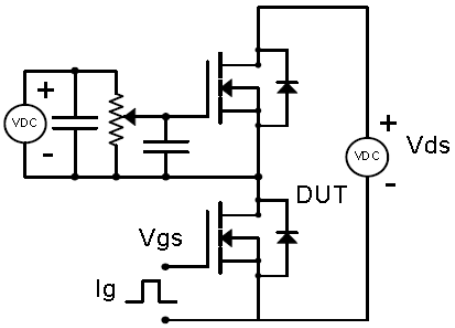
Diagram 15: Drain-source breakdown voltage

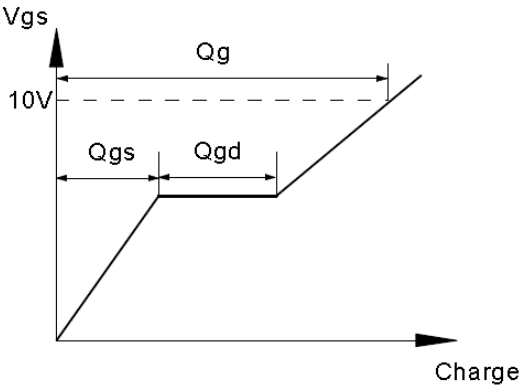


$V_{BR(DSS)}=f(T_j)$; I_D=1 mA

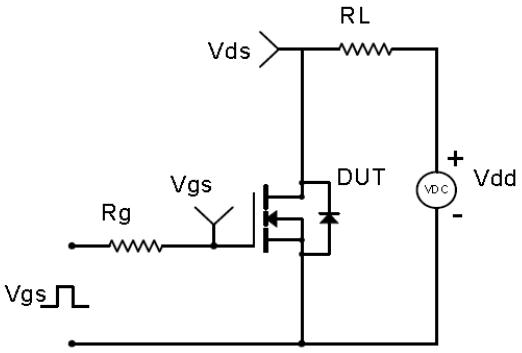
Test Circuit & Waveform

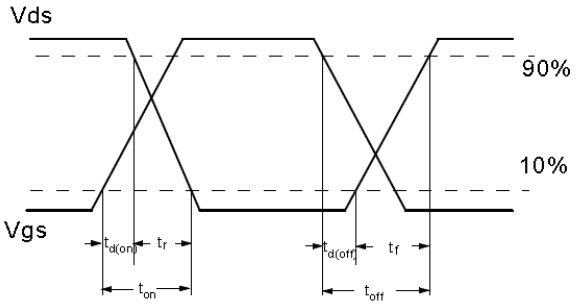
Gate Charge Test Circuit & Waveform



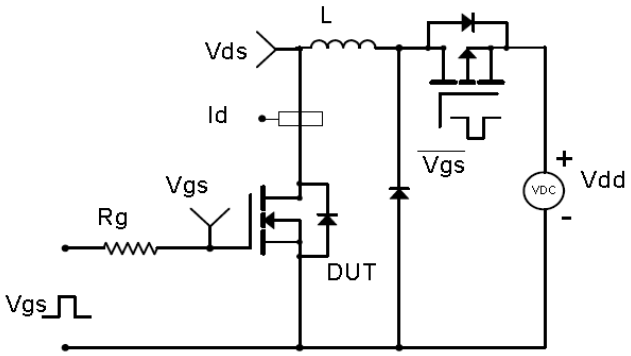


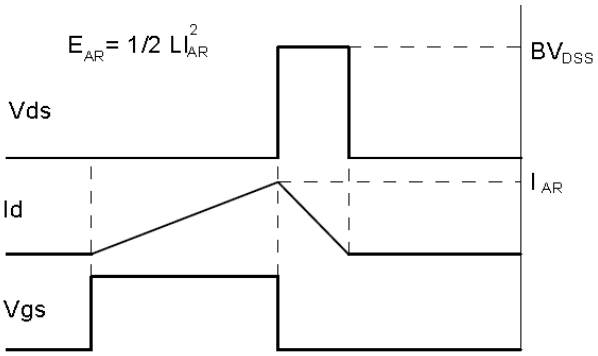
Resistive Switching Test Circuit & Waveforms



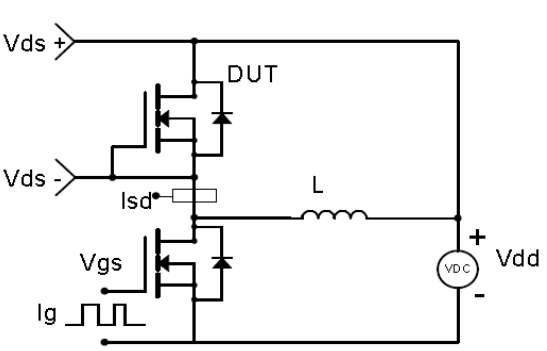


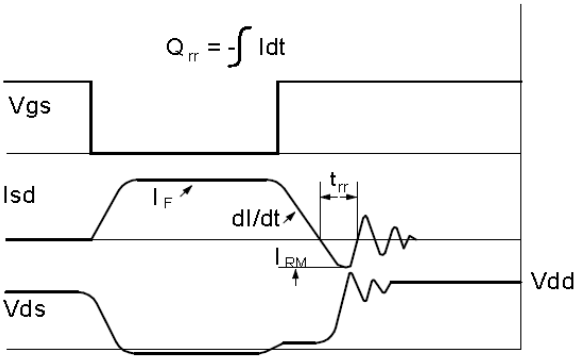
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



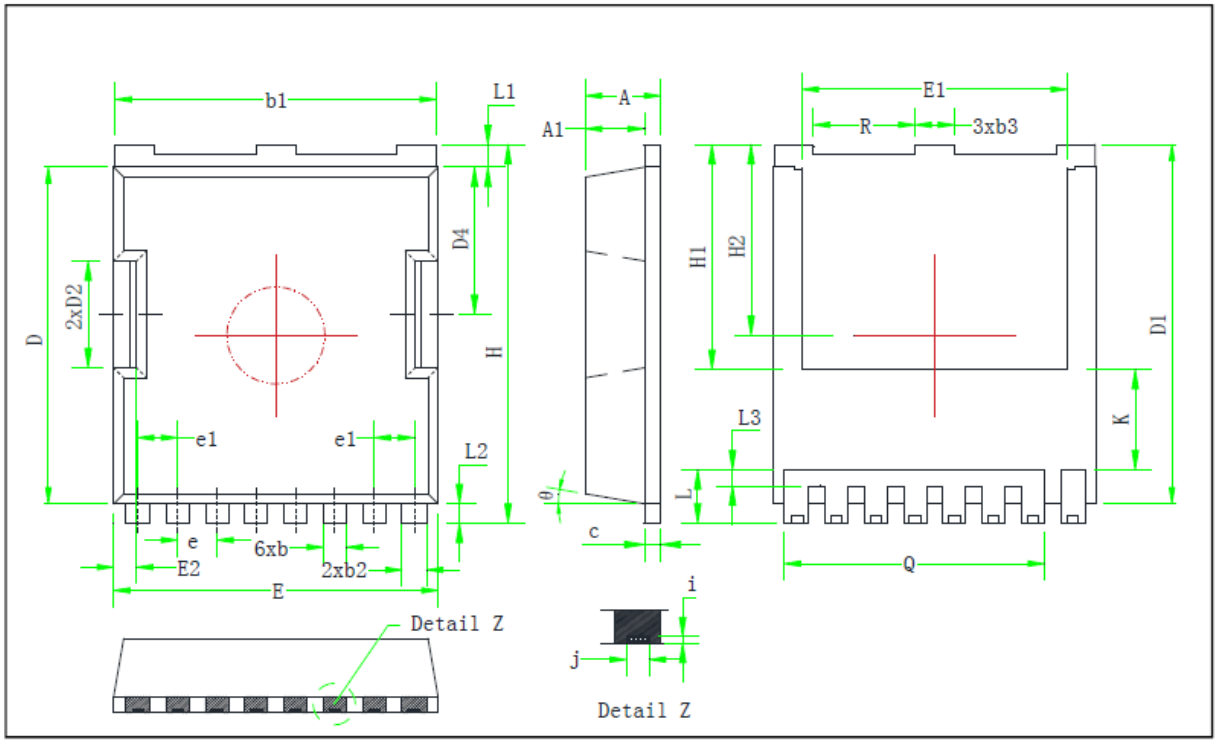


Diode Recovery Test Circuit & Waveforms





Package Outline:TOLL



Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
A	2.25	2.30	2.35		E2	0.65	0.70	0.75
A1	1.75	1.80	1.85		H	11.60	11.70	11.80
b	0.65	0.70	0.75		H1	6.95 BSC		
b1	9.75	9.80	9.85		H2	5.90 BSC		
b2	0.70	0.75	0.80		i	0.10 REF		
b3	1.15	1.20	1.25		j	0.35 REF		
c	0.45	0.50	0.55		K	3.10 REF		
D	10.35	10.40	10.45		L	1.55	1.65	1.75
D1	11.00	11.10	11.20		L1	0.65	0.70	0.75
D2	3.25	3.30	3.35		L2	0.50	0.60	0.70
D4	4.50	4.55	4.60		L3	0.40	0.50	0.60
e	1.20 BSC				Q	7.95 REF		
e1	1.225 BSC				R	3.05	3.10	3.15
E	9.85	9.90	9.95		θ	10°REF		
E1	8.00	8.10	8.20					