

Features

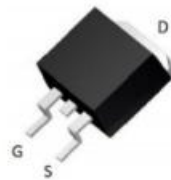
- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

Application

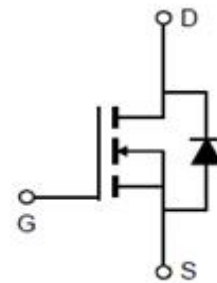
- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications

Product Summary

V_{DS}	100V
$R_{DS(on)}@V_{GS}=10V$	2.8mΩ
I_D	160A



TO-263 top view



Package Marking and Ordering Information

Type	Package	Marking	Reel Size	Tape Width	Qty
LR035N10SM2	TO-263	LR035N10SM2	330*28.5mm	24mm	800

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	160 128	A
Pulsed drain current $T_C = 25^\circ\text{C}$, t_p limited by T_{jmax}	$I_{D \text{ pulse}}$	640	
Avalanche energy, single pulse ($L=0.3\text{mH}$, $R_g=25\Omega$) ⁽¹⁾	E_{AS}	600	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation $T_C = 25^\circ\text{C}$	P_D	183	W
Operating junction and storage temperature	T_j, T_{stg}	-55~150	°C

Notes:

(1) $V_{DS}=50V, V_{GS}=10V, L=0.3\text{mH}$.

Thermal Resistance

	Symbol	Value	Unit
Thermal resistance, junction – case. Max	R_{thJC}	0.75	°C/W

Electrical Characteristic, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Test Condition	Value			Unit
			min.	typ.	max.	

Static Characteristic

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$ $T_j=25^\circ C$	2.4	3	3.6	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$ $T_j=25^\circ C$	-	-	1	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A,$ $T_j=25^\circ C$	-	2.8	3.5	mΩ
Transconductance	g_{fs}	$V_{DS}=5V, I_D=50A$	-	100	-	S

Dynamic Characteristic

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=50V,$ $f=1MHz$	-	7040	-	pF
Output Capacitance	C_{oss}		-	1010	-	
Reverse Transfer Capacitance	C_{rss}		-	35	-	
Gate Total Charge	Q_G	$V_{GS}=10V, V_{DS}=50V,$ $I_D=50A$	-	122	-	nC
Gate-Source charge	Q_{gs}		-	28	-	
Gate-Drain charge	Q_{gd}		-	36	-	
Turn-on delay time	$t_{d(on)}$	$V_{GS}=10V, V_{DS}=50V,$ $R_G=3\Omega$	-	48	-	ns
Rise time	t_r		-	56	-	
Turn-off delay time	$t_{d(off)}$		-	75	-	
Fall time	t_f		-	33	-	
Gate resistance	R_G	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$	-	1	-	Ω

Body Diode Characteristic

Body Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=50A$	-	0.9	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F=100A,$ $dI/dt=100A/\mu s$	-	115	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}	$I_F=100A,$ $dI/dt=100A/\mu s$	-	320	-	nC

Typical Performance Characteristics

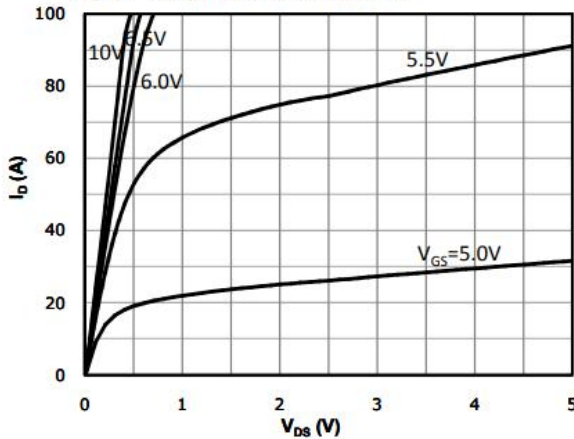
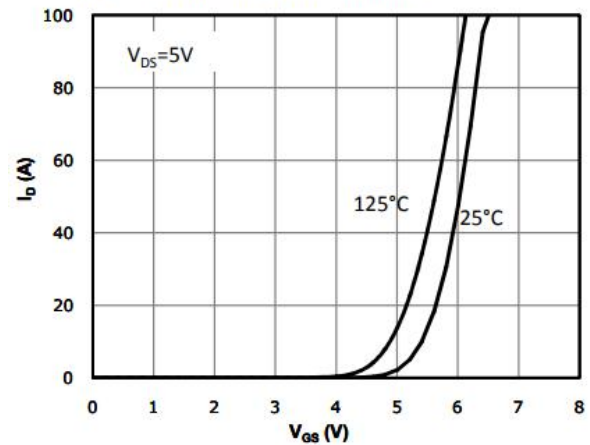
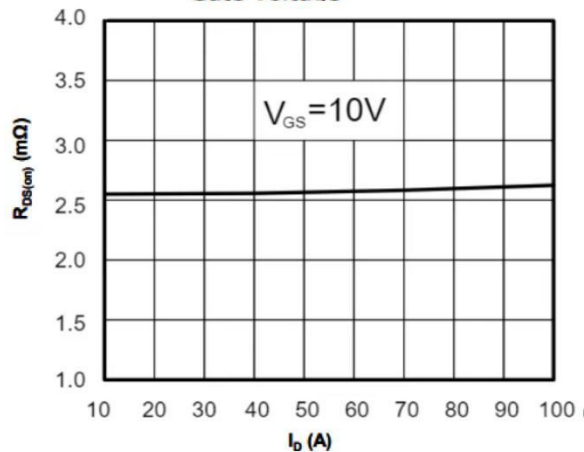
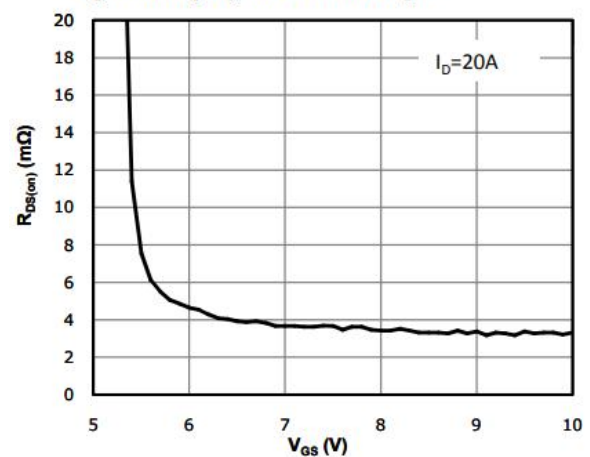
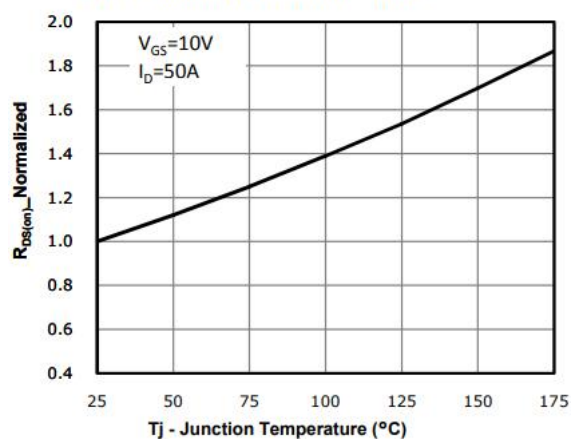
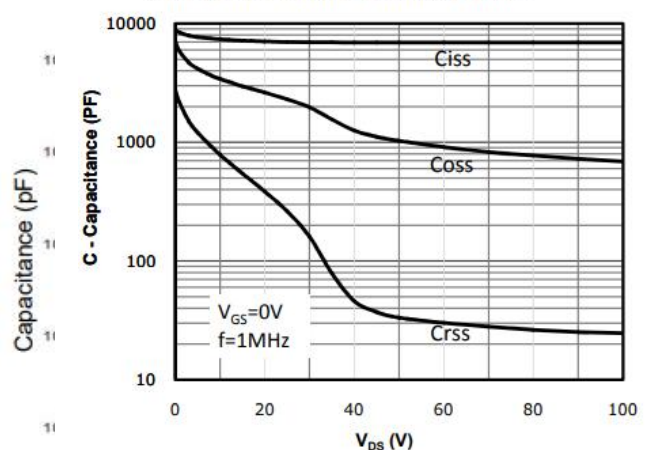
Fig 1: Output Characteristics

Fig 2: Transfer Characteristics

Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

Fig 4: $R_{DS(on)}$ vs Gate Voltage

Fig 5: $R_{DS(on)}$ vs. Temperature

Fig 6: Capacitance Characteristics


Fig 7: Gate Charge Characteristics

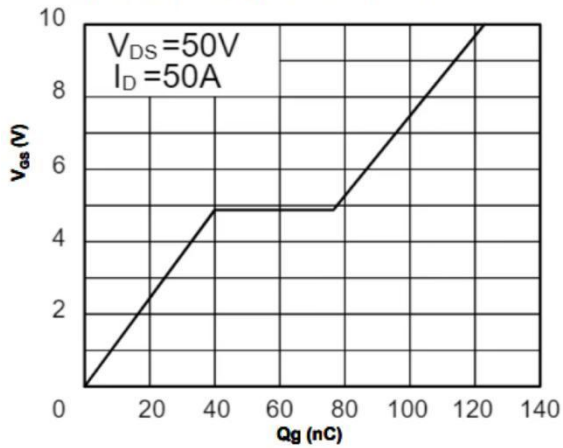


Fig 8: Body-diode Forward Characteristics

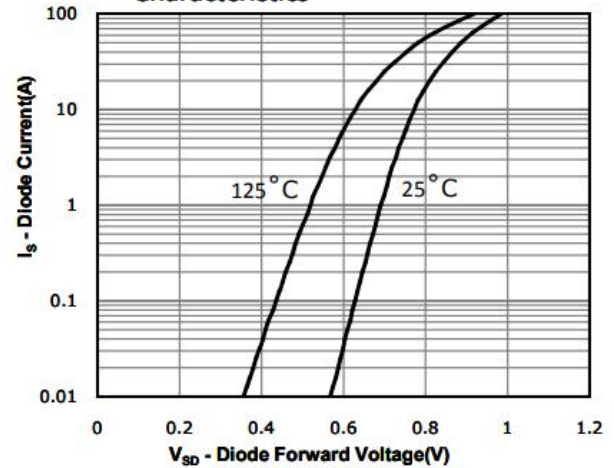


Fig 9: Power Dissipation

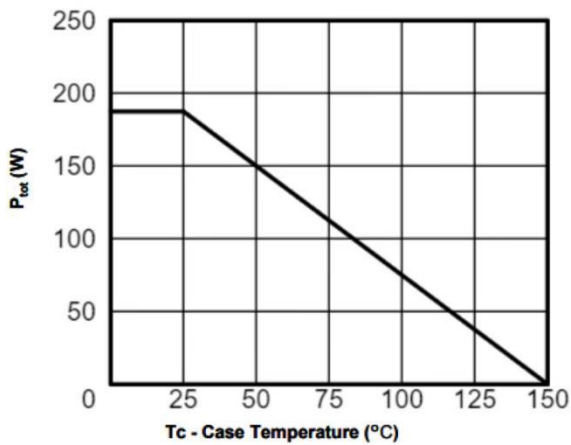


Fig 10: Drain Current Derating

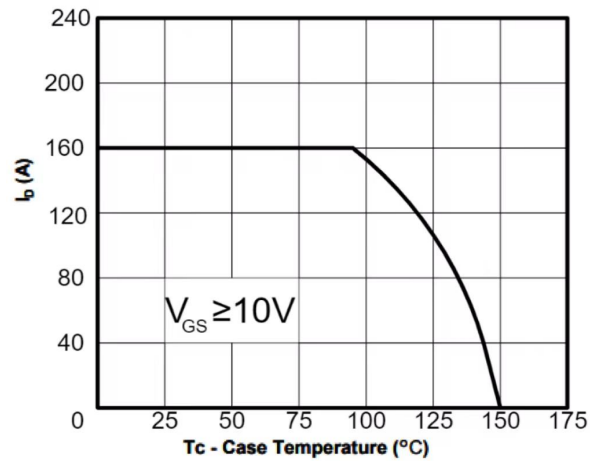


Fig 11: Safe Operating Area

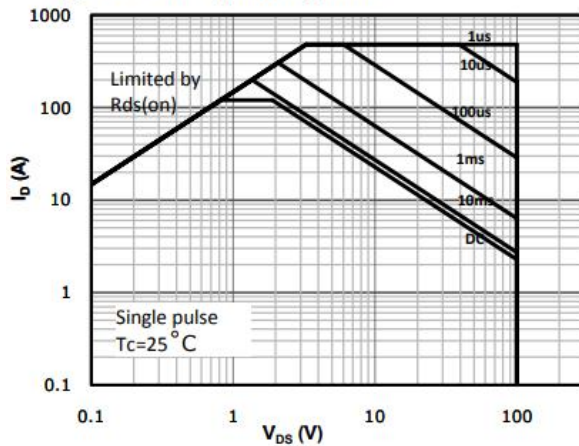
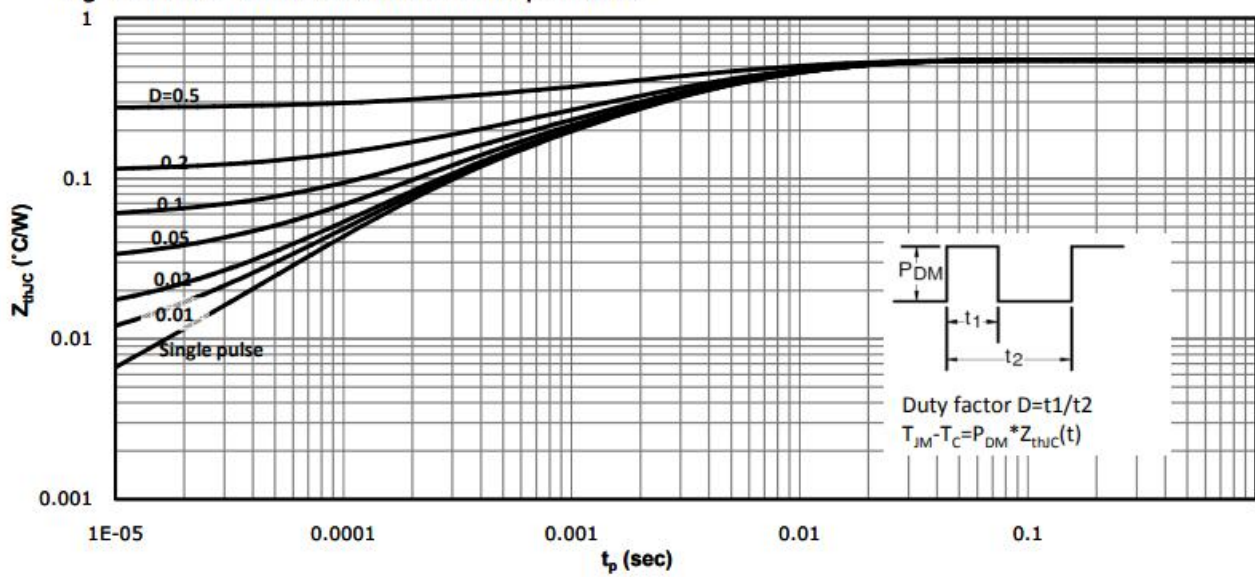
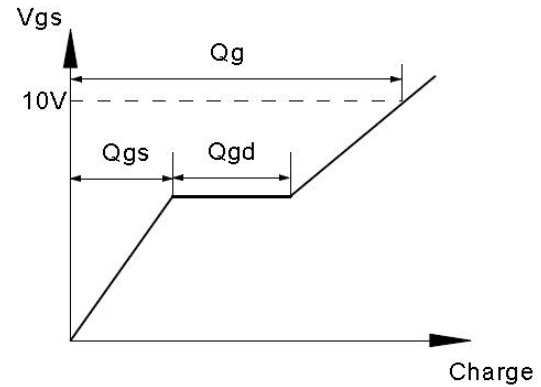
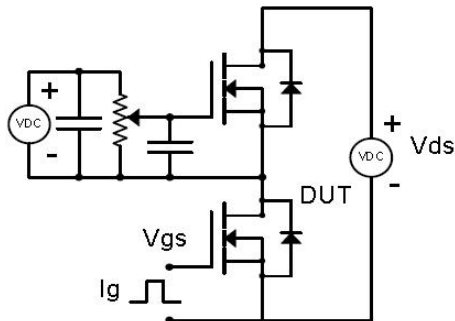


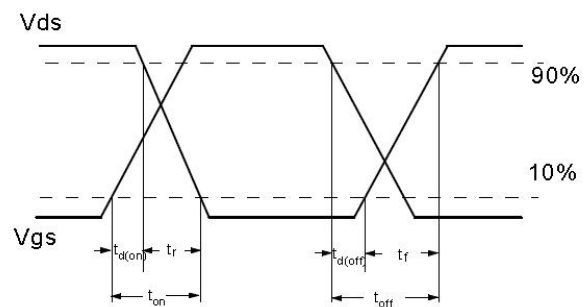
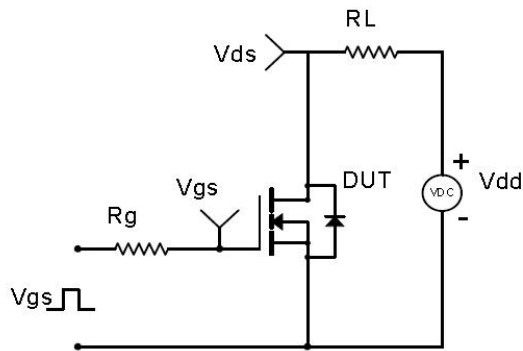
Fig 12: Max. Transient Thermal Impedance


Test Circuit & Waveform

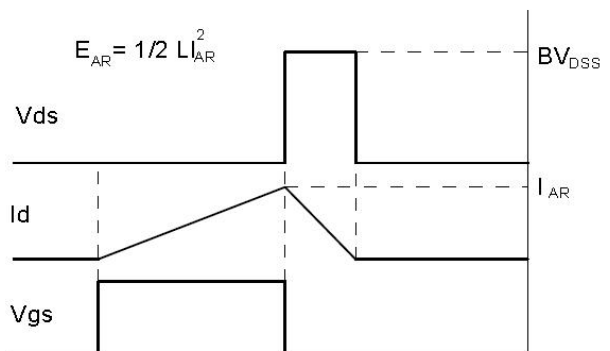
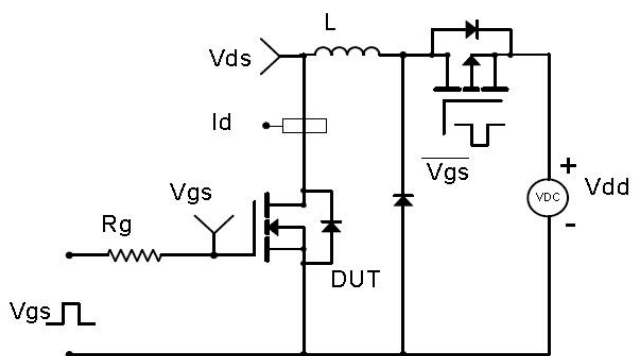
Gate Charge Test Circuit & Waveform

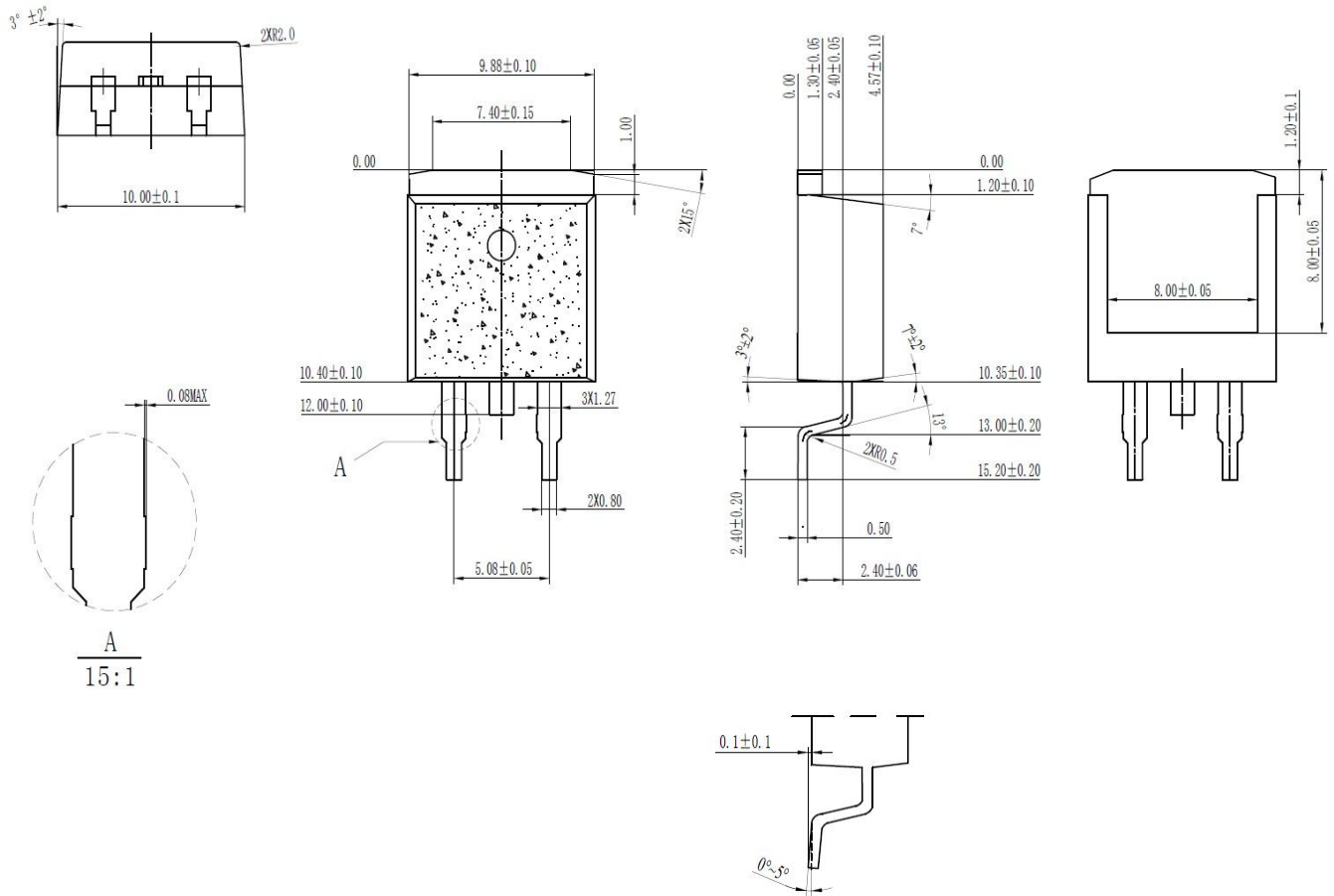


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Package Outline: TO-263

技术要求:

1. 塑封体中心与引线框架中心线偏差 ≤ 0.05 ,
上下塑封体中心偏差 ≤ 0.05 ;
2. 塑封体不准有缺损、气泡、气孔、裂纹等缺陷;
3. 塑封体表面除阴影部分为毛面, 其余为光面;
4. 未注脱模斜度 $\leq 5^\circ$;
5. 未注公差为 ± 0.05 , 未注圆角为 $R0.15$ (max)。