

Description

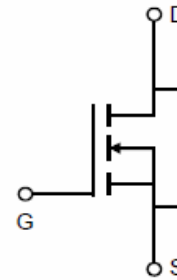
The RSTP40T20GU uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

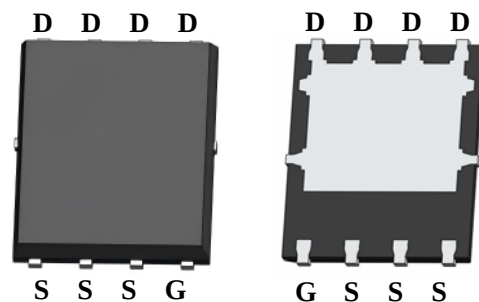
- $V_{DS} = 40V, I_D = 200A$
 $R_{DS(ON)} = 0.85m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 1.0m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View

Bottom View

100% UIS TESTED!

100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
RSTP40T20GU	RSTP40T20GU	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	200	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	150	A
Pulsed Drain Current (Package Limited)	I_{DM}	450	A
Maximum Power Dissipation	P_D	180	W
Derating factor		1.44	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	1800	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

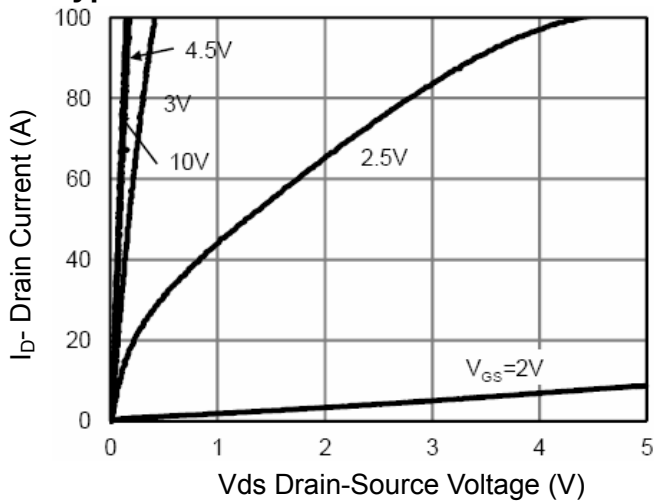
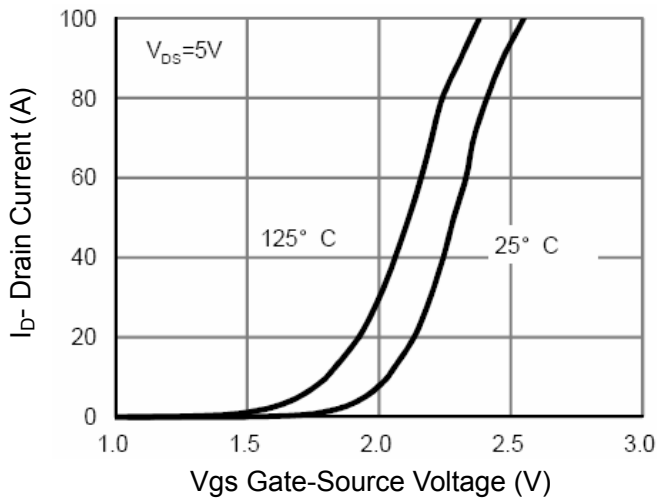
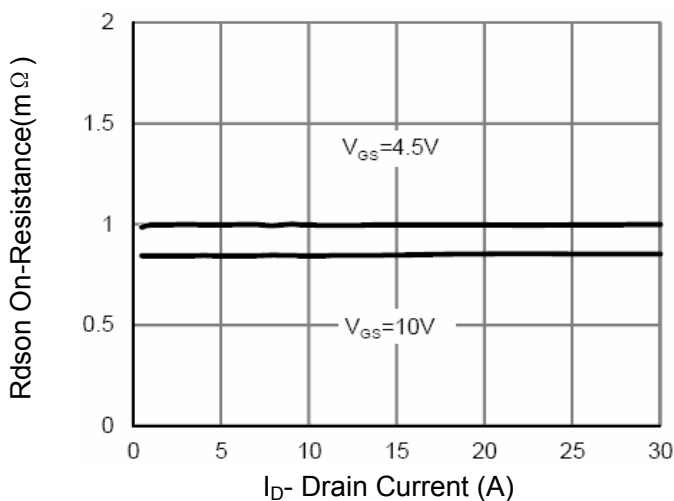
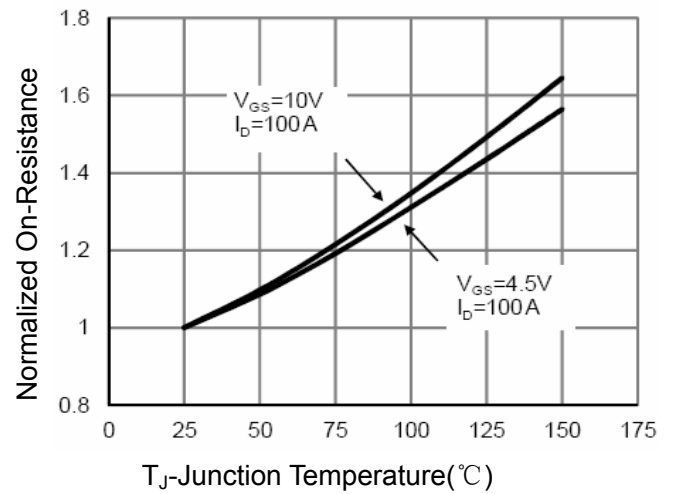
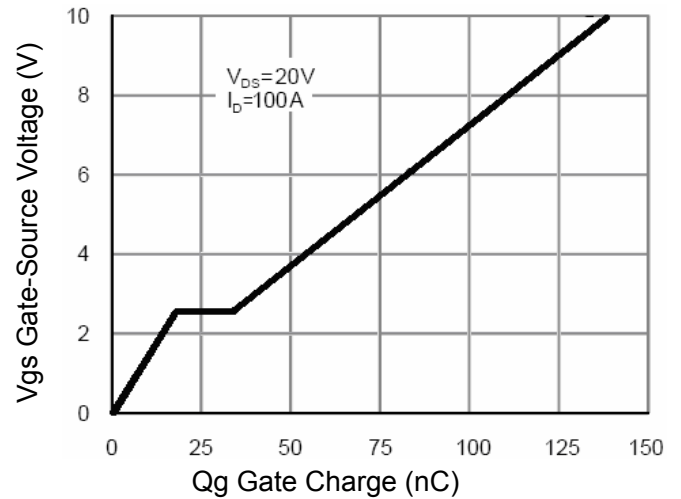
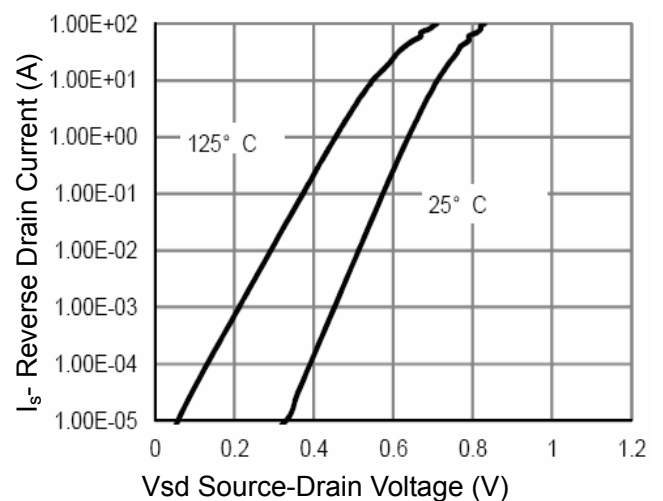
Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.67	°C/W
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =100A	-	0.85	1.0	mΩ
		V _{GS} =4.5V, I _D =100A	-	1.0	1.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =100A		90	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =20V,V _{GS} =0V, F=1.0MHz	-	8085	-	PF
Output Capacitance	C _{oss}		-	2123	-	PF
Reverse Transfer Capacitance	C _{rss}		-	121	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V,I _D =100A V _{GS} =10V,R _G =1.6Ω	-	13	-	nS
Turn-on Rise Time	t _r		-	8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	55	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Gate Charge	Q _g	V _{DS} =20V,I _D =100A, V _{GS} =10V	-	137	-	nC
Gate-Source Charge	Q _{gs}		-	19		nC
Gate-Drain Charge	Q _{gd}		-	14		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =100A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	200	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S	-	35	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	120	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5mH, R_G=25\Omega$

Pb Free Product
Typical Electrical and Thermal Characteristics

Figure 1 Output Characteristics

Figure 2 Transfer Characteristics

Figure 3 Rdson- Drain Current

Figure 4 Rdson-Junction Temperature

Figure 5 Gate Charge

Figure 6 Source- Drain Diode Forward

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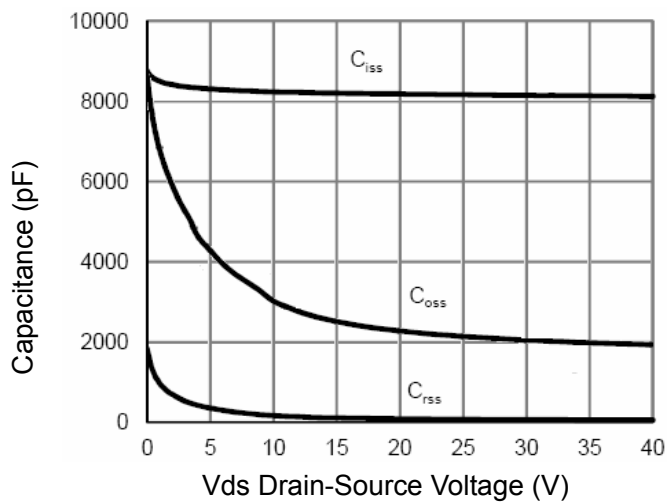


Figure 7 Capacitance vs Vds

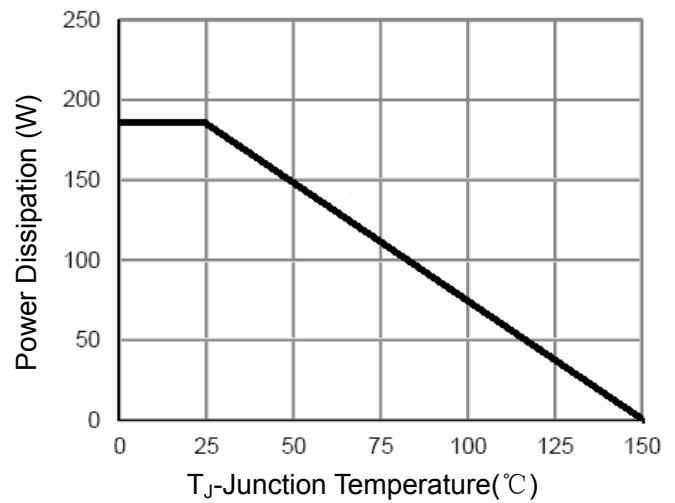


Figure 9 Power De-rating

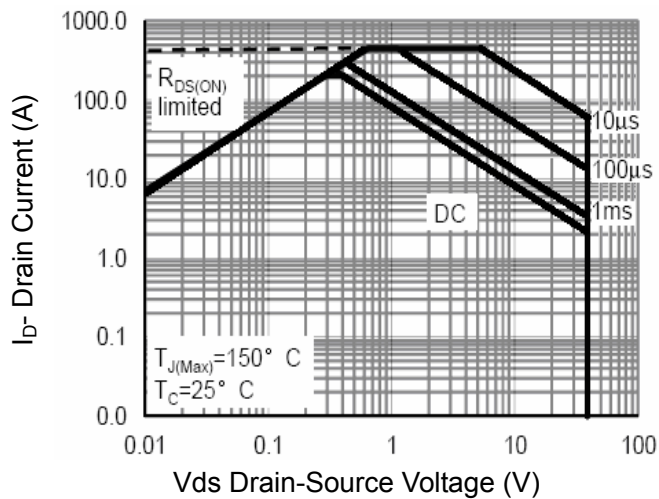


Figure 8 Safe Operation Area

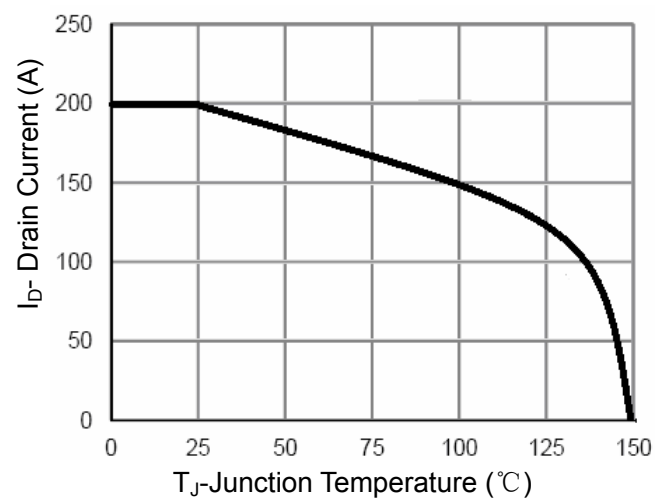


Figure 10 Current De-rating

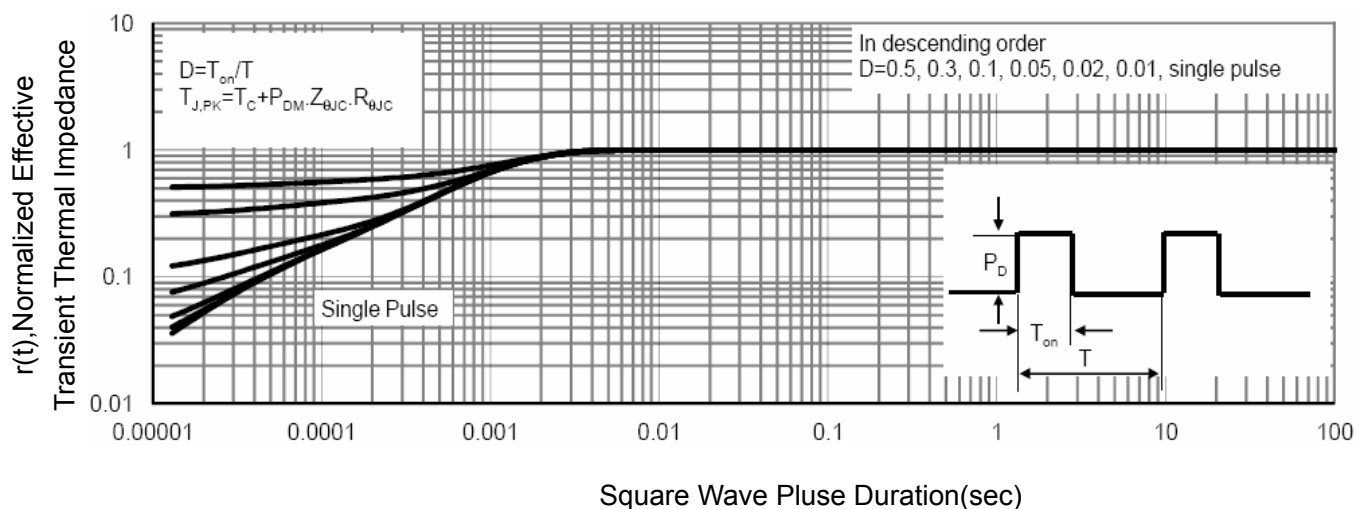


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information

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