

Description

The RST8060CK uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

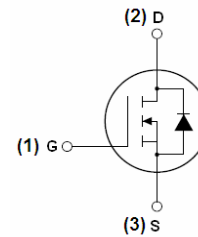
- $V_{DS} = 80V, I_D = 60A$
 $R_{DS(ON)} < 12\text{ m}\Omega @ V_{GS} = 10V$ (Typ: 9m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Special designed for convertors and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

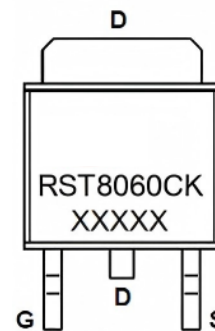
- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-252 -2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
RST8060CK	RST8060CK	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	60	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D (100^\circ\text{C})$	42.4	A
Pulsed Drain Current ^(Note 1)	I_{DM}	240	A
Maximum Power Dissipation	P_D	130	W
Derating factor		0.87	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	380	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.15	°C/W
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

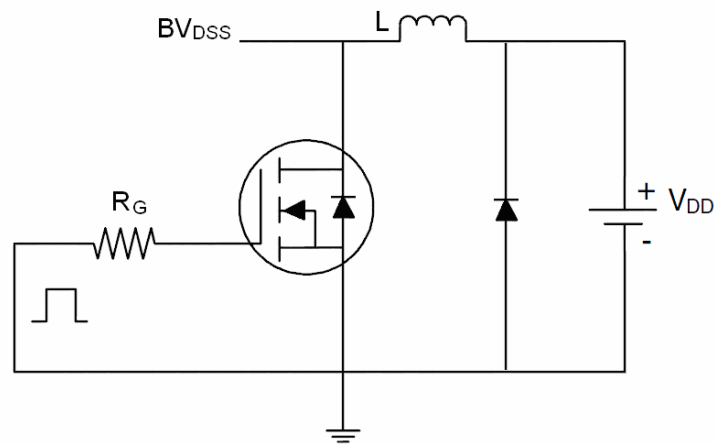
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	80	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	9	12	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	-	30	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	4414	-	PF
Output Capacitance	C _{OSS}		-	219	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	188	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =40V, R _L =15Ω R _G =2.5Ω, V _{GS} =10V	-	19	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	40	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =40V, I _D =20A, V _{GS} =10V	-	81.5	-	nC
Gate-Source Charge	Q _{gs}		-	26.9	-	nC
Gate-Drain Charge	Q _{gd}		-	23.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	60	A
Reverse Recovery Time	t _{rr}	T _j =25℃, I _F =20A di/dt=100A/μs ^(Note3)	-	36	-	nS
Reverse Recovery Charge	Q _{rr}		-	54	-	nC

Notes:

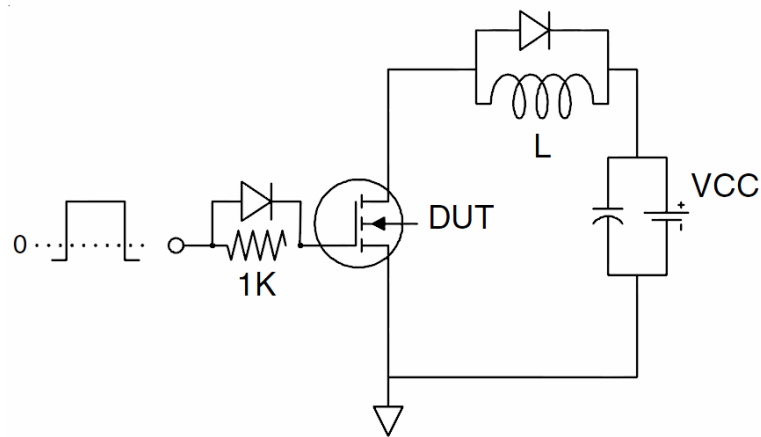
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=40V, V_G=10V, L=0.5mH, R_G=25\Omega$

Test Circuit

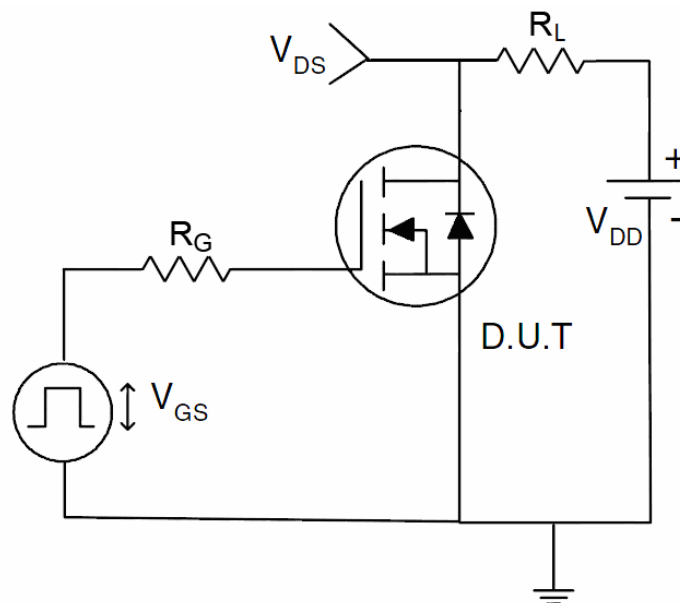
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

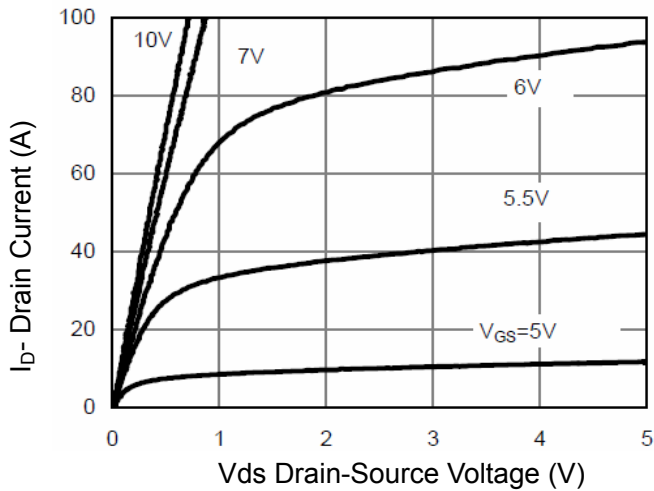


Figure 1 Output Characteristics

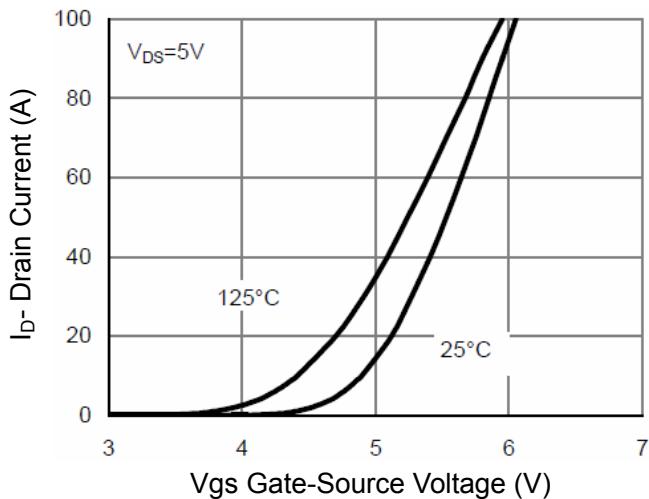


Figure 2 Transfer Characteristics

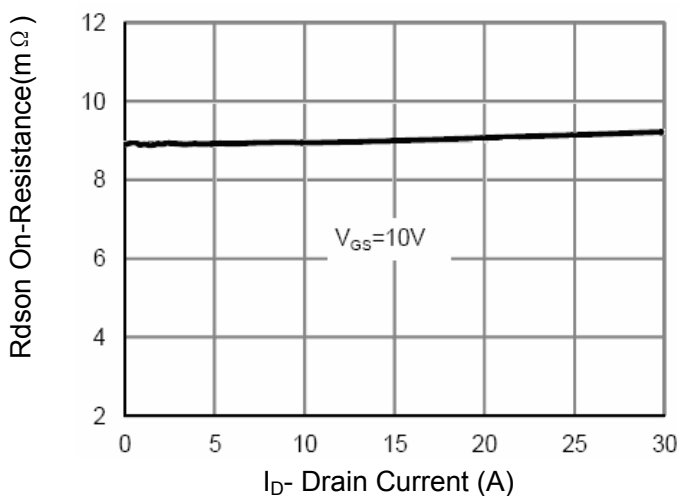


Figure 3 Rdson- Drain Current

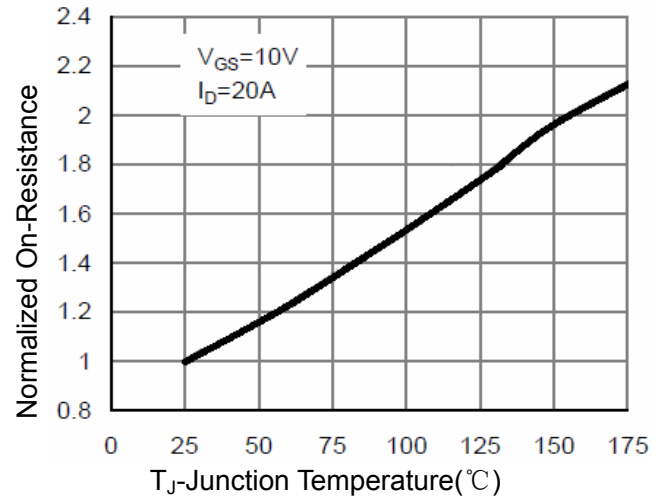


Figure 4 Rdson-Junction Temperature

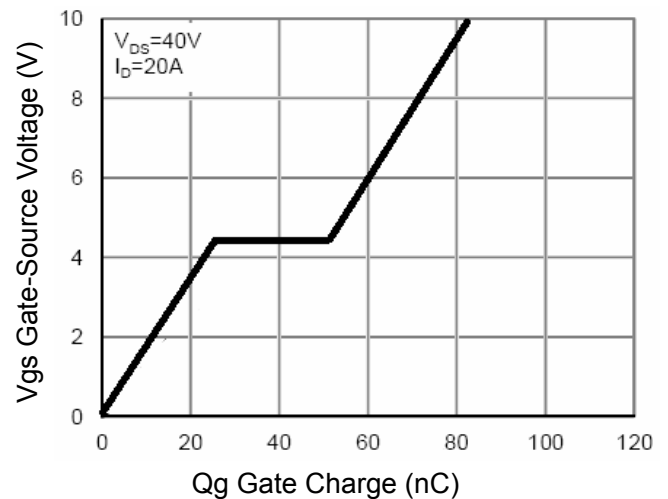


Figure 5 Gate Charge

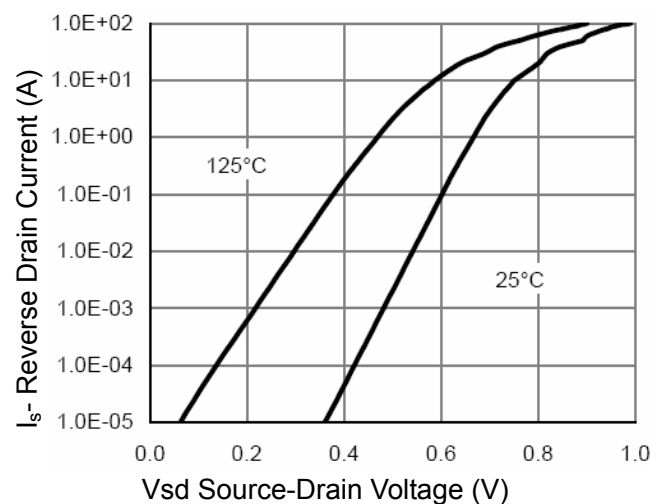


Figure 6 Source- Drain Diode Forward

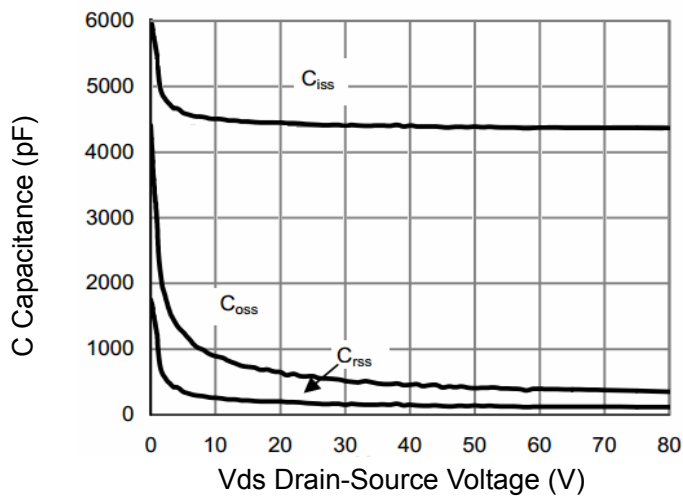


Figure 7 Capacitance vs Vds

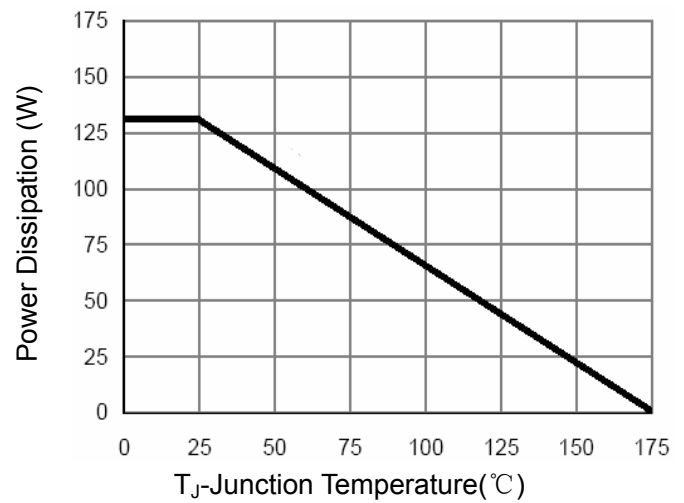


Figure 9 Power De-rating

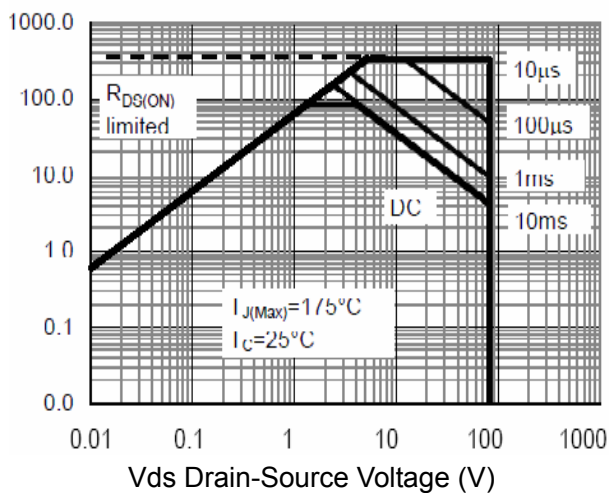


Figure 8 Safe Operation Area

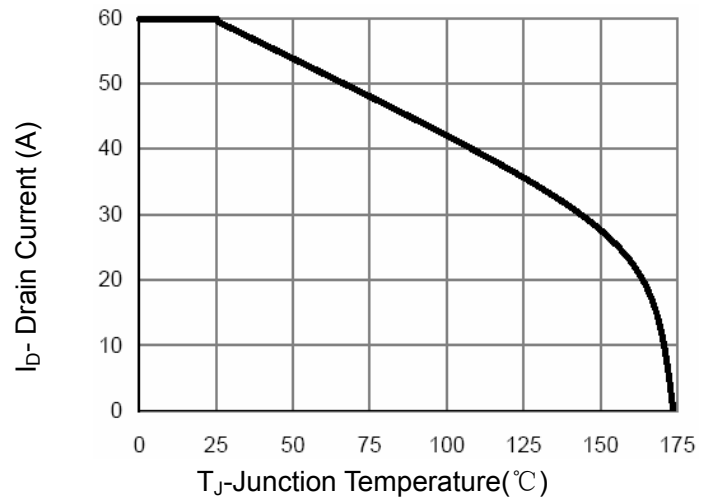


Figure 10 I_D Current De-rating

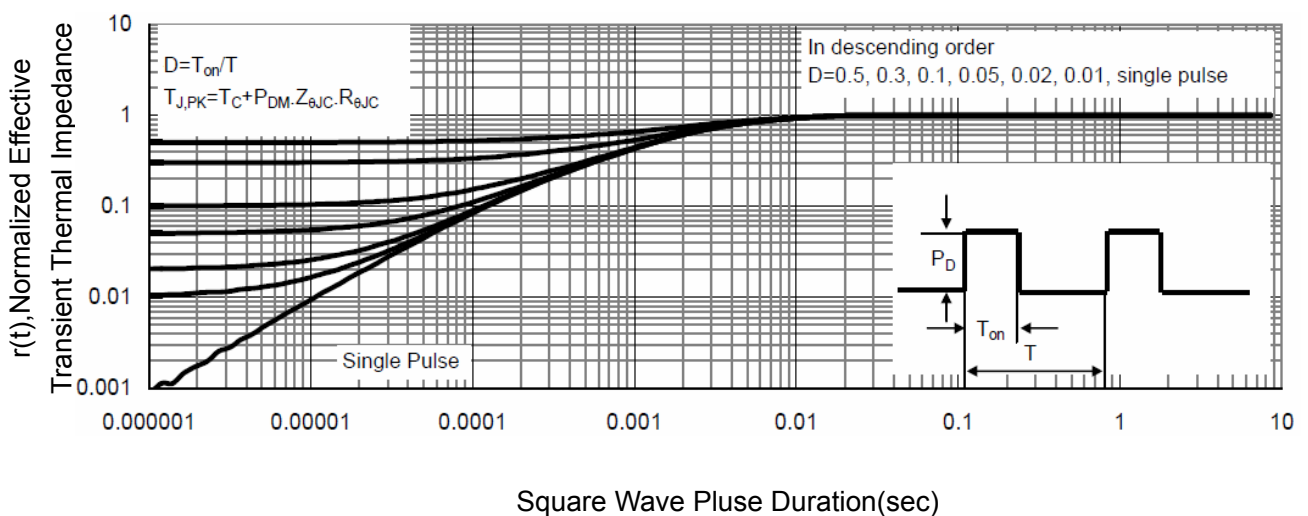
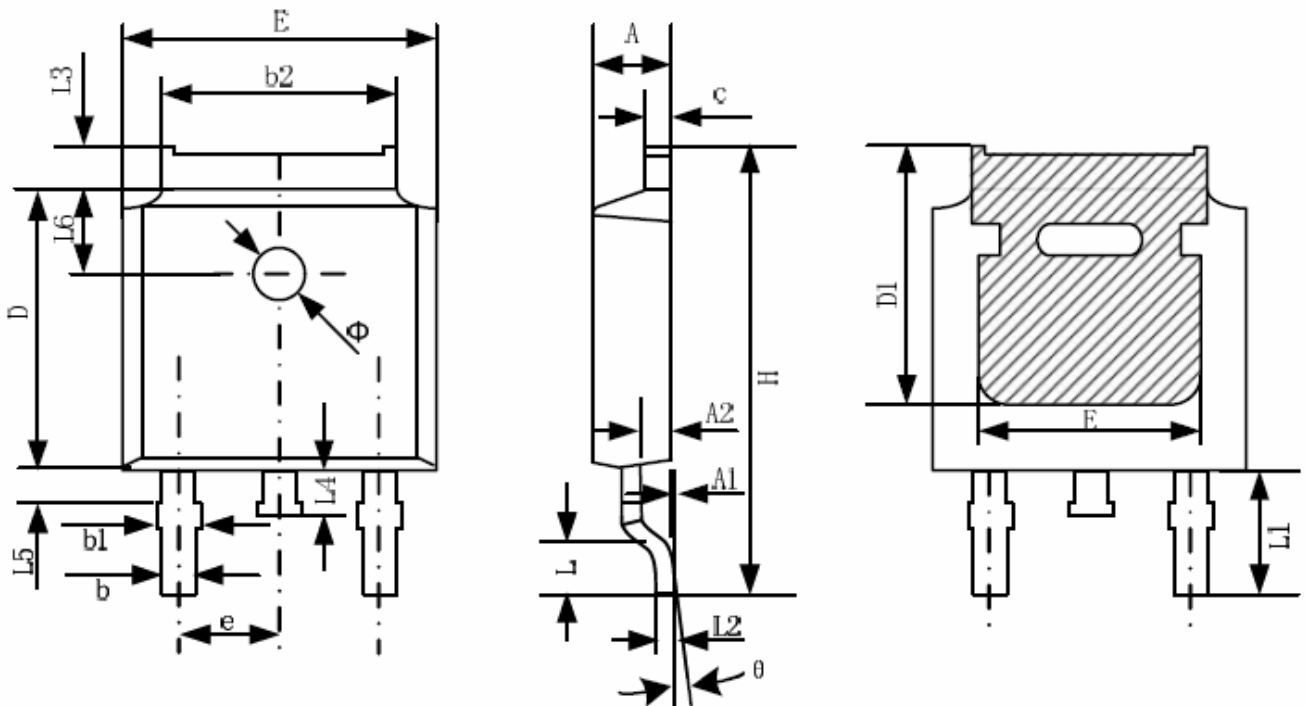


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.38	0.087	0.094
A1	0.00	0.10	0.000	0.004
A2	0.90	1.10	0.035	0.043
b	0.72	0.85	0.028	0.033
b1	0.72	0.90	0.028	0.035
b2	5.13	5.46	0.202	0.215
c	0.47	0.60	0.019	0.024
D	6.00	6.20	0.236	0.244
D1	5.25	--	0.207	--
E	6.50	6.70	0.256	0.264
E1	4.70	--	0.185	--
e	2.19	2.39	0.086	0.094
H	9.80	10.40	0.386	0.409
L	1.40	1.70	0.055	0.067
L1	2.90 REF		0.114 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039
L5	0.15	0.75	0.006	0.030
L6	1.80 REF		0.071 REF	
Φ	1.20	1.40	0.047	0.055
θ	0°	8°	0°	8°