

Pb Free Product

Description

The RST3050K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

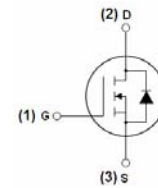
- $V_{DS} = 30V, I_D = 50A$
 $R_{DS(ON)} < 11m\Omega @ V_{GS}=10V$ (Typ:8m Ω)
 $R_{DS(ON)} < 16m\Omega @ V_{GS}=4.5V$ (Typ:10m Ω)
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

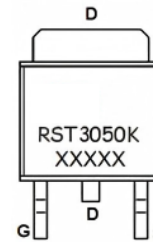
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

100% UIS TESTED!

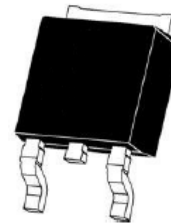
100% ΔV_{DS} TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
RST3050K	RST3050K	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	35.4	A
Pulsed Drain Current	I_{DM}	200	A
Maximum Power Dissipation	P_D	60	W
Derating factor		0.4	W/ $^{\circ}C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	100	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.5	$^{\circ}C/W$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

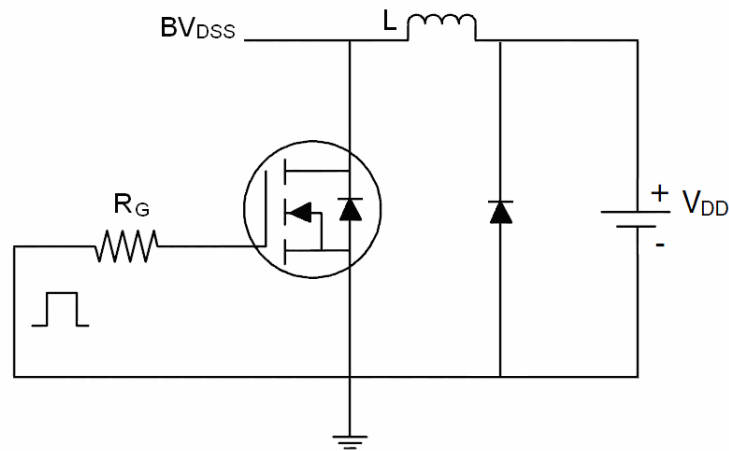
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	33	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.6	2.6	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	8	11	mΩ
		V _{GS} =4.5V, I _D =20A	-	10	16	
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A		20	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	2000	-	PF
Output Capacitance	C _{OSS}		-	280	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	210	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, I _D =20A V _{GS} =10V, R _{GEN} =1.8Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	25	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =20A, V _{GS} =10V	-	32.3	-	nC
Gate-Source Charge	Q _{gs}		-	4.9	-	nC
Gate-Drain Charge	Q _{gd}		-	6.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	0.85	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	50	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A di/dt = 100A/μs ^(Note3)	-	-	27	nS
Reverse Recovery Charge	Q _{rr}		-	-	20	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

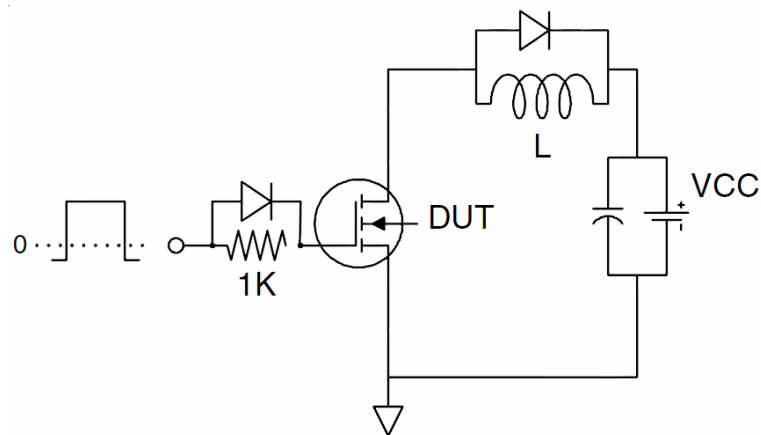
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}$, $V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

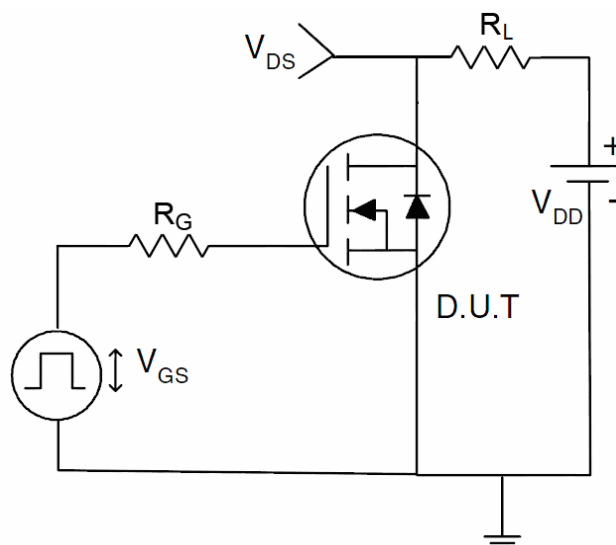
1) E_{AS} test Circuits

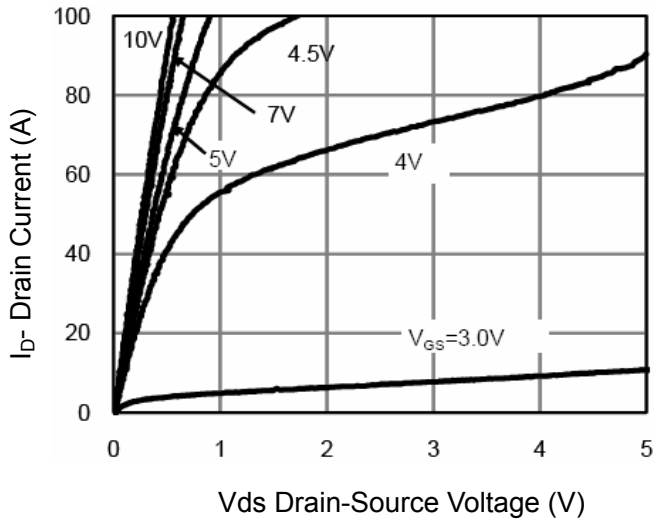
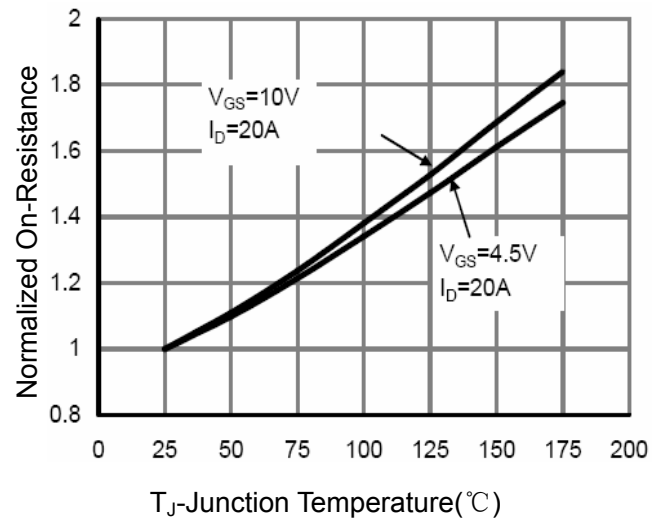
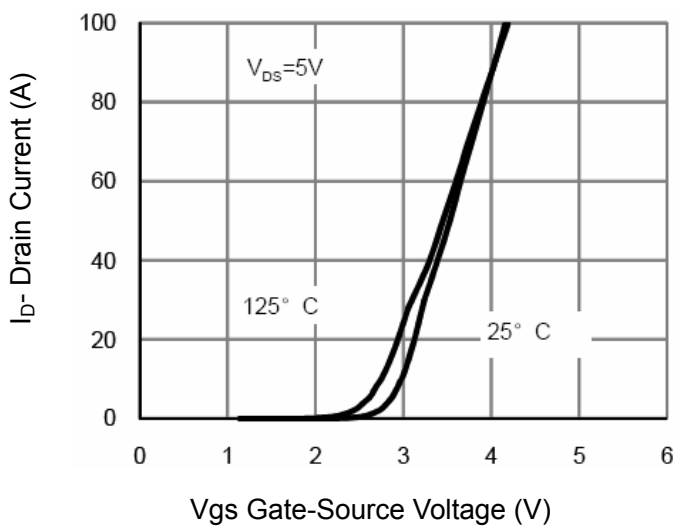
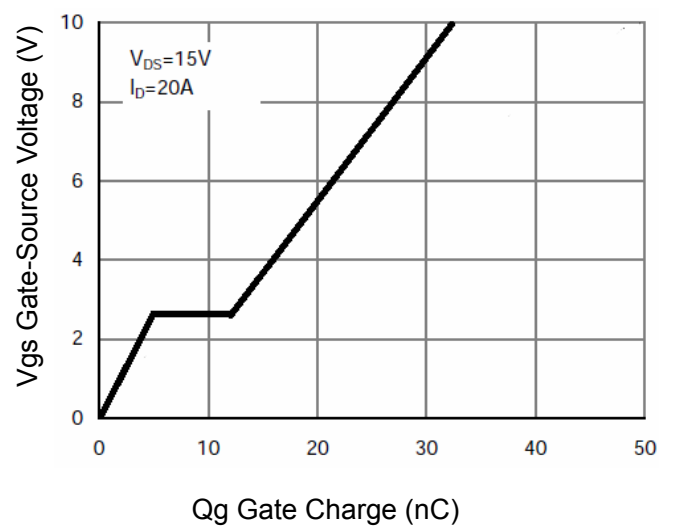
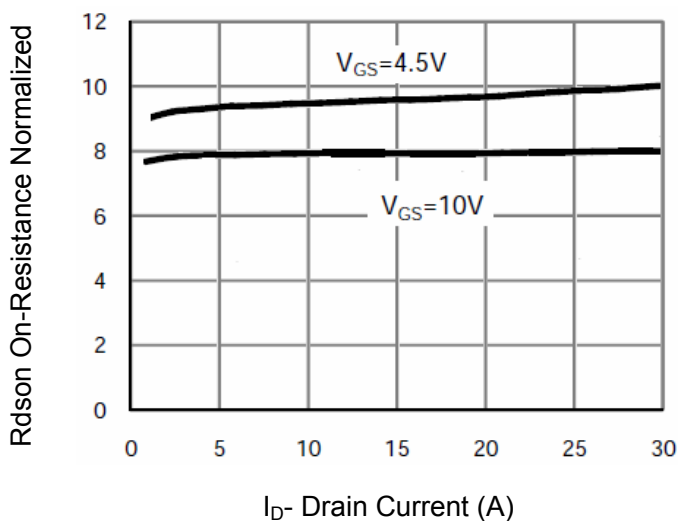
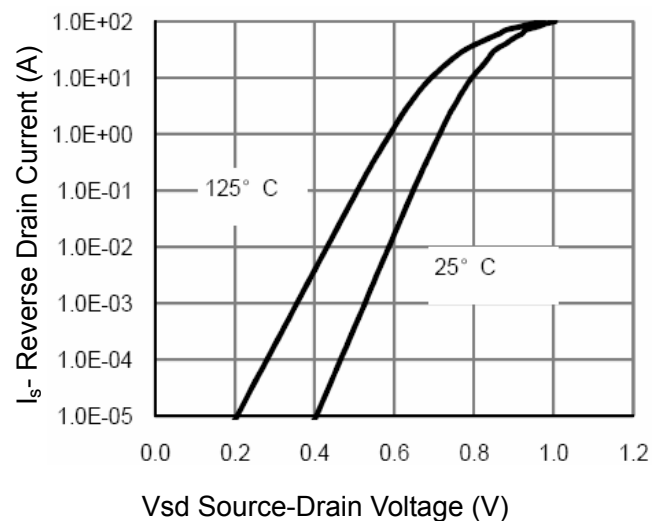


2) Gate charge test Circuit:

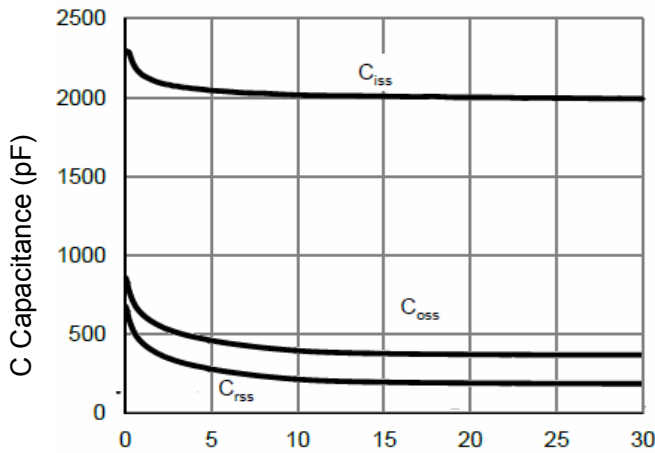


3) Switch Time Test Circuit:

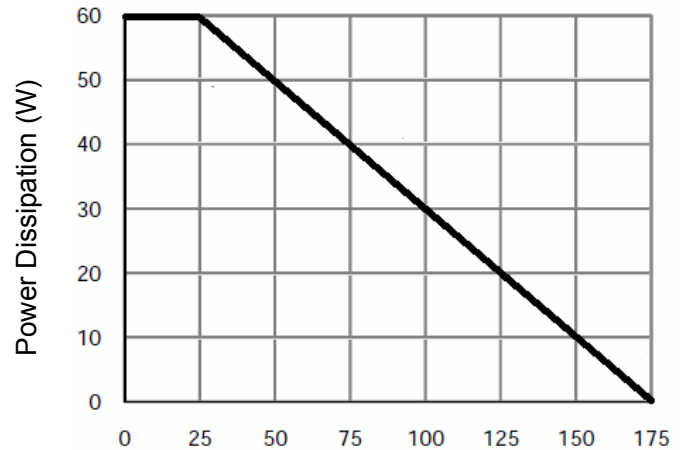


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Typical Electrical and Thermal Characteristics (Curves)

Figure 1 Output Characteristics

Figure 4 Rdson-Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 Rdson- Drain Current

Figure 6 Source- Drain Diode Forward

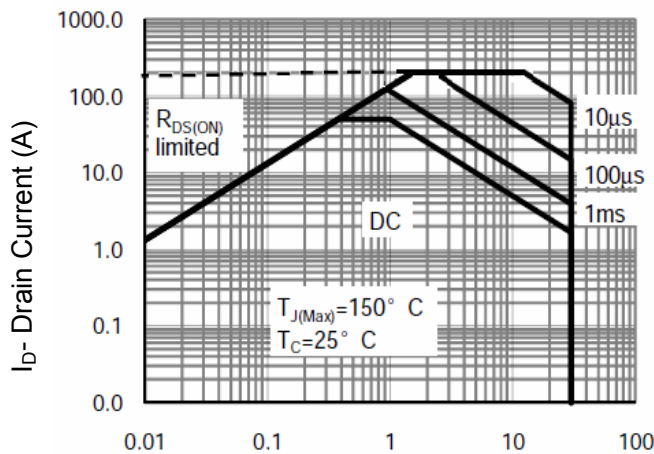
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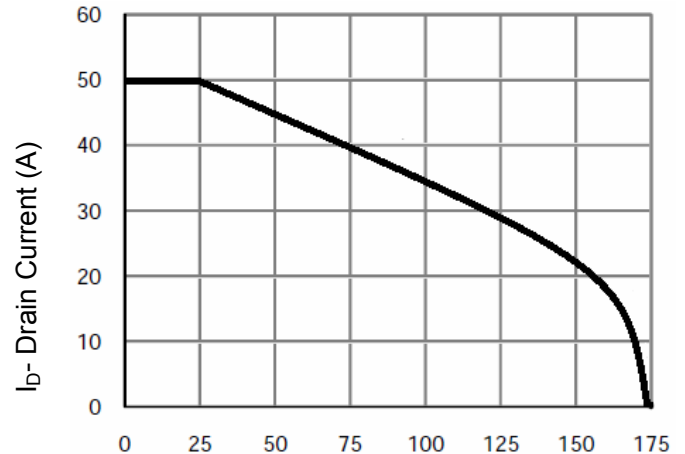
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



TJ-Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



TJ-Junction Temperature(°C)
Figure 10 ID Current- Junction Temperature

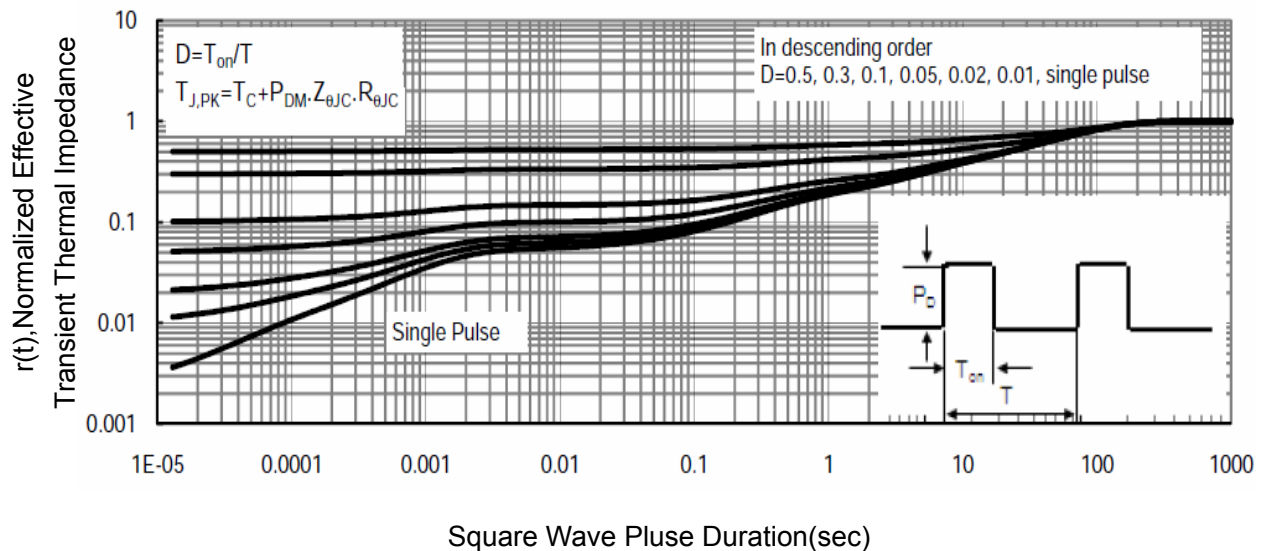
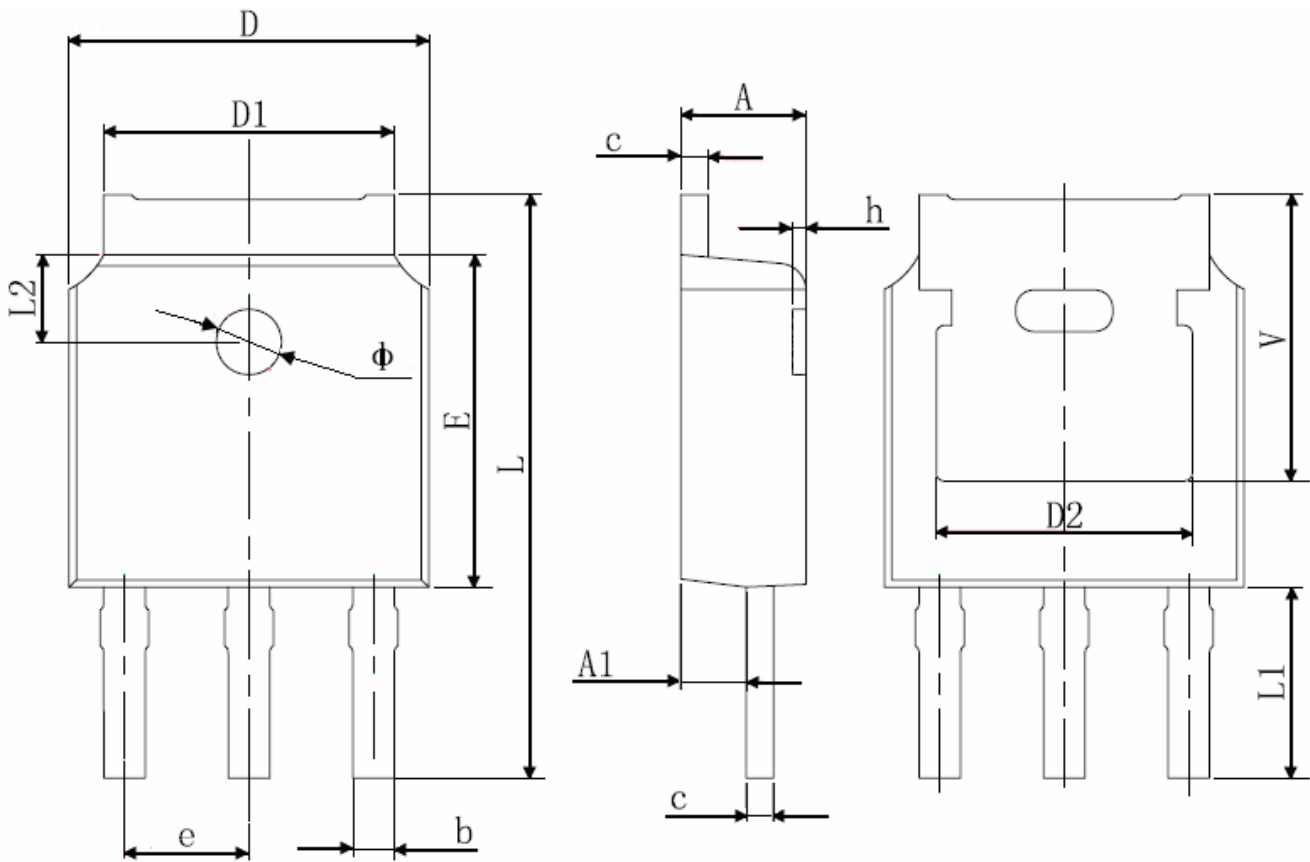


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-251S Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.860	1.160	0.034	0.046
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	10.400	11.000	0.409	0.433
L1	3.300	3.700	0.130	0.146
L2	1.600 REF.		0.063 REF.	
ϕ	1.100	1.300	0.043	0.051
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	