

Pb Free Product

Description

The RST0160G uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

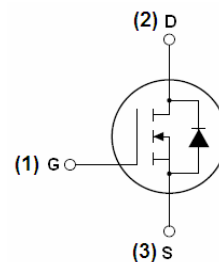
- $V_{DS} = 100V, I_D = 60A$
 $R_{DS(ON)} < 16m\Omega @ V_{GS}=12.6V$
- Special designed for converters and power controls
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

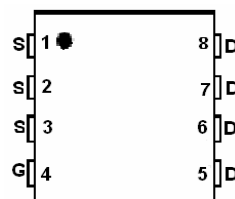
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



DFN5X6-8L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
RST0160G	RST0160G	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	60	A
Drain Current-Continuous($T_C=70^{\circ}C$)	$I_D (70^{\circ}C)$	50	A
Pulsed Drain Current	I_{DM}	80	A
Maximum Power Dissipation	P_D	105	W
Derating factor		0.70	W/ $^{\circ}C$
Single pulse avalanche energy (Note 5)	E_{AS}	550	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to- Case ^(Note 2)	$R_{\theta Jc}$	1.43	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

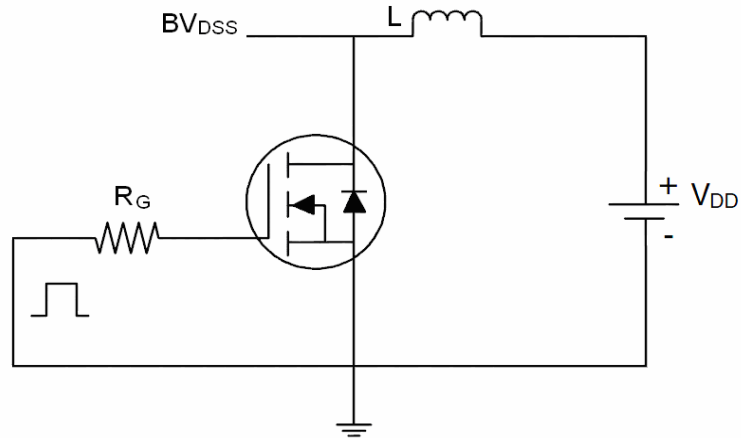
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	110	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5	3.7	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	12.6	16	mΩ
Forward Transconductance	g _{FS}	V _{DS} =15V, I _D =10A	-	30	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	2850	-	PF
Output Capacitance	C _{OSS}		-	220	-	PF
Reverse Transfer Capacitance	C _{rss}		-	90	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =5A, R _L =10Ω V _{GS} =10V, R _G =1Ω	-	17	-	nS
Turn-on Rise Time	t _r		-	10	-	nS
Turn-Off Delay Time	t _{d(off)}		-	26	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =10A, V _{GS} =10V	-	47	-	nC
Gate-Source Charge	Q _{gs}		-	13	--	nC
Gate-Drain Charge	Q _{gd}		-	12.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =4A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	60	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 10A di/dt = 100A/μs ^(Note3)	-	-	60	nS
Reverse Recovery Charge	Q _{rr}		-	-	200	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

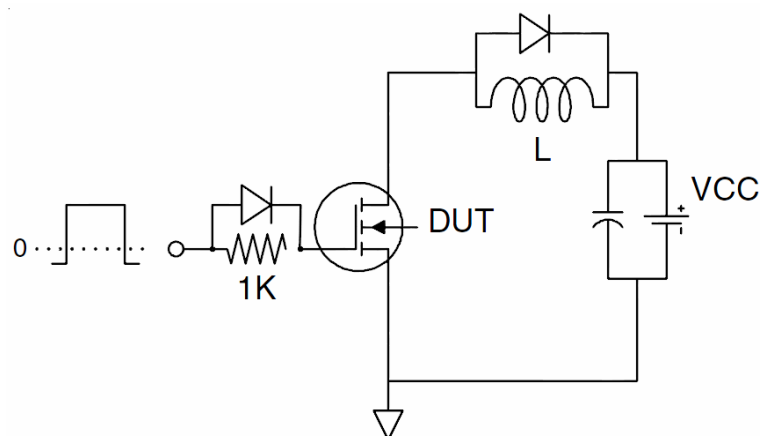
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25\Omega$

Test Circuit

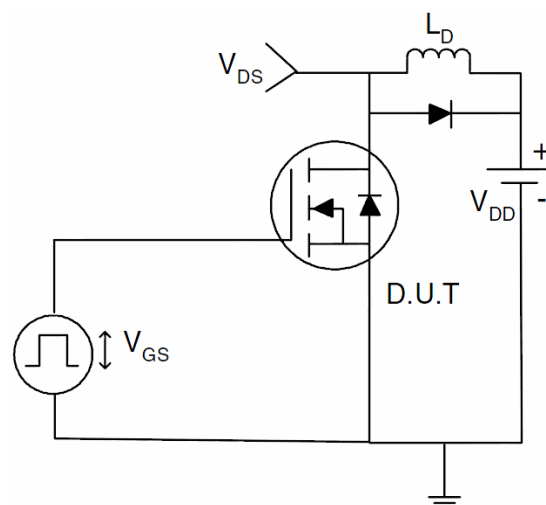
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

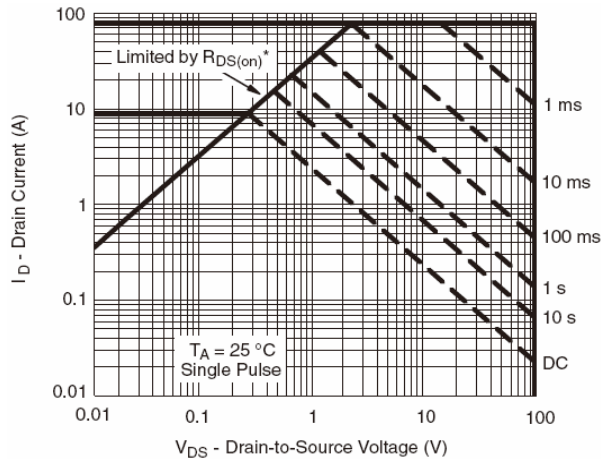
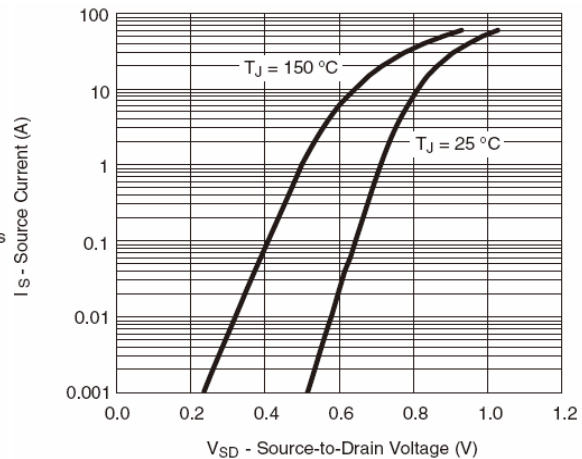
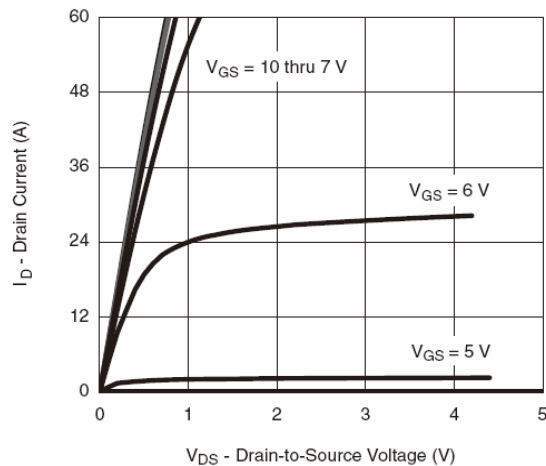
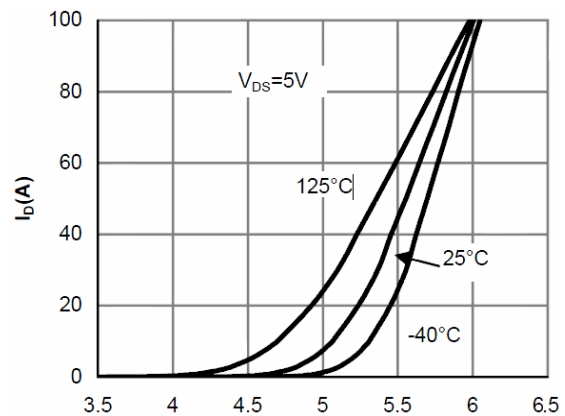
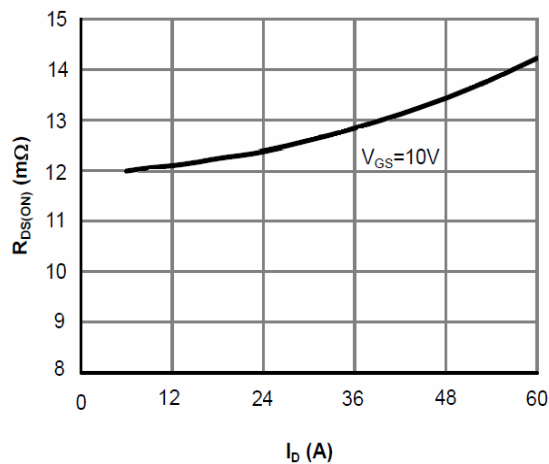
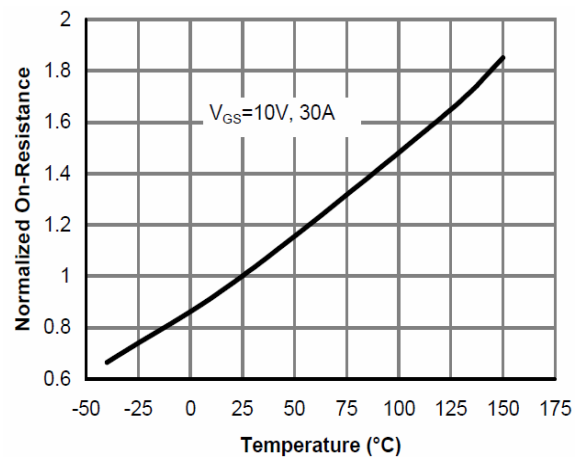
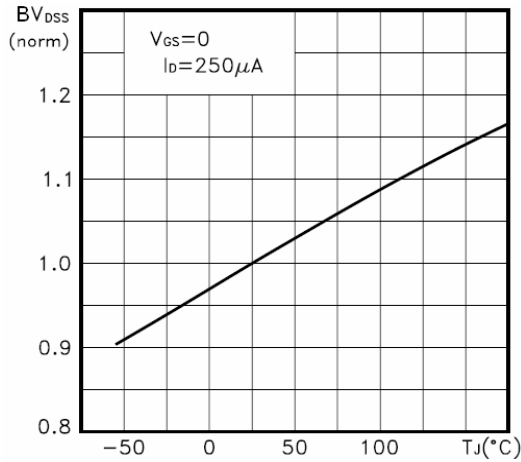
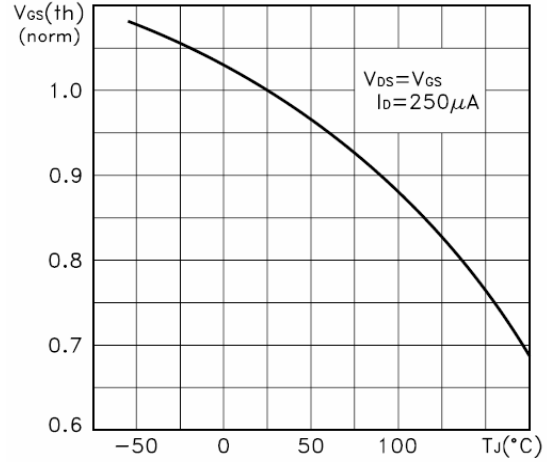
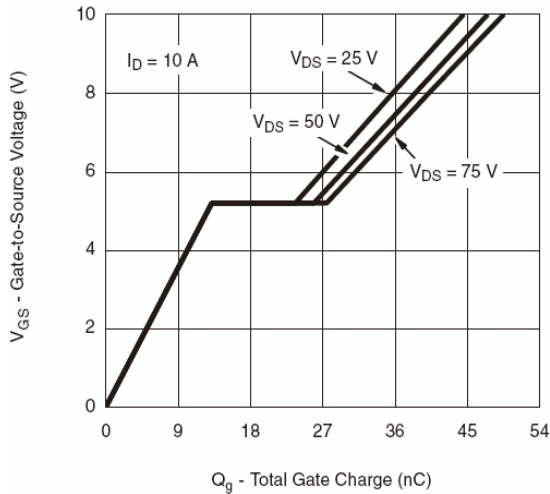
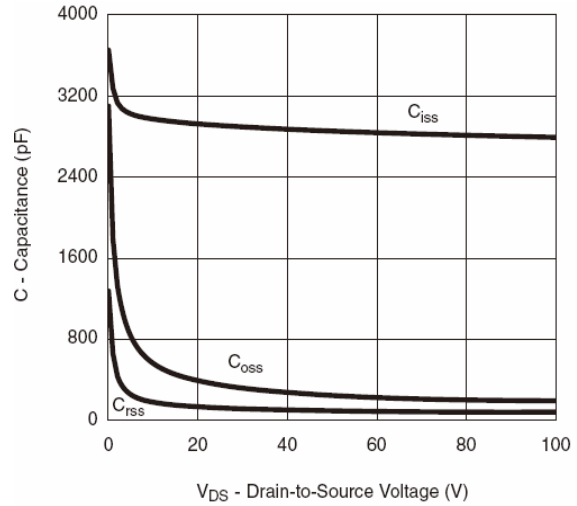
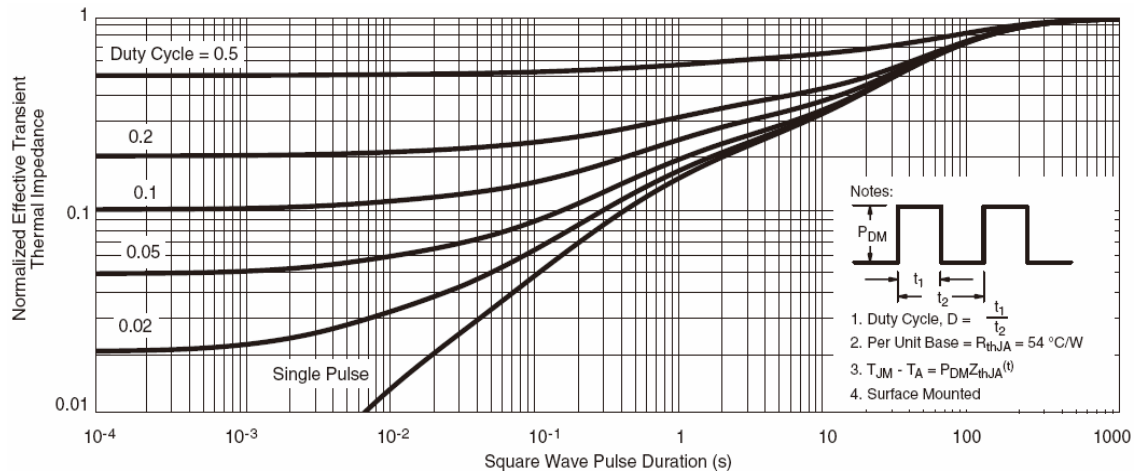
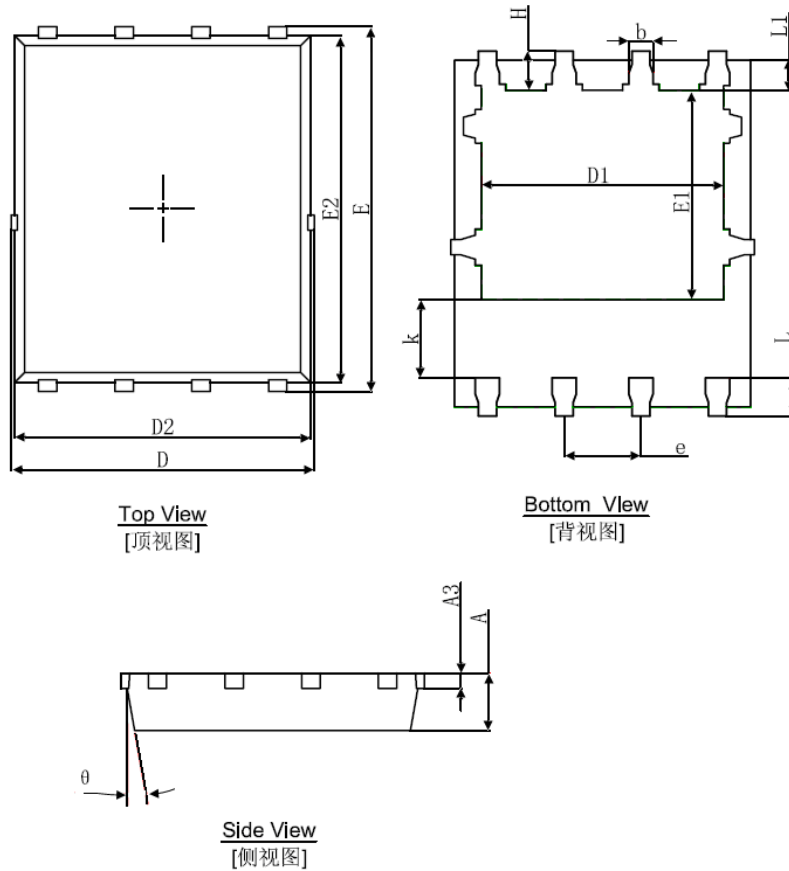
Figure1. Safe operating area

Figure2. Source-Drain Diode Forward Voltage

Figure3. Output characteristics

Figure4. Transfer characteristics

Figure5. Static drain-source on resistance

Figure6. $R_{DS(ON)}$ vs Junction Temperature


Figure7. BV_{DSS} vs Junction Temperature

Figure8. $V_{GS(th)}$ vs Junction Temperature

Figure9. Gate charge waveforms

Figure10. Capacitance

Figure11. Normalized Maximum Transient Thermal Impedance


DFN5X6-8L Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
K	1.190	1.390	0.047	0.055
b	0.035	0.450	0.014	0.018
e	1.270(TYP.)		0.050(TYP.)	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°