

Description

The RST0130GA uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!
100% ΔV_{ds} TESTED!

General Features

- $V_{DS} = 100V, I_D = 30A$
 $R_{DS(ON)} < 32m\Omega @ V_{GS}=10V$ (Typ:25m Ω)
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=4.5V$ (Typ:28m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

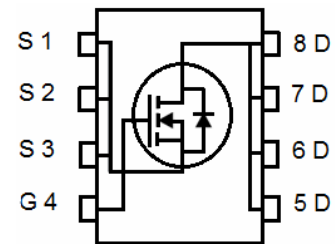
DFN 5X6



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
RST0130GA	RST0130GA	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	30	A
$I_D (100^\circ\text{C})$	Drain Current-Continuous($T_C=100^\circ\text{C}$)	21	A
I_{DM}	Pulsed Drain Current	120	A
P_D	Maximum Power Dissipation	85	W
	Derating factor	0.68	W/ $^\circ\text{C}$
E_{AS}	Single pulse avalanche energy ^(Note 5)	200	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ^(Note 2)	1.5	$^\circ\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

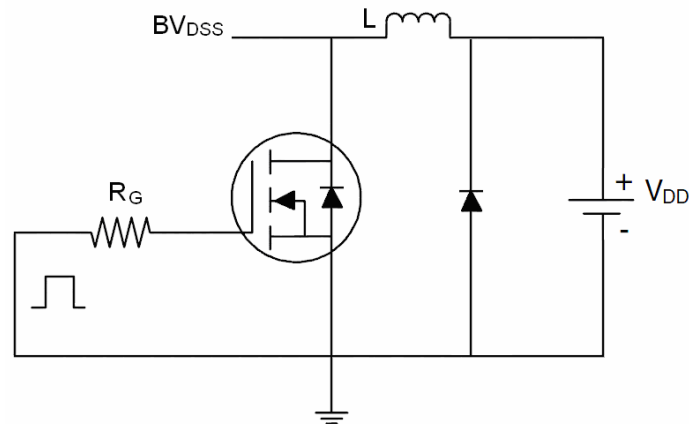
Symbol		Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage		V _{GS} =0V I _D =250μA	100	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current		V _{DS} =100V, V _{GS} =0V	-	-	1	μA
I _{GSS}	Gate-Body Leakage Current		V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)							
V _{GS(th)}	Gate Threshold Voltage		V _{DS} =V _{GS} , I _D =250μA	1.3	1.9	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =15A	-	25	32	mΩ	
		V _{GS} =4.5V, I _D =15A		28	35		
g _{FS}	Forward Transconductance		V _{DS} =5V, I _D =15A	-	15	-	S
Dynamic Characteristics ^(Note4)							
C _{iss}	Input Capacitance		V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	2479	-	PF
C _{Oss}	Output Capacitance			-	96	-	PF
C _{rss}	Reverse Transfer Capacitance			-	79	-	PF
Switching Characteristics ^(Note 4)							
t _{d(on)}	Turn-on Delay Time		V _{DD} =50V, R _L =3.3Ω V _{GS} =10V, R _{GEN} =3Ω	-	9	-	nS
t _r	Turn-on Rise Time			-	9	-	nS
t _{d(off)}	Turn-Off Delay Time			-	32	-	nS
t _f	Turn-Off Fall Time			-	8	-	nS
Q _g	Total Gate Charge		V _{DS} =50V, I _D =15A, V _{GS} =10V	-	67.2	-	nC
Q _{gs}	Gate-Source Charge			-	9.4	-	nC
Q _{gd}	Gate-Drain Charge			-	15.5	-	nC
Drain-Source Diode Characteristics							
V _{SD}	Diode Forward Voltage ^(Note 3)		V _{GS} =0V, I _S =15A	-	-	1.2	V
I _S	Diode Forward Current ^(Note 2)		-	-	-	30	A
t _{rr}	Reverse Recovery Time		TJ = 25°C, IF = 15A	-	32	-	nS
Q _{rr}	Reverse Recovery Charge		di/dt = 100A/μs ^(Note3)	-	53	-	nC
t _{on}	Forward Turn-On Time		Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

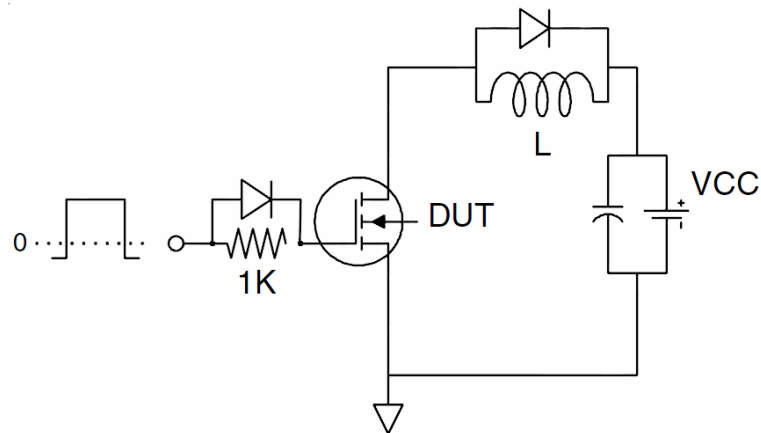
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS Condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$,

Test Circuit

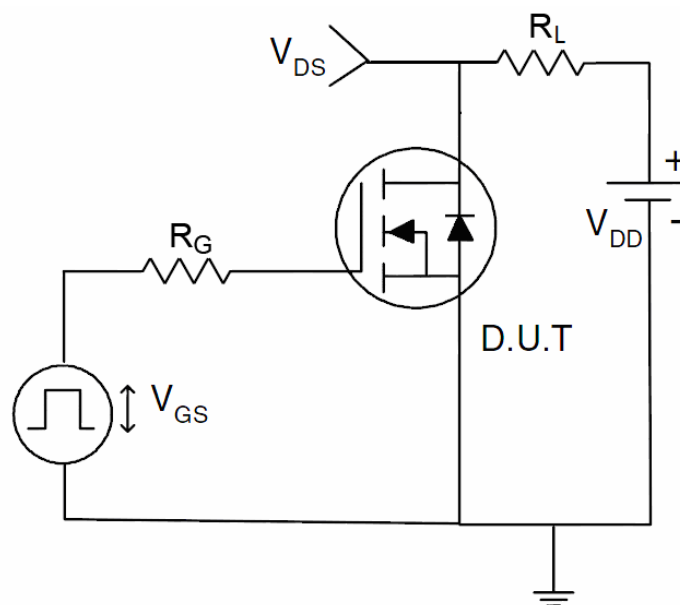
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

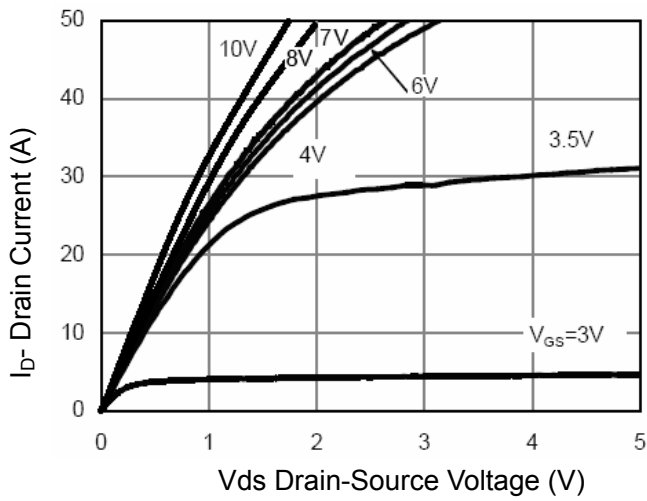


Figure 1 Output Characteristics

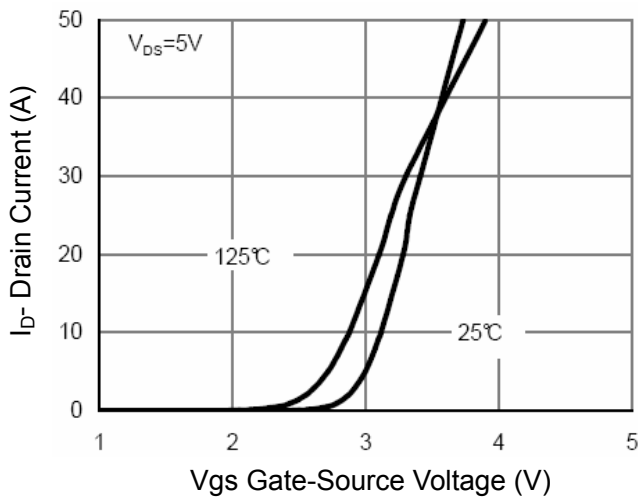


Figure 2 Transfer Characteristics

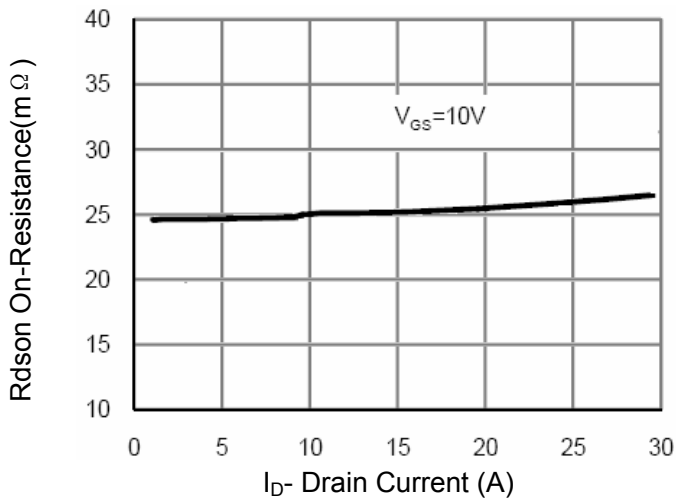


Figure 3 $R_{DS(on)}$ - Drain Current

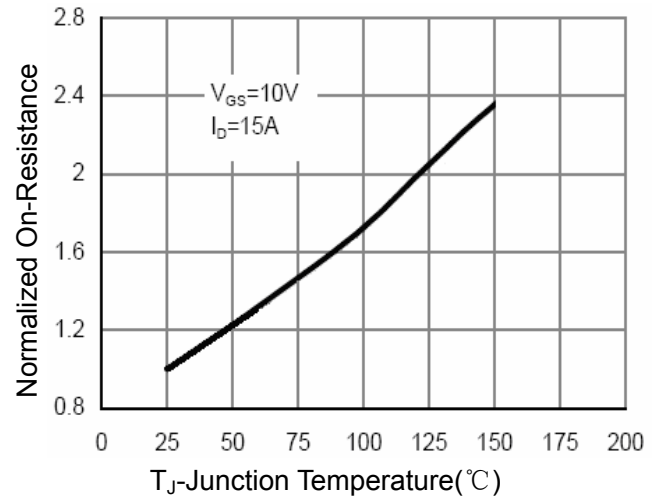


Figure 4 $R_{DS(on)}$ -Junction Temperature

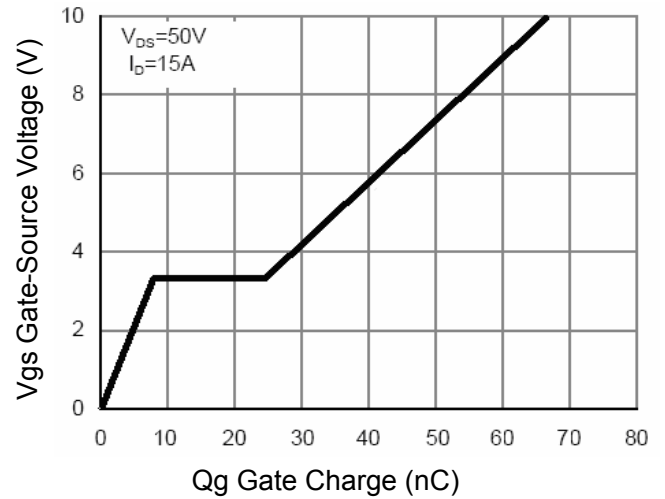


Figure 5 Gate Charge

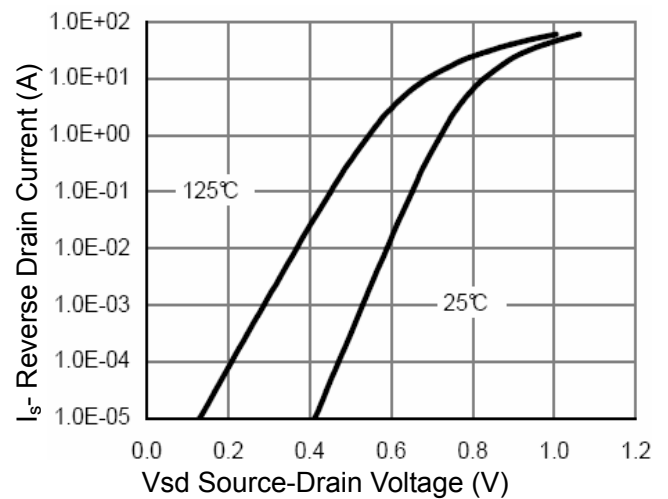


Figure 6 Source- Drain Diode Forward

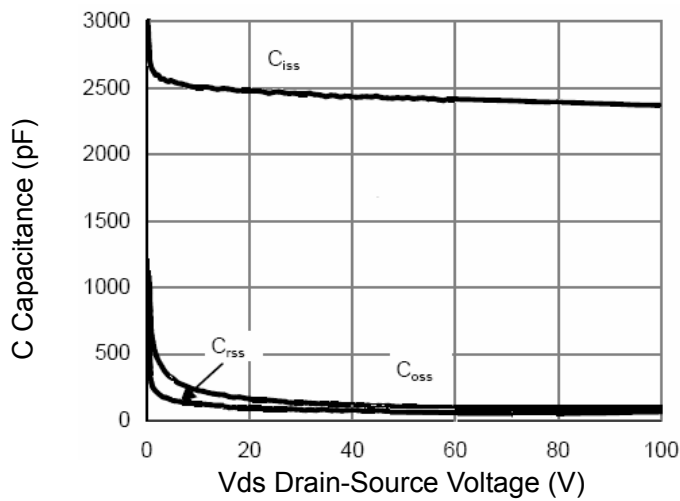


Figure 7 Capacitance vs Vds

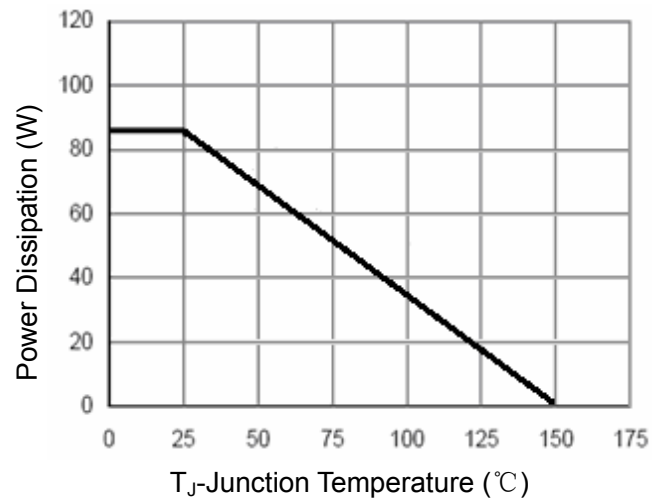


Figure 9 Power De-rating

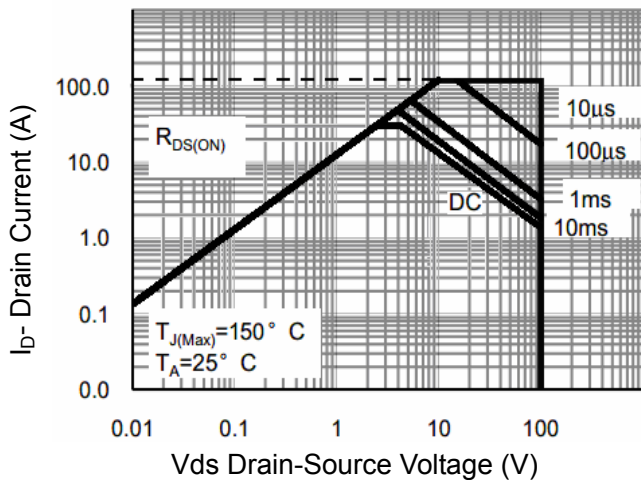


Figure 8 Safe Operation Area

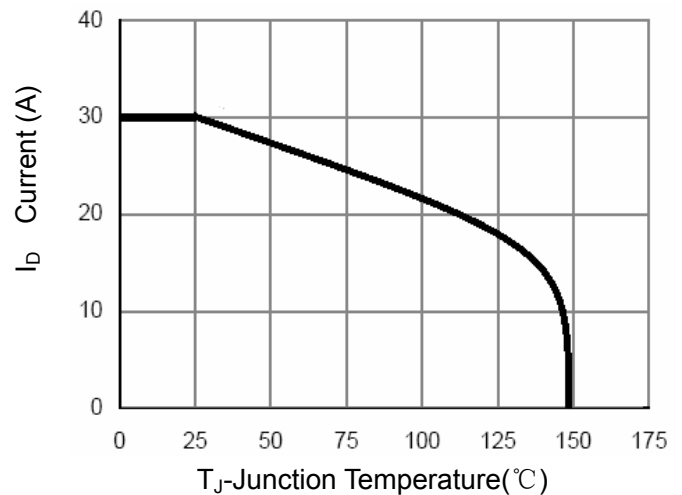


Figure 10 ID Current- Junction Temperature

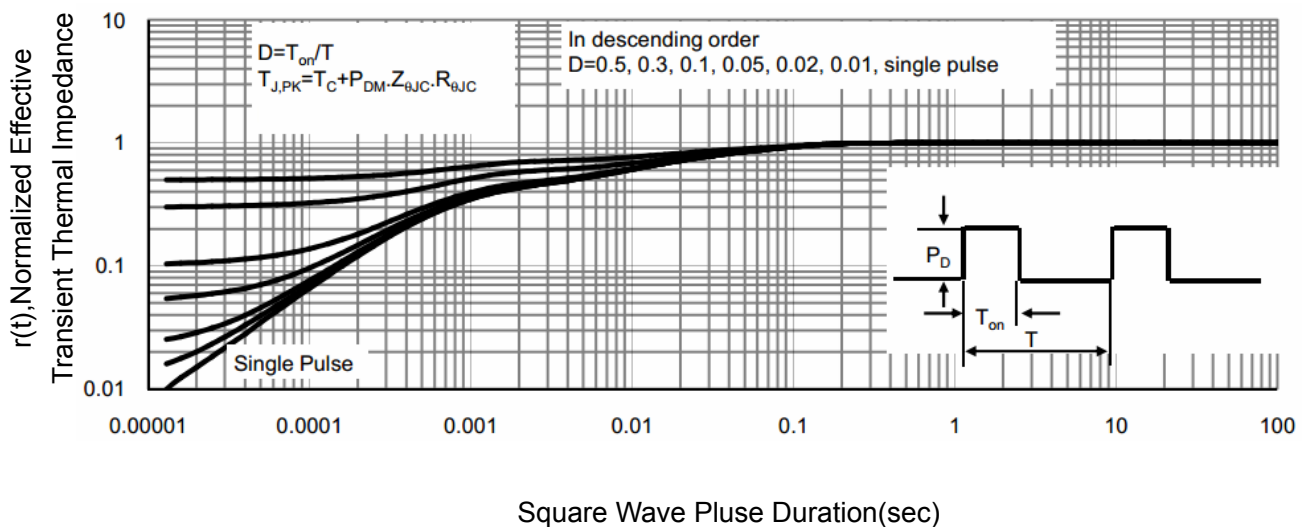
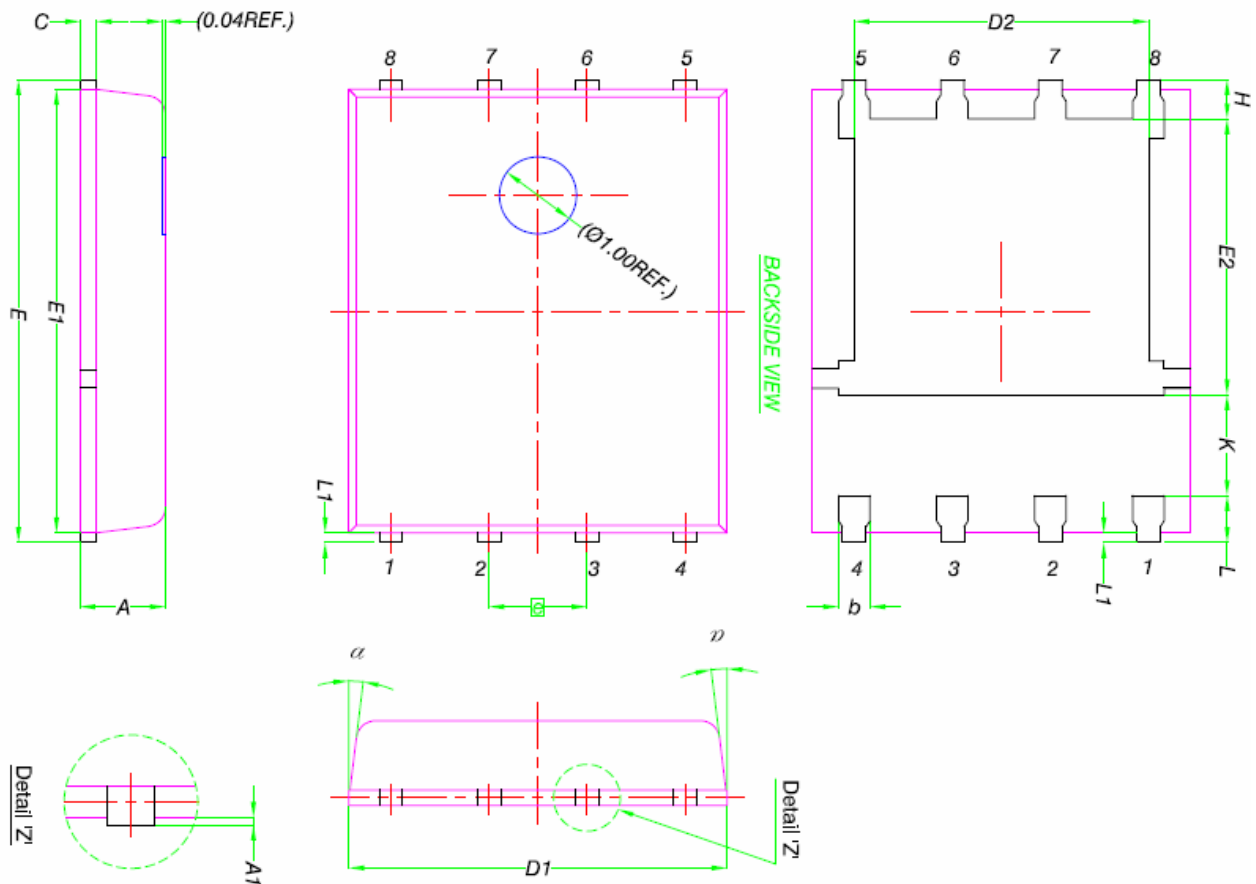


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information


DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

