

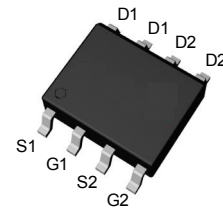
Features

- -30V/-6.5A ,
 $R_{DS(ON)} = 36m\Omega (typ.) @ V_{GS} = -10V$
 $R_{DS(ON)} = 50m\Omega (typ.) @ V_{GS} = -4.5V$
- Reliable and Rugged
- Lead Free and Green Device Available
(RoHS Compliant)

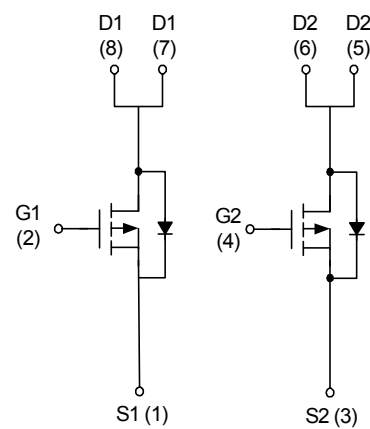
Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems

Pin Description



Top View of SOP8



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 25	
I_D^*	Continuous Drain Current	$V_{GS} = -10\text{V}$ -6.5	A
I_{DM}^*	Pulsed Drain Current		
I_S^*	Diode Continuous Forward Current	-2	A
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	
P_D^*	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$ 2	W
		$T_A = 100^\circ\text{C}$ 0.8	
$R_{\theta JA}^*$	Thermal Resistance-Junction to Ambient	62.5	$^\circ\text{C/W}$

Note:

*Surface Mounted on 1in^2 pad area, $t \leq 10\text{sec}$.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition				Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V	-	-	-1	μA
		T _J =85°C	-	-	-30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	-1	-1.5	-2.3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-6.5A	-	36	45	mΩ
		V _{GS} =-4.5V, I _{DS} =-5.6A	-	50	65	
V _{SD} ^a	Diode Forward Voltage	I _{SD} =-1.7A, V _{GS} =0V	-	-0.8	-1.3	V
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _{DS} =-4.9A	-	11.6	16	nC
Q _{gs}	Gate-Source Charge		-	1.3	-	
Q _{gd}	Gate-Drain Charge		-	2.5	-	

Electrical Characteristics (Cont.) ($T_A = 25^\circ\text{C}$ unless otherwise noted)

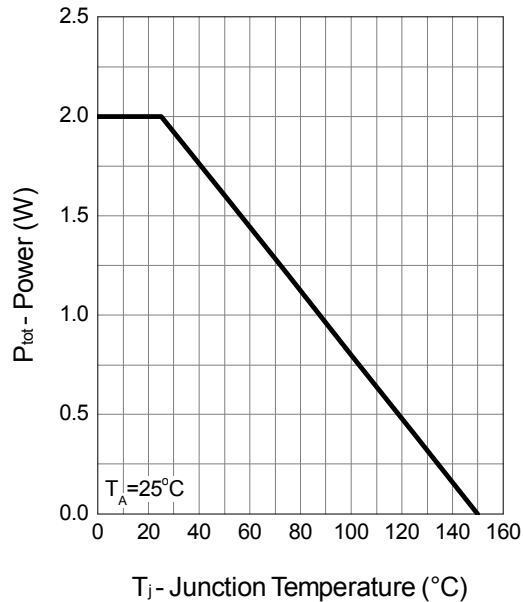
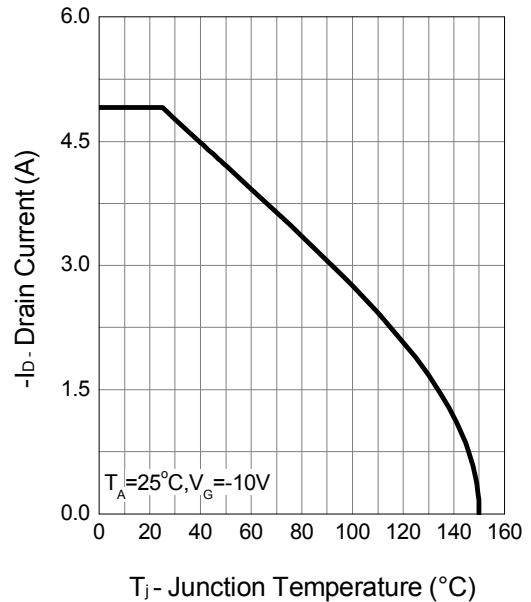
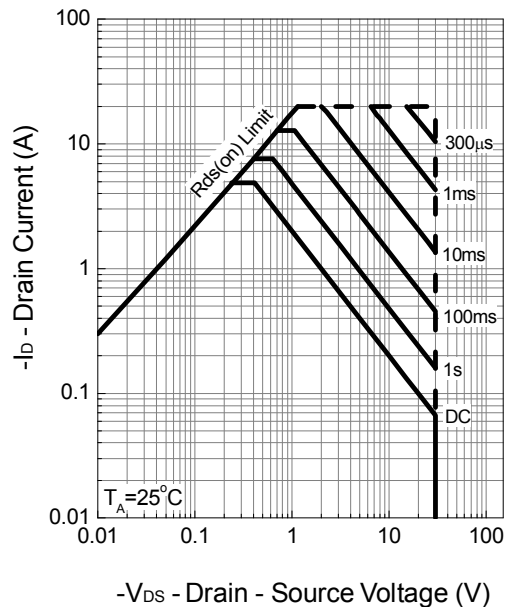
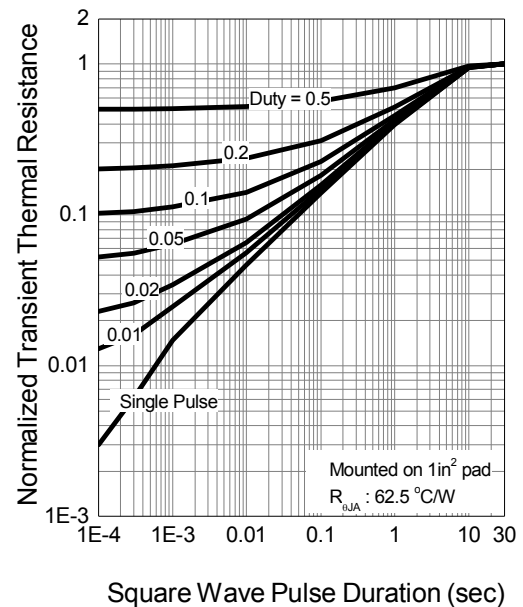
Symbol	Parameter	Test Condition				Unit
			Min.	Typ.	Max.	
Dynamic Characteristics ^b						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	-	8	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, Frequency=1.0MHz	-	625	-	pF
C _{oss}	Output Capacitance		-	100	-	
C _{rss}	Reverse Transfer Capacitance		-	60	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =-15V, R _L =15Ω, I _{DS} =-1A, V _{GEN} =-10V, R _G =6Ω	-	6	12	ns
t _r	Turn-on Rise Time		-	12	23	
t _{d(OFF)}	Turn-off Delay Time		-	25	46	
t _f	Turn-off Fall Time		-	6	12	
t _{rr}	Reverse Recovery Time	I _{DS} =-4.9A,	-	14	-	ns
Q _{rr}	Reverse Recovery Charge	di _{SD} /dt=100A/μs	-	5	-	nC

Notes:

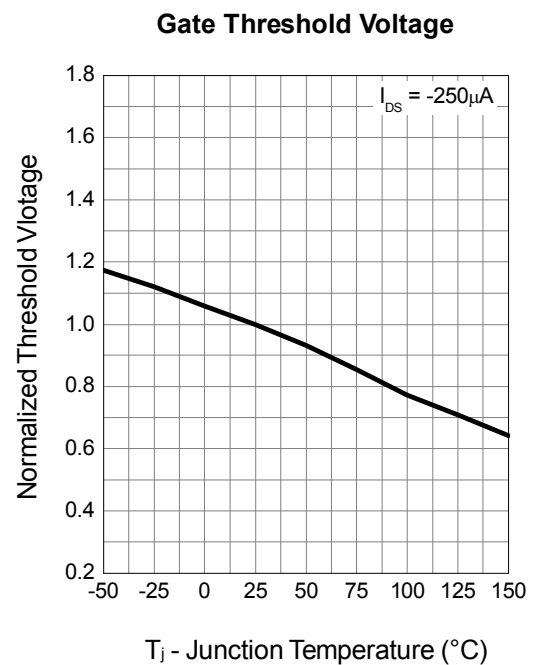
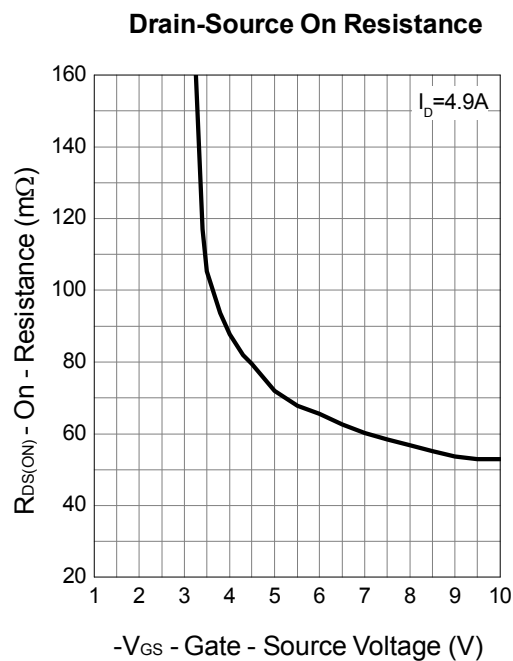
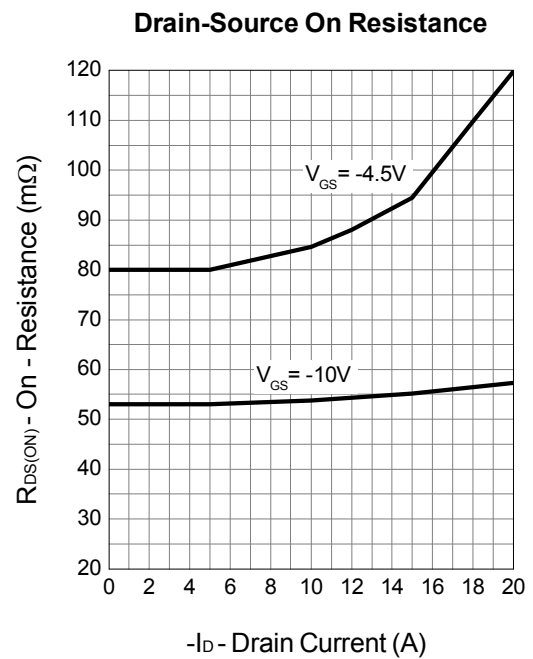
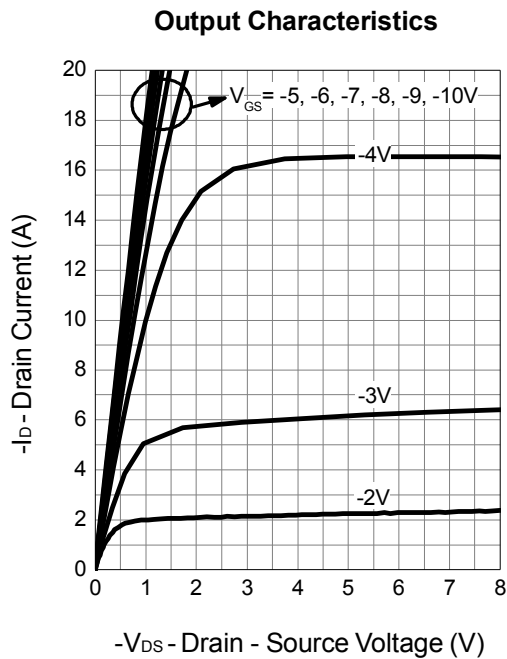
a : Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

b : Guaranteed by design, not subject to production testing.

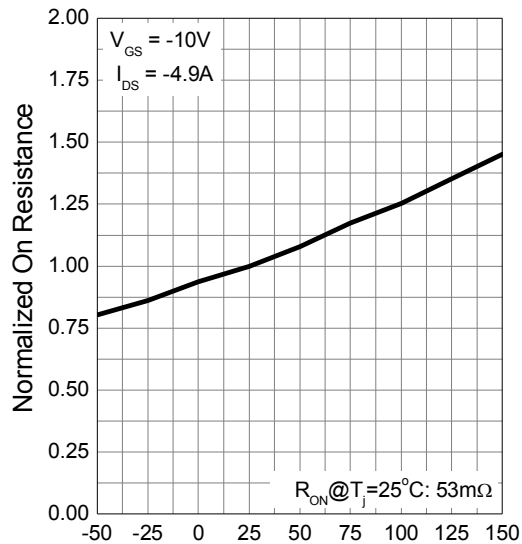
Typical Characteristics

Power Dissipation

Drain Current

Safe Operation Area

Thermal Transient Impedance


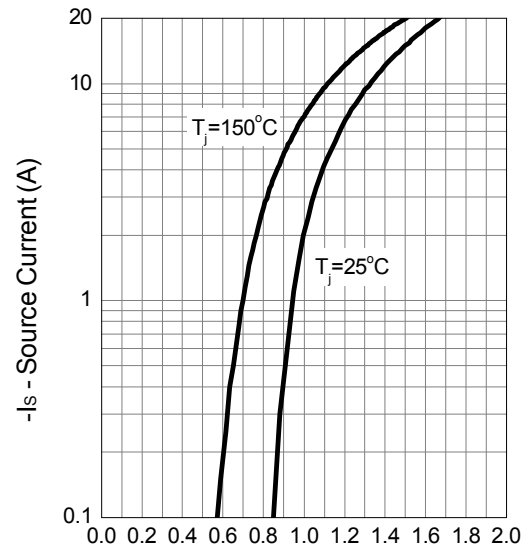
Typical Characteristics (Cont.)



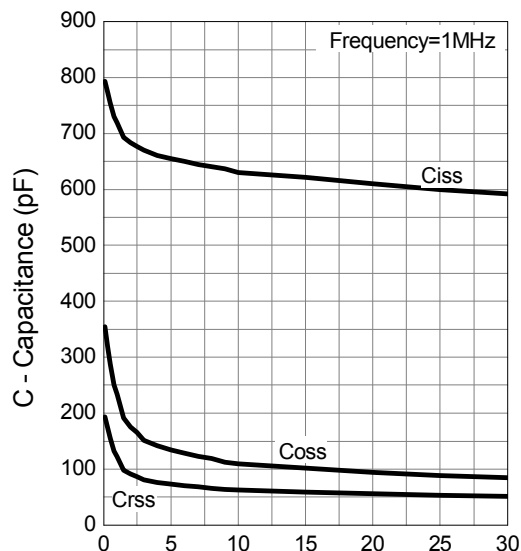
Typical Characteristics (Cont.)

Drain-Source On Resistance


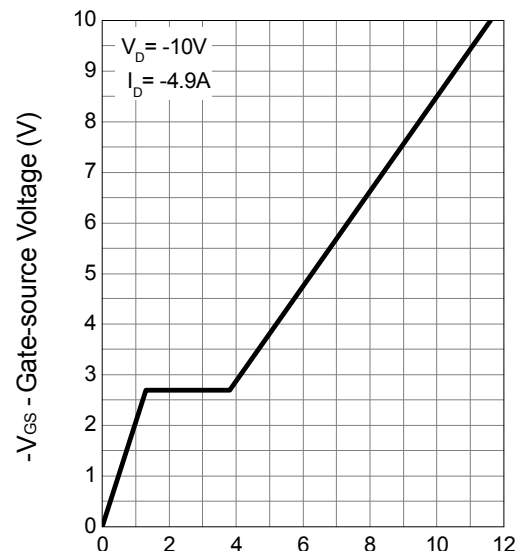
T_J - Junction Temperature ($^{\circ}\text{C}$)

Source-Drain Diode Forward


$-V_{SD}$ - Source-Drain Voltage (V)

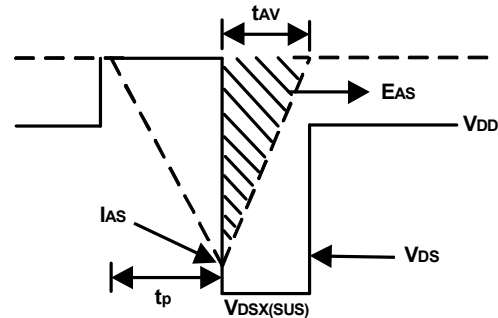
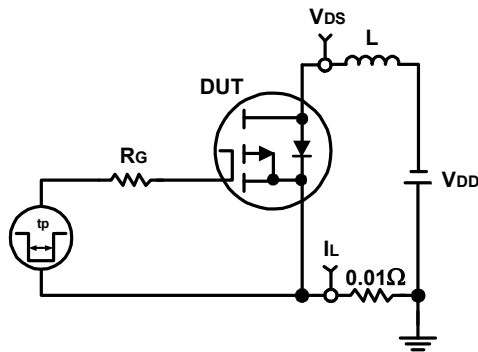
Capacitance


$-V_{DS}$ - Drain-Source Voltage (V)

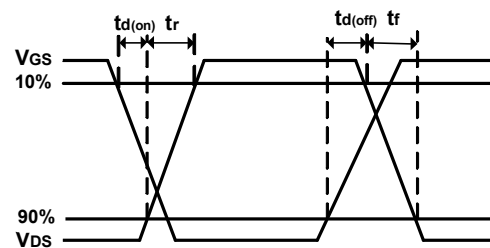
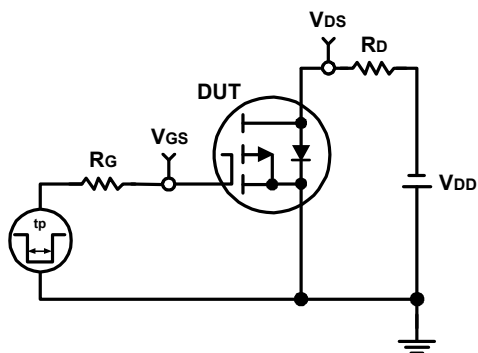
Gate Charge


Q_G - Gate Charge (nC)

Avalanche Test Circuit and Waveforms

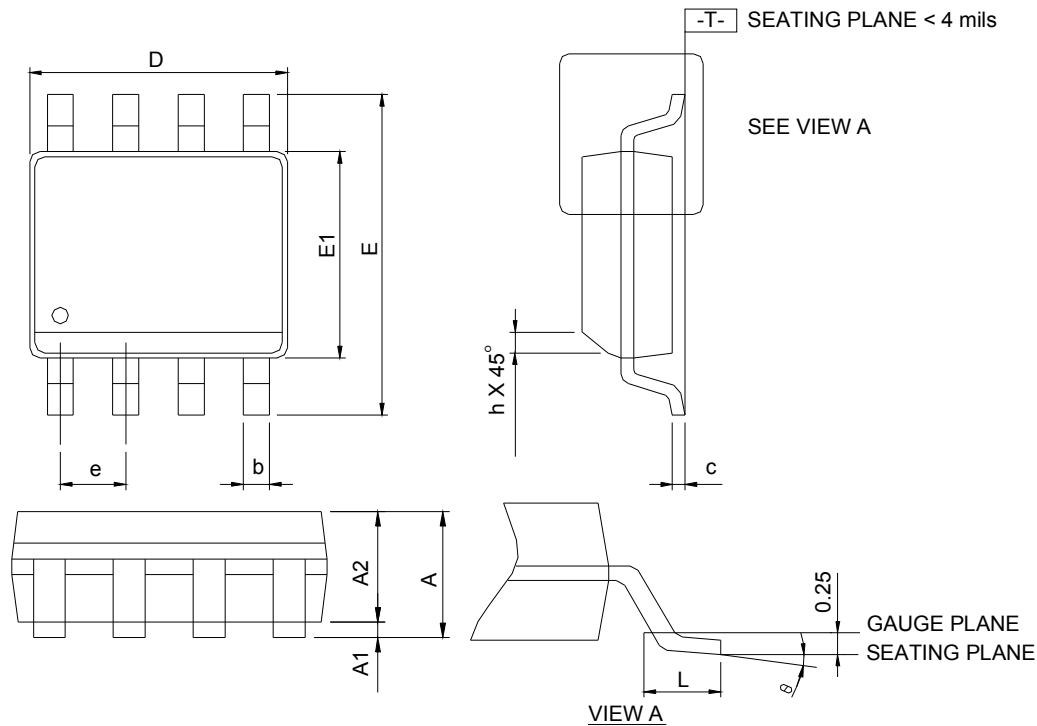


Switching Time Test Circuit and Waveforms



Package Information

SOP8



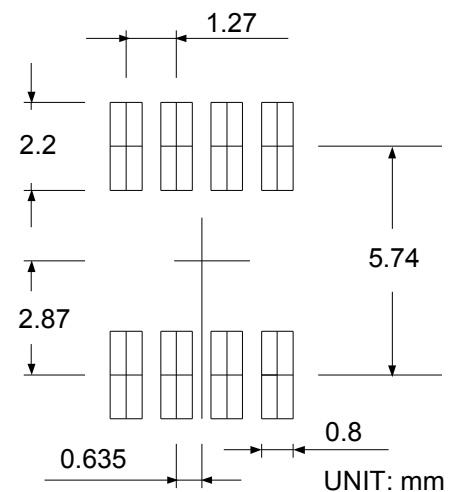
DIMENSIONS	SOP8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN



UNIT: mm