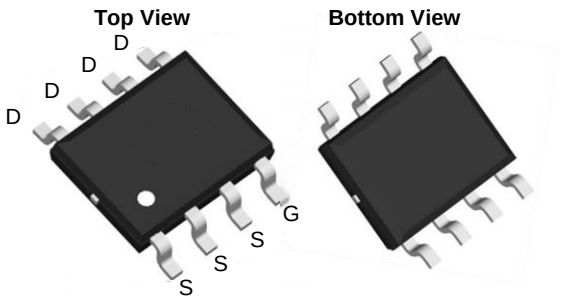
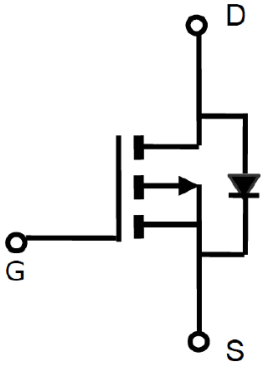
- -30V/-15A
- $R_{DS(ON)}$=5.5mΩ (typ) @VGS=10V
  $R_{DS(ON)}$=9mΩ (typ) @VGS=4.5V
- 100% UIS & RG Tested
- Reliableand Rugged
- Lead Freeand Green Devices Available (RoHS Compliant)

SOP-8



Applic

- PowerManagementforIndustrialDC/DC Converters



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Absolute Maximum Ratings (T_A= 25°C unless otherwise noted)

Symbol	Parameter		Maximum	Units
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±25	V
I_D	Continuous Drain Current	T_A=25°C	-16	A
		T_A=70°C	-12.5	
I_{DM}	Pulsed Drain Current [C]		-64	
I_{AS}	Avalanche Current [C]		39	A
E_{AS}	Avalanche energy [C] L=0.1mH		76	mJ
P_D	Power Dissipation [B]	T_A=25°C	3.1	W
		T_A=70°C	2.0	
T_J, T_{STG}	Junction and Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter		Typ	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient [A]	t ≤ 10s	31	40	°C/W
	Maximum Junction-to-Ambient [A D]	Steady-State	59	75	°C/W
$R_{\theta JL}$	Maximum Junction-to-Lead	Steady-State	16	24	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
advanced	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±25V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=-250μA	-1	-1.8	-2.7	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-15A		5.5	7.2	mΩ
		T_J=125°C		7.6	10.5	
		V_{GS}=-4.5V, I_D=-10A		9	12	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-16A		50		S
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		3560		pF
C_{oss}	Output Capacitance			635		pF
C_{rss}	Reverse Transfer Capacitance			645		pF
R_g	Gate resistance	f=1MHz		8		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-16A		50	70	nC
Q_g(4.5V)	Total Gate Charge			25	35	nC
Q_{gs}	Gate Source Charge			9		nC
Q_{gd}	Gate Drain Charge			12		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=0.95Ω, R_{GEN}=3Ω		12		ns
t_r	Turn-On Rise Time			12.5		ns
$t_{D(off)}$	Turn-Off DelayTime			135		ns
t_f	Turn-Off Fall Time			63		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-16A, di/dt=500A/μs		32		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-16A, di/dt=500A/μs		62		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

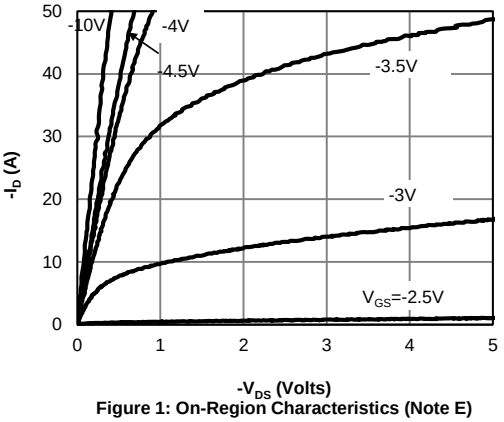


Figure 1: On-Region Characteristics (Note E)

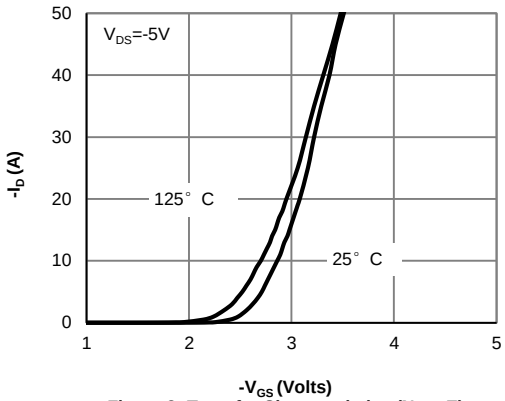


Figure 2: Transfer Characteristics (Note E)

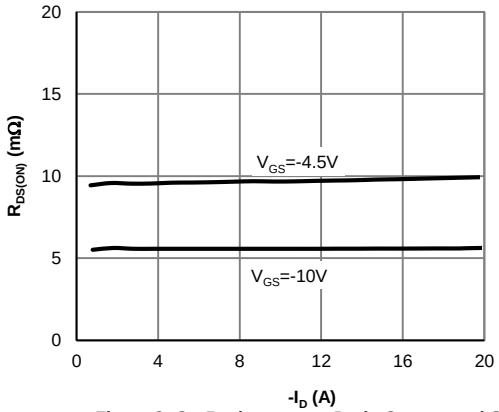


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

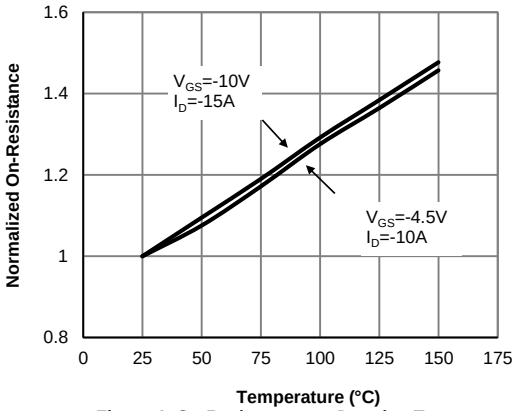


Figure 4: On-Resistance vs. Junction Temperature (Note E)

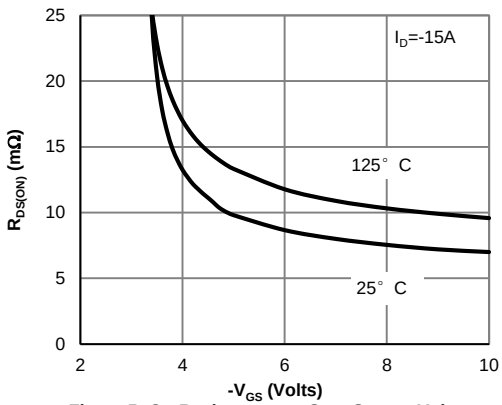


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

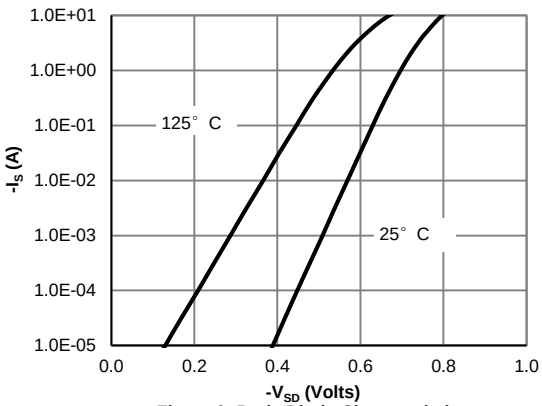


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

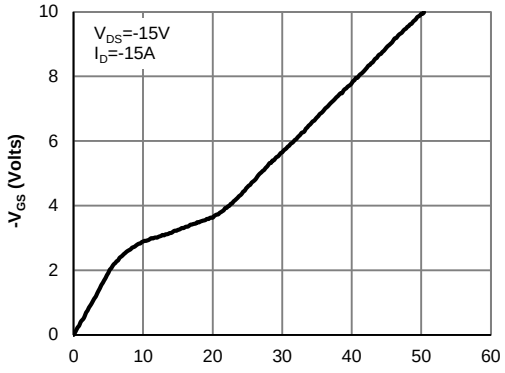


Figure 7: Gate-Charge Characteristics

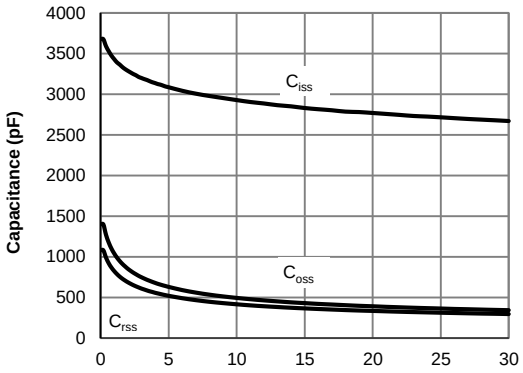
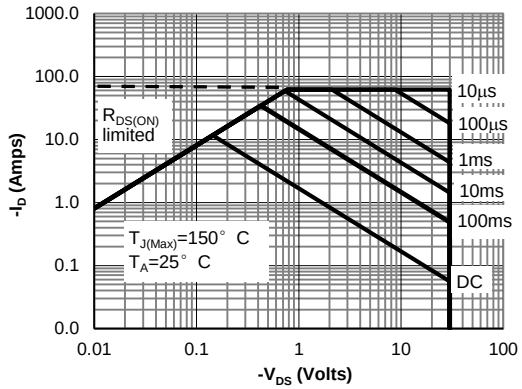


Figure 8: Capacitance Characteristics



V_{GS}> or equal to -4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

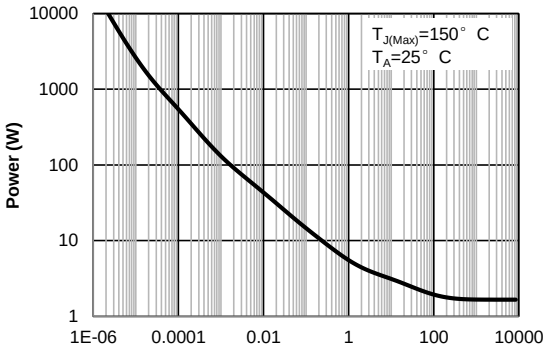


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

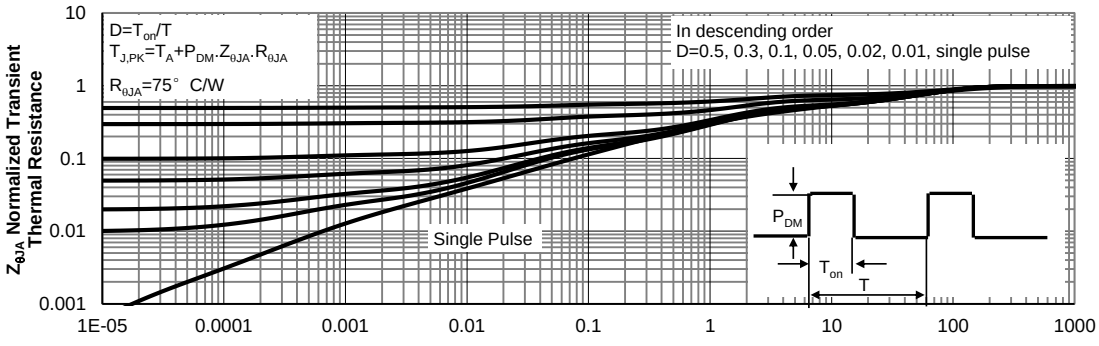
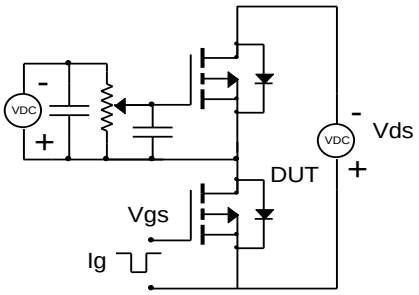
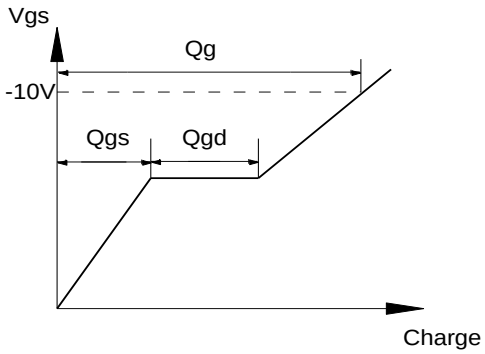


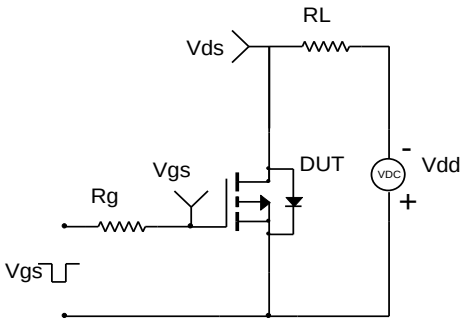
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

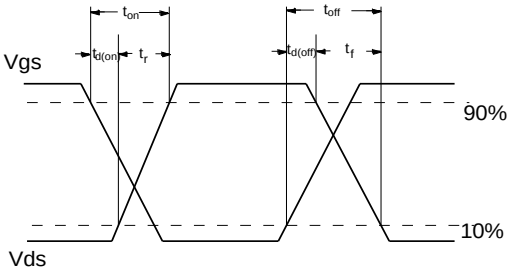
Gate Charge Test Circuit & Waveform



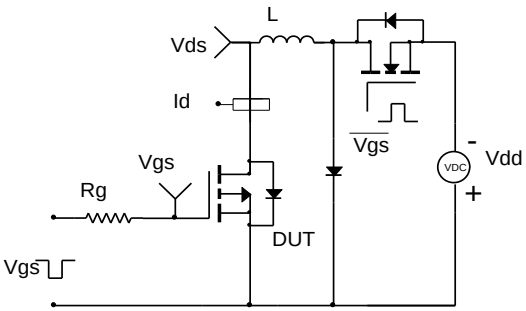


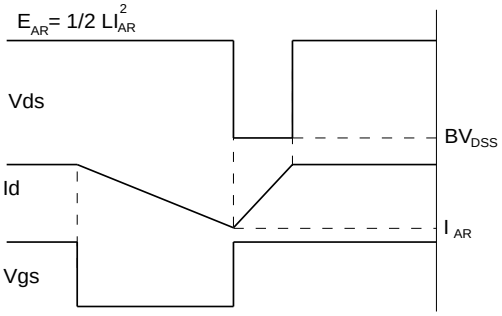
Resistive Switching Test Circuit & Waveforms



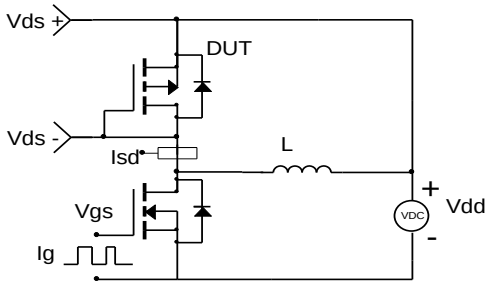


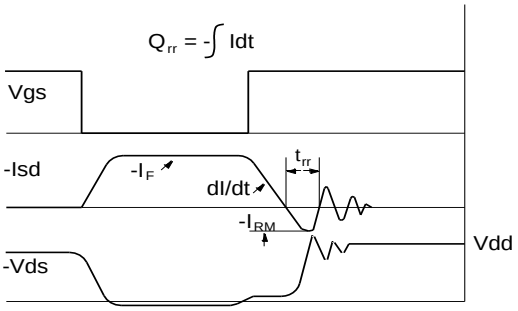
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



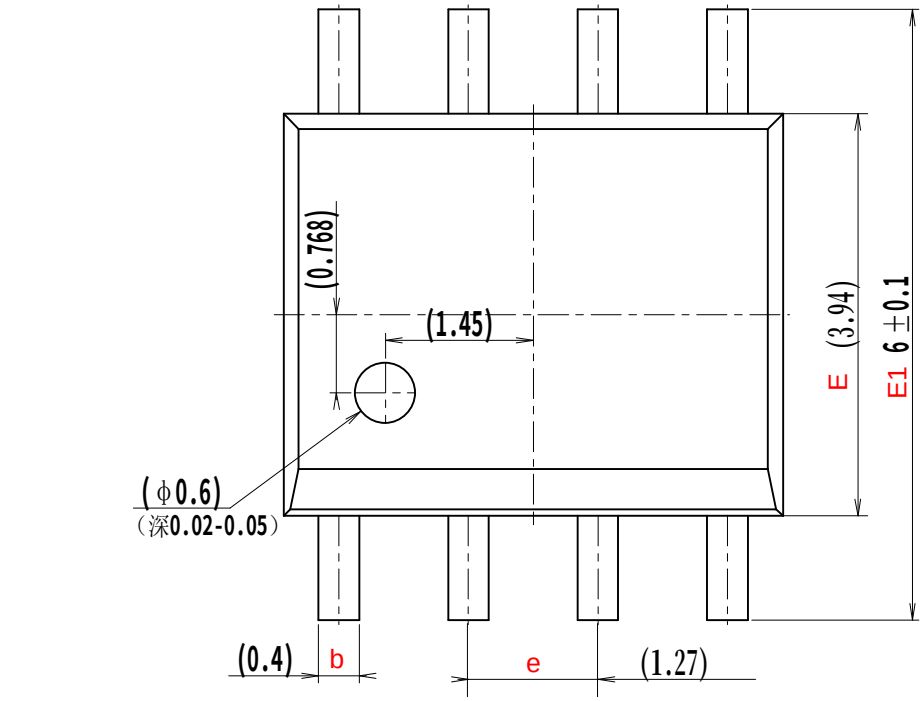


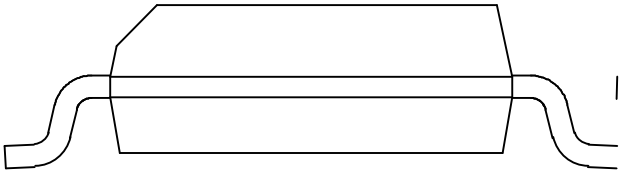
Diode Recovery Test Circuit & Waveforms

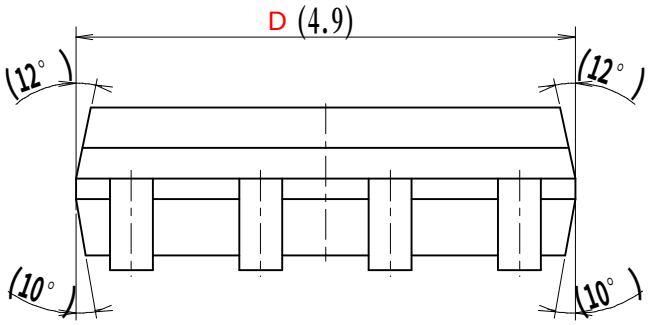




SOP8 PACKAGE OUTLINE DIMENSIONS







字符	Dimension millimeters		
	Min	Standard	Max
A	1.500	1.600	1.700
A1	0.050		
A2	1.350	1.450	1.550
b	0.300	0.400	0.500
c	0.220	0.254	0.280
D	4.800	4.900	5.000
E	3.840	3.940	4.040
E1	5.900	6.000	6.100
e		1.27 (BSC)	
L	0.520	0.620	0.720
θ	0°		8°