

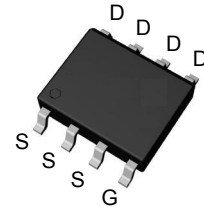
Features

- 30V/9A,
 $R_{DS(ON)} = 15m\Omega(\text{typ.}) @ V_{GS} = 10V$
 $R_{DS(ON)} = 19m\Omega(\text{typ.}) @ V_{GS} = 4.5V$
- Reliable and Rugged
- Lead Free and Green Devices Available
(RoHS Compliant)
- 100% UIS Tested

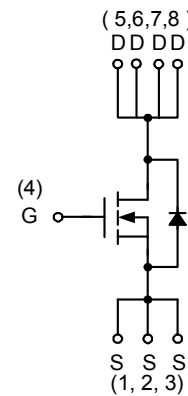
Applications

- Power Management in Notebook Computer,
Portable Equipment and Battery Powered
Systems.

Pin Description



Top View of SOP8



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter		Rating	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	
I_D^a	Continuous Drain Current ($V_{GS}=10V$)	$T_A=25^\circ\text{C}$	9	A
		$T_A=70^\circ\text{C}$	6.4	
I_{DM}^a	300 μs Pulsed Drain Current ($V_{GS}=10V$)		32	
I_S^a	Diode Continuous Forward Current		1	
I_{AS}^b	Avalanche Current (Single Pulse)		7	mJ
E_{AS}^b	Avalanche Energy, Single Pulse ($L=0.5mH$)		12.25	
T_J	Maximum Junction Temperature		150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-55 to 150	
P_D^a	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	1.92	W
		$T_A=70^\circ\text{C}$	1.23	
$R_{\theta JA}^a$	Thermal Resistance-Junction to Ambient	$t \leq 10s$	38	$^\circ\text{C/W}$
		Steady State	65	
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	Steady State	25	

Note a : Surface Mounted on 1in² pad area, $t \leq 10\text{sec}$.

Note b : UIS tested and pulse width limited by maximum junction temperature 150 $^\circ\text{C}$ (initial temperature $T_J=25^\circ\text{C}$).

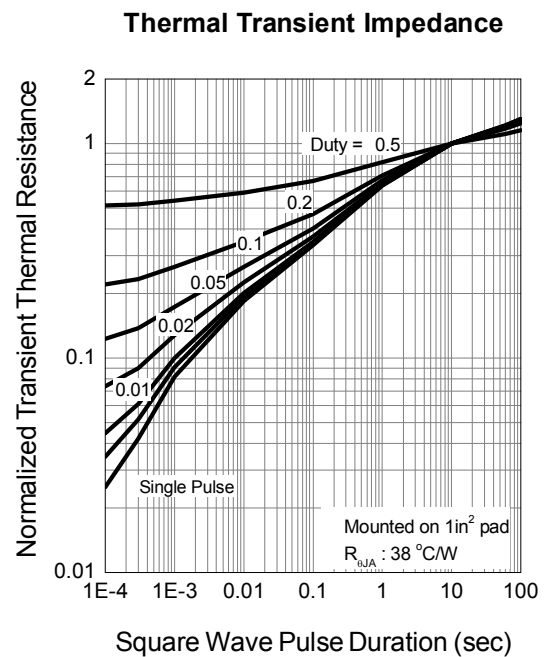
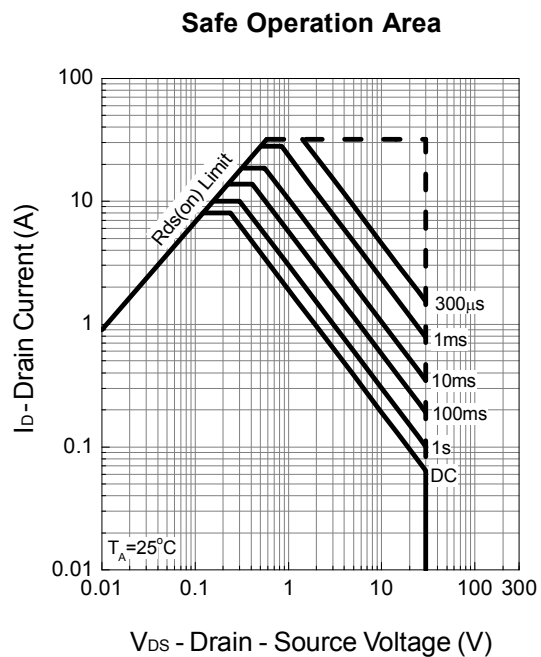
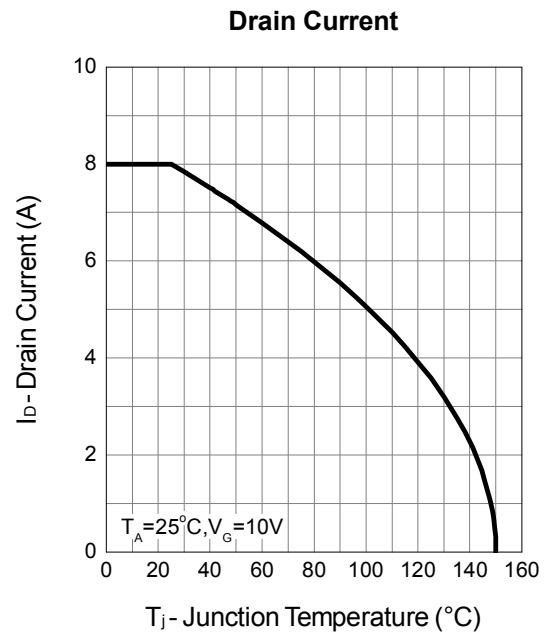
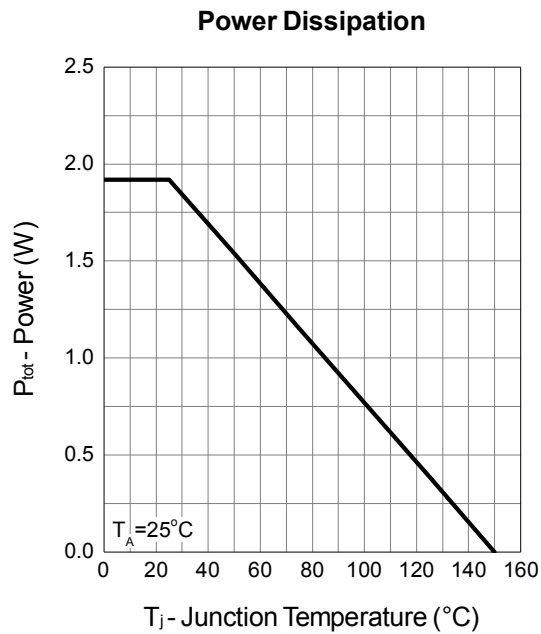
Electrical Characteristics (Cont.) ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions				Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1.3	1.8	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =9A	-	15	18	mΩ
		V _{GS} =4.5V, I _{DS} =5A	-	19	28	
G _{fs}	Forward Transconductance	V _{DS} =3V, I _{DS} =5A	-	12	-	S
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =1A, V _{GS} =0V	-	0.75	1.1	V
t _{rr} ^b	Reverse Recovery Time	I _{SD} =8A, dI _{SD} /dt=100A/μs	-	12	-	ns
Q _{rr} ^b	Reverse Recovery Charge		-	3.5	-	nC
Dynamic Characteristics ^b						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	1	1.5	3	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, Frequency=1.0MHz	300	410	550	pF
C _{oss}	Output Capacitance		50	70	100	
C _{rss}	Reverse Transfer Capacitance		30	40	60	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =15V, R _L =15Ω, I _{DS} =1A, V _{GEN} =10V, R _G =6Ω	-	6	9	ns
t _r	Turn-on Rise Time		-	9	15	
t _{d(OFF)}	Turn-off Delay Time		-	14	25	
t _f	Turn-off Fall Time		-	3.6	7	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _{DS} =8A	-	8	13	nC
	Total Gate Charge		-	3.8	5.5	
Q _{gth}	Threshold Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _{DS} =8A	-	0.67	-	
Q _{gs}	Gate-Source Charge		-	1.3	-	
Q _{gd}	Gate-Drain Charge		-	1.6	-	

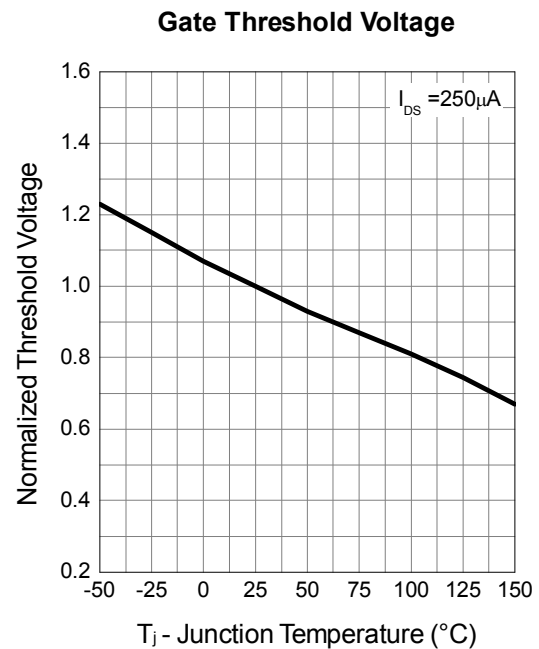
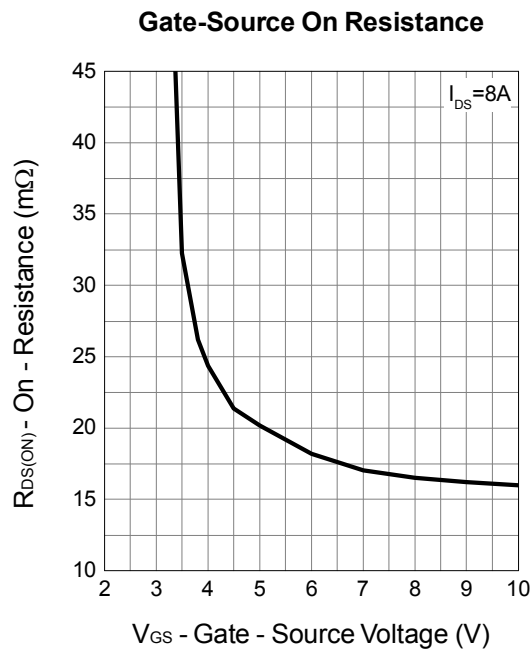
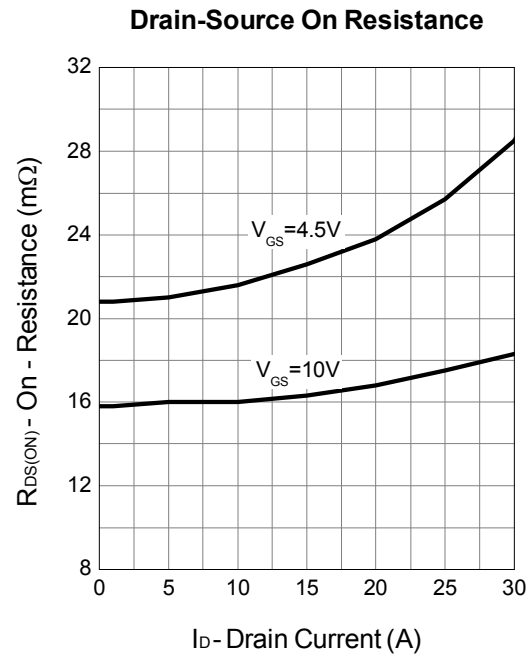
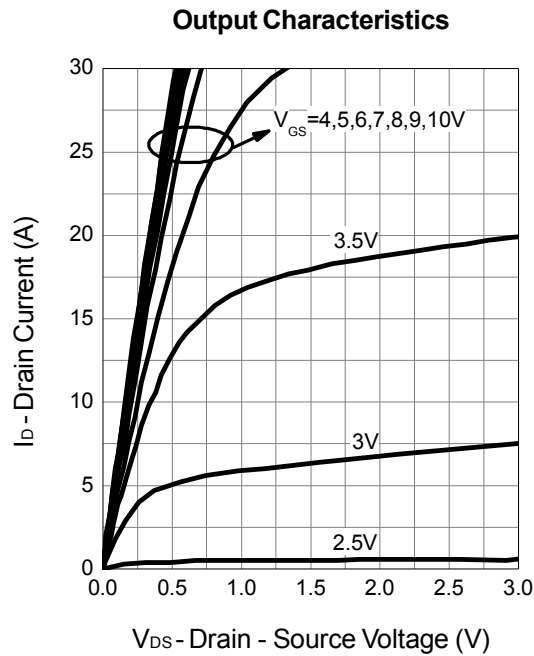
Note a : Pulse test ; pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.

Note b : Guaranteed by design, not subject to production testing.

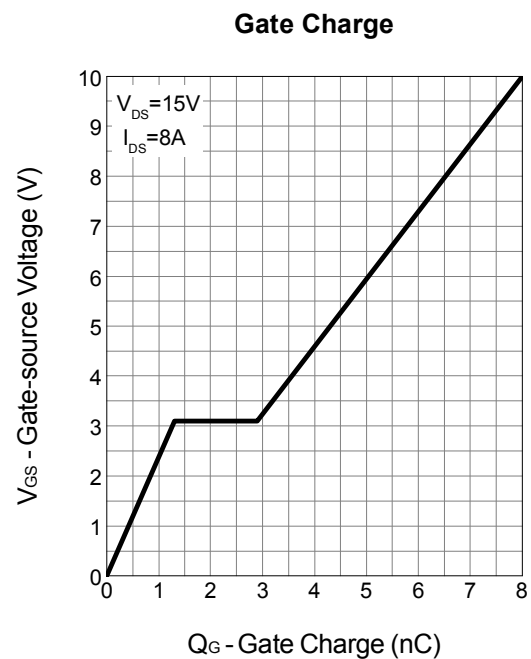
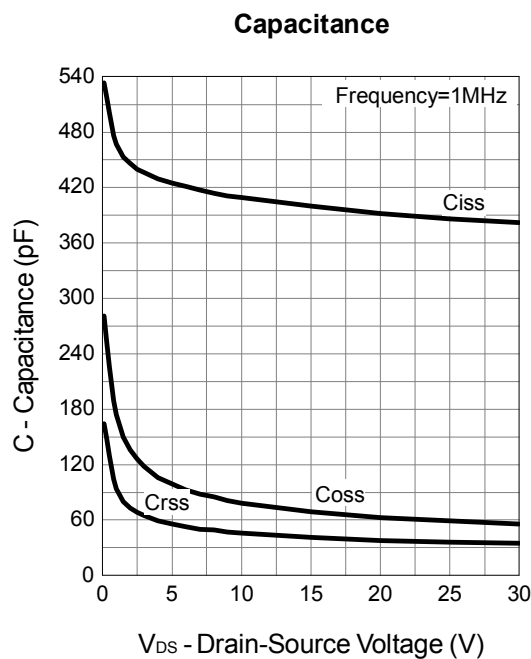
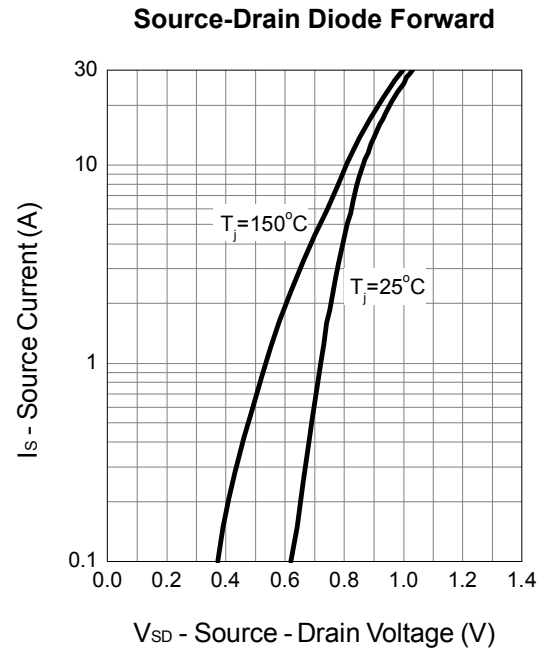
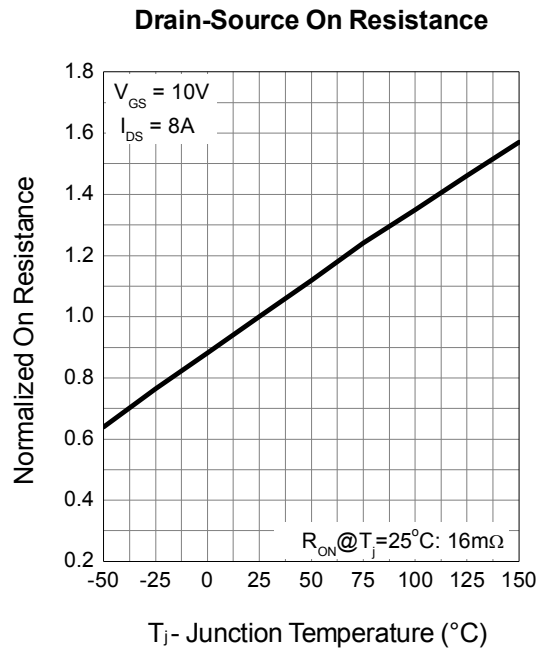
Typical Operating Characteristics



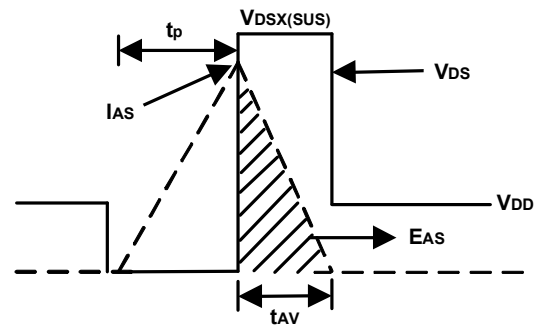
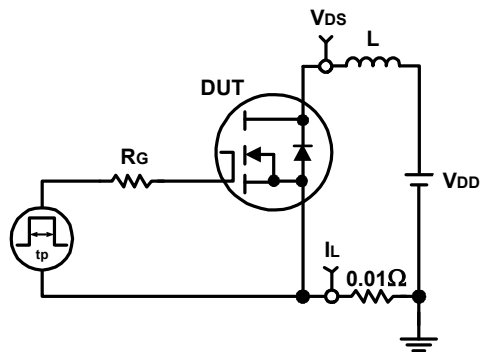
Typical Operating Characteristics (Cont.)



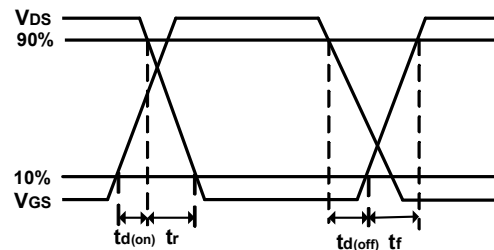
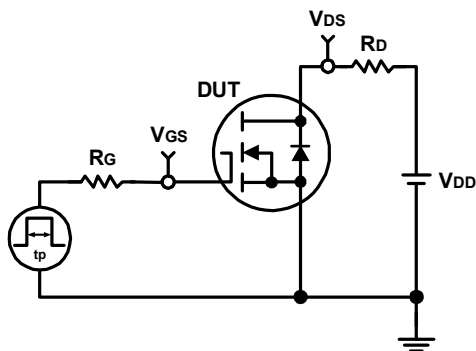
Typical Operating Characteristics (Cont.)



Avalanche Test Circuit and Waveforms

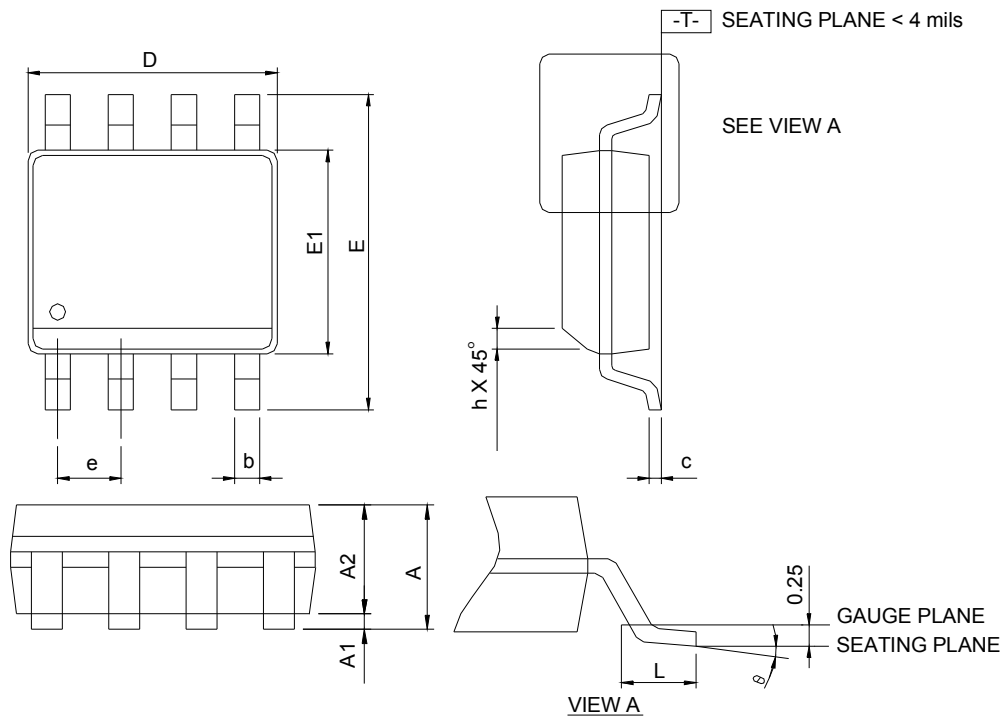


Switching Time Test Circuit and Waveforms



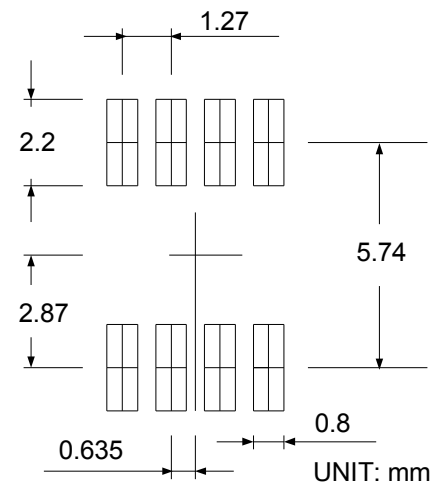
Package Information

SOP8



DIMENSIONS	SOP8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.