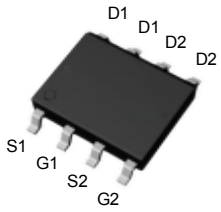
Features

- 100V/3.5A,
  $R_{DS(ON)}$= 78mΩ(typ.) @ V_{GS}= 10V
  $R_{DS(ON)}$= 83mΩ(typ.) @ V_{GS}= 4.5V
- Reliable and Rugged
- Lead Free and Green Devices Available
  (RoHS Compliant)

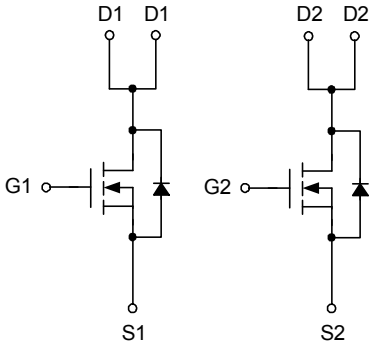
Applications

- Power Management in DC/DC Converter.

Pin Description



Top View of SOP8



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	
I_S	Diode Continuous Forward Current	T_A=25°C	3.5	A
I_D	Continuous Drain Current	T_A=25°C	3.5	A
		T_A=70°C	2.7	
I_{DM} [a]	Pulsed Drain Current	T_A=25°C	10.5	A
P_D	Maximum Power Dissipation	T_A=25°C	2.5	W
		T_A=70°C	1.6	
$R_{\theta JA}$ [c]	Thermal Resistance-Junction to Ambient	t ≤ 10s	50	°C/W
		Steady State	90	°C/W
I_{AS} [b]	Avalanche Current, Single pulse	L=0.5mH	7	A
E_{AS} [b]	Avalanche Energy, Single pulse	L=0.5mH	12	mJ

Note a：Pulse width limited by max. junction temperature.
Note b：UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T_J=25°C).
Note c：Surface Mounted on 1in^2 pad area.

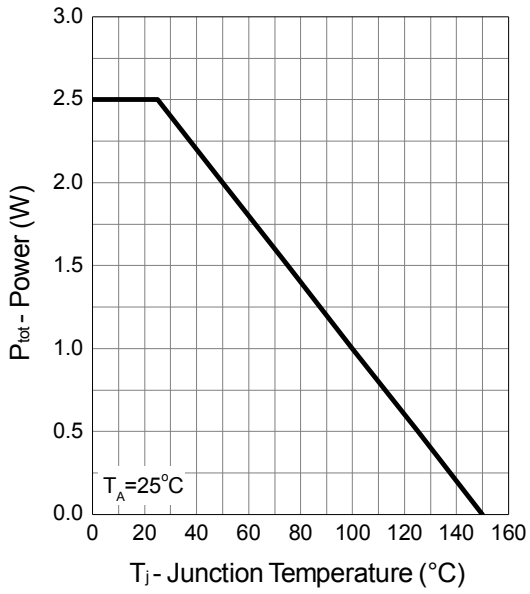
Electrical Characteristics (T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V	-	-	1	μA
		T_J=85°C	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	1	2	3	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±10	μA
$R_{DS(ON)}$ [d]	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=3.5A	-	78	90	mΩ
		V_{GS}=4.5V, I_{DS}=3A	-	83	110	mΩ
Diode Characteristics						
V_{SD} [d]	Diode Forward Voltage	I_{SD}=3A, V_{GS}=0V	-	0.8	1.3	V
t_{rr}	Reverse Recovery Time	I_{SD}=3A, dI_{SD}/dt=100A/μs	-	27	-	ns
Q_{rr}	Reverse Recovery Charge		-	36	-	nC
Dynamic Characteristics [e]						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz	-	2.5	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, Frequency=1.0MHz	-	740	960	pF
C_{oss}	Output Capacitance		-	45	-	
C_{rss}	Reverse Transfer Capacitance		-	24	-	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=30V, R_L=30Ω, I_{DS}=1A, V_{GEN}=10V, R_G=6Ω	-	11	20	ns
t_r	Turn-on Rise Time		-	6	11	
$t_{d(OFF)}$	Turn-off Delay Time		-	27	49	
t_f	Turn-off Fall Time		-	5	10	
Gate Charge Characteristics [e]						
Q_g	Total Gate Charge	V_{DS}=30V, V_{GS}=4.5V, I_{DS}=3.5A	-	7.7	-	nC
Q_g	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_{DS}=3.5A	-	16	23	
Q_{gs}	Gate-Source Charge		-	2.5	-	
Q_{gd}	Gate-Drain Charge		-	3	-	

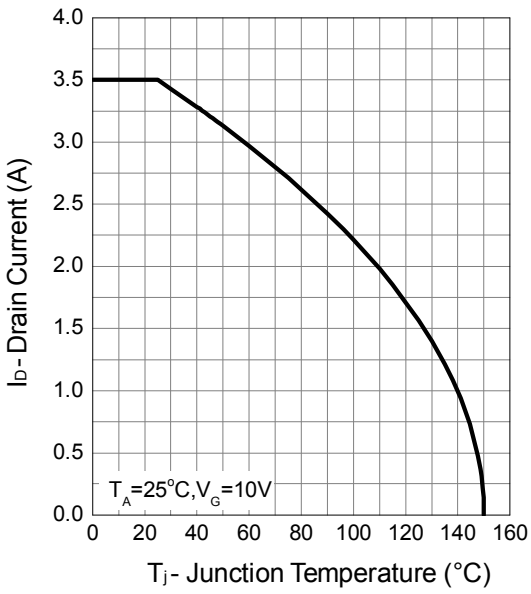
Note d：Pulse test ; pulse width≤300μs, duty cycle≤2%.
Note e：Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

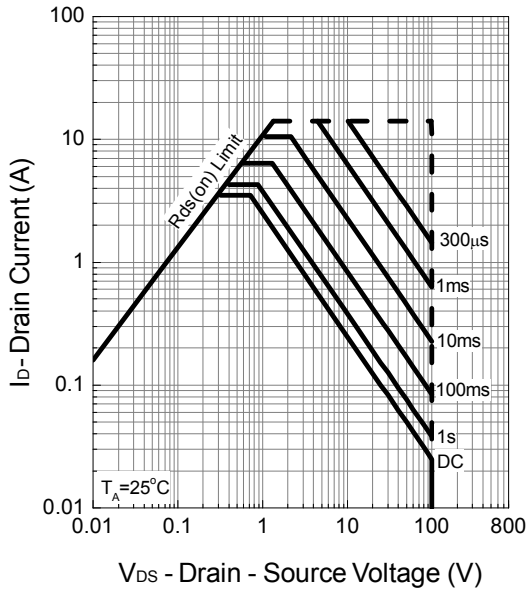
Power Dissipation



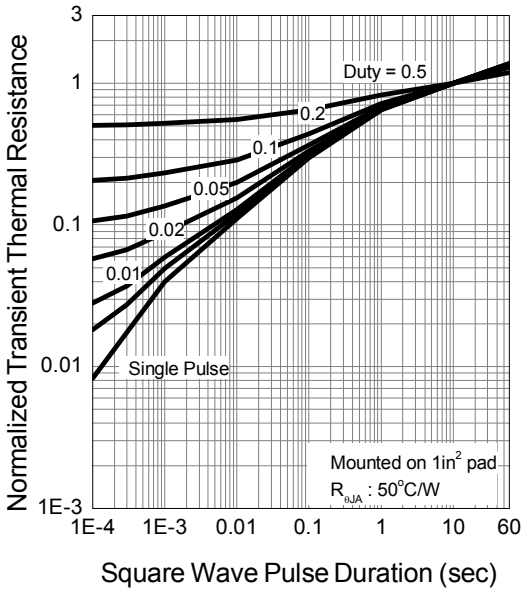
Drain Current



Safe Operation Area

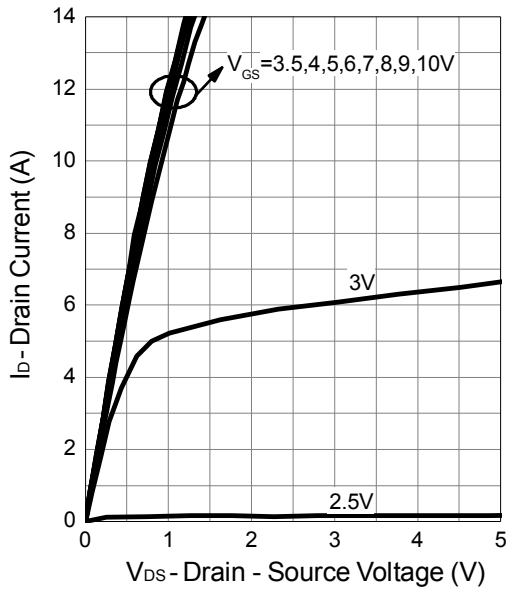


Thermal Transient Impedance

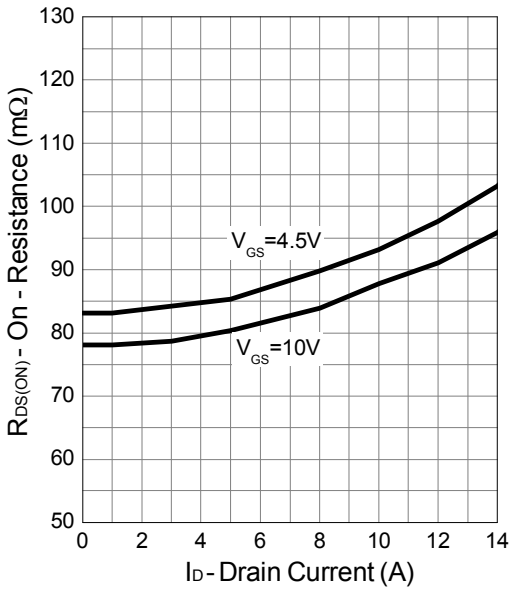


Typical Operating Characteristics (Cont.)

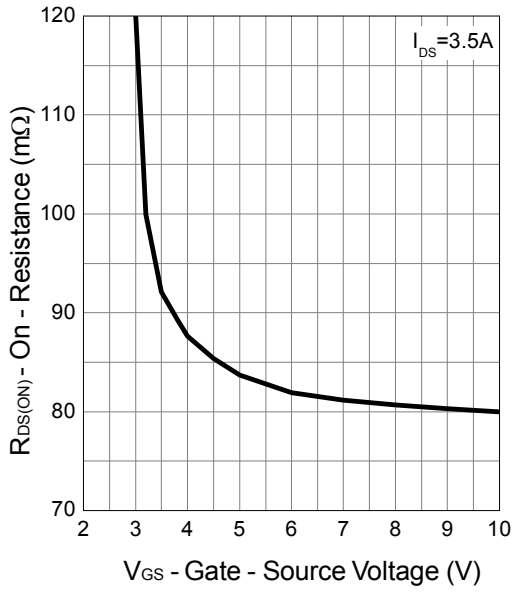
Output Characteristics



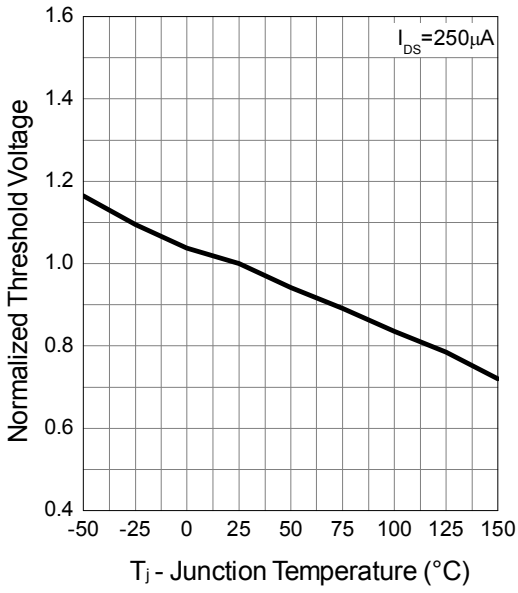
Drain-Source On Resistance



Gate-Source On Resistance

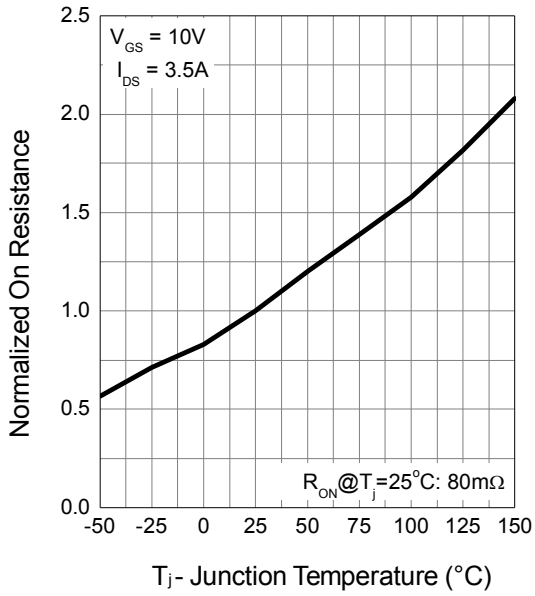


Gate Threshold Voltage

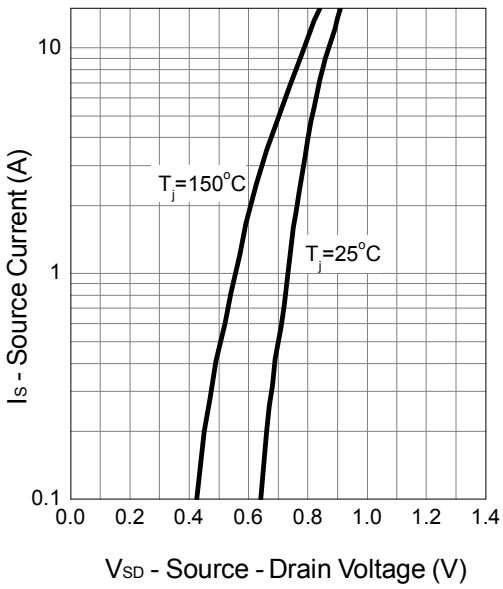


Typical Operating Characteristics (Cont.)

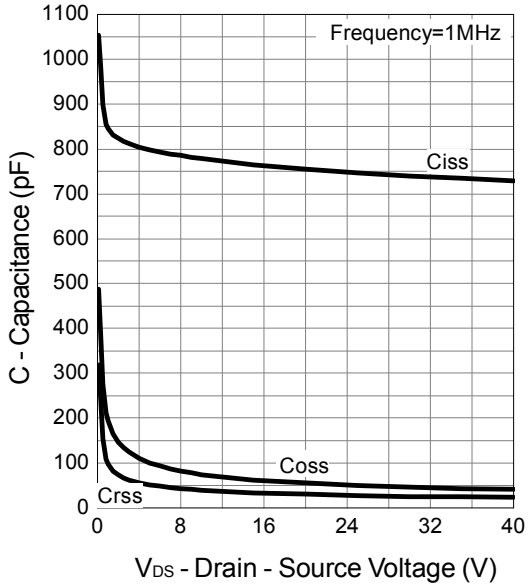
Drain-Source On Resistance



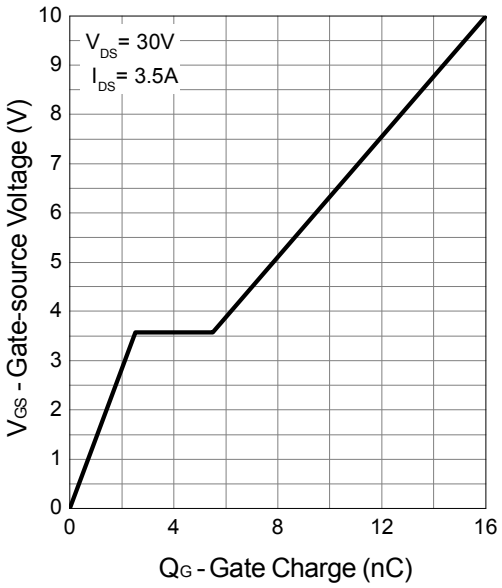
Source-Drain Diode Forward



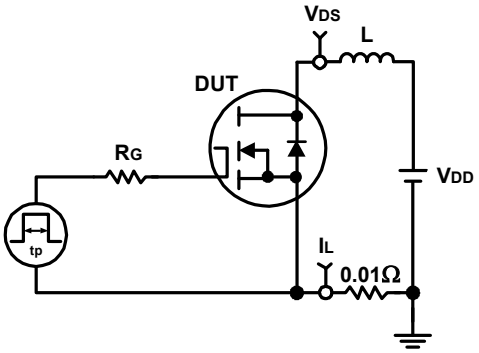
Capacitance

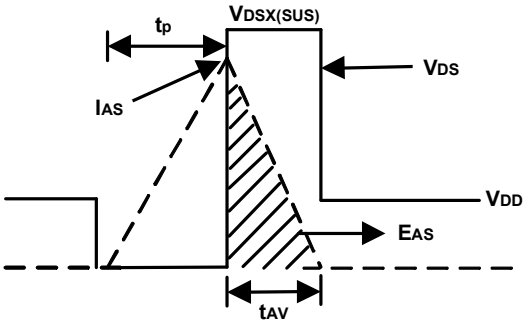


Gate Charge

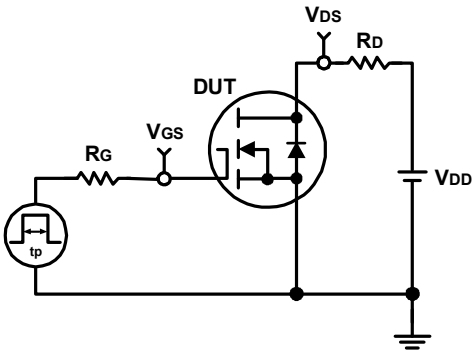


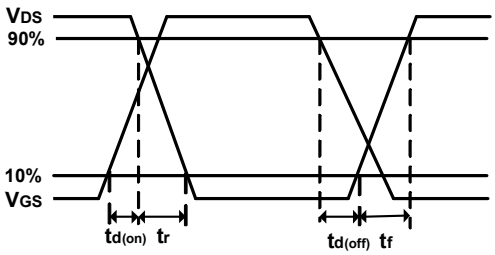
Avalanche Test Circuit and Waveforms





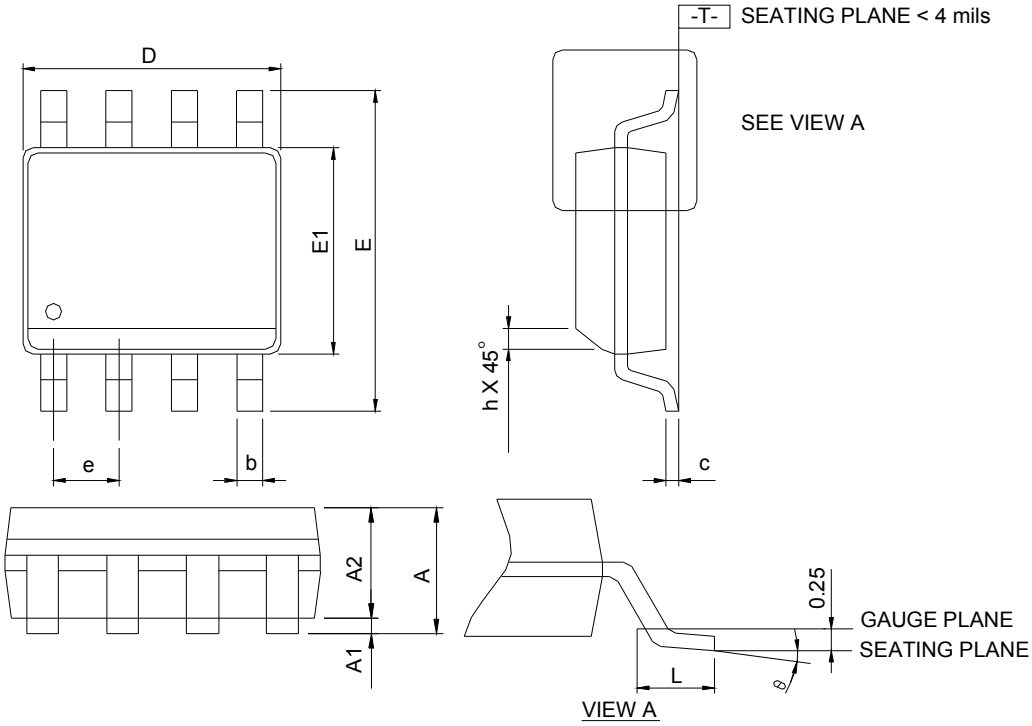
Switching Time Test Circuit and Waveforms





Package Information

SOP8



SYMBOL	SOP8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN