

GaN Amplifier, 40 V, 100 W

8.4 - 9.6 GHz



CGHV96100F2

Rev. V5

Features

- Output Power: 100 W
- Power Gain: 10 dB
- PAE: 45%
- Internally Matched: 50 Ω
- Power Droop: <0.3 dB
- RoHS* Compliant

Applications

- Marine Radar
- Weather Monitoring
- Air Traffic Control
- Maritime Vessel Traffic Control
- Port Security

Description

The CGHV96100F2 is a gallium nitride (GaN) high electron mobility transistor (HEMT) on Silicon Carbide (SiC) substrates. This GaN internally matched (IM) FET offers excellent power added efficiency in comparison to other technologies. GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity and higher thermal conductivity. GaN HEMTs also offer greater power density and wider bandwidths compared to GaAs transistors. This IM FET is available in a metal/ceramic flanged package for optimal electrical and thermal performance.



AC-587BH-2

Ordering Information

Part Number	Package
CGHV96100F2	bulk
CGHV96100F2-AMP	test board

Typical Performance¹: 8.4 - 9.6 GHz ($T_c = +25^\circ\text{C}$) of Demonstration Amplifier

Parameter	8.4 GHz	8.8 GHz	9.0 GHz	9.2 GHz	9.4 GHz	9.6 GHz	Units
Linear Gain	13.8	12.8	13.0	12.4	11.8	11.4	dB
Gain	10.3	10.1	10.0	9.7	9.4	9.1	dB
Output Power	171	163	160	150	137	131	W
Power Added Efficiency	45.5	42.8	41.5	39.2	35.5	35.4	%

1. Measured in the CGHV96100F2-AMP (838179) application circuit, under 100 μs pulse width, 10% duty cycle, $P_{IN} = 42 \text{ dBm}$.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

DC Electrical Characteristics² @ T_C = +25°C

Characteristics	Symbol	Conditions	Units	Min.	Typ.	Max.
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = 10 V, I _D = 28.8 mA	V	-3.8	-3.0	-2.3
Gate Quiescent Voltage	V _{GS(Q)}	V _{DS} = 40 V, I _D = 1000 mA	V	—	-2.7	—
Saturated Drain Current ³	I _{DS}	V _{DS} = 6 V, V _{GS} = 2 V	A	20.7	28.8	—
Drain-Source Breakdown Voltage	V _{BR}	V _{GS} = -8 V, I _D = 28.8 mA	V	100	—	—

2. Measured on-wafer prior to packaging.

3. Scaled from PCM data

RF Electrical Characteristics⁴ @ T_C = +25°C, V_{DD} = 40 V, I_{DQ} = 1000 mA

Characteristics	Symbol	Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	S21	P _{IN} = -20 dBm	dB	10.5	12.4	—
Input Return Loss	S11	P _{IN} = -20 dBm 8.4 - 9.4 GHz 9.4 - 9.6 GHz	dB	—	-5.2 —	-2.8 -3.3
Output Return Loss	S22	P _{IN} = -20 dBm	dB	—	-12.3	-6.0
Output Power ^{4,5}	P _{OUT}	P _{IN} = 41.5 dBm	W	100	131	—
Power Added Efficiency ^{4,5}	PAE	P _{IN} = 41.5 dBm	%	30	45	—
Power Gain	P _G	P _{IN} = 41.5 dBm	dB	—	10.2	—
Output Mismatch Stress	VSWR	No damage at all phase angles	Ψ	—	—	5:1

4. Measured in CGHV96100F2-AMP under 100 μs pulse width, 10% duty

5. Fixture loss de-embedded using the following offsets: Frequency = 9.6 GHz. Input = 0.5 dB and Output = 0.5 dB.

ESD Ratings

Characteristics	Symbol	Class	Test Methodology
Human Body Model	HBM	2	JEDEC JESD22 A114-D
Charge Device Model	CDM	C3	JEDEC JESD22 C101-C

Absolute Maximum Ratings (Not Simultaneous)

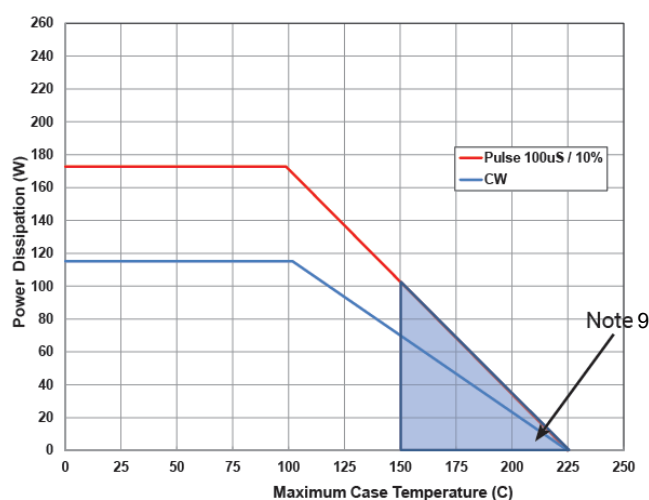
Parameter	Symbol	Conditions	Units	Rating
Drain-Source Voltage	V_{DS}	25°C	V	100
Gate-to-Source Voltage	V_{GS}	25°C	V	-10 to +2
Forward Gate Current	I_{GMAX}	25°C	mA	28.8
Drain Current ⁶	I_{DMAX}	25°C	A	12
Power Dissipation	P_{DISS}	CW / Pulse	W	115.2 / 222.0
Thermal Resistance, Junction to Case	$R_{\theta JC}$	100 μ s, 10%, 85°C, $P_{DISS} = 173$ W CW, 85°C, $P_{DISS} = 115.2$ W	°C/W	0.71 1.07
Screw Torque	τ	—	in-oz	40
Soldering Temperature ⁷	T_S	—	°C	245
Operating Junction Temperature	T_J	—	°C	225
Case Operating Temperature ⁸	T_C	—	°C	-40 to +125
Storage Temperature	T_{STG}	—	°C	-65 to +150
Pulse Width	P_W	85°C	μ s	100
Duty Cycle	D	85°C	%	10

6. Current limit for long term, reliable operation.

7. Refer to the Application Note on soldering.

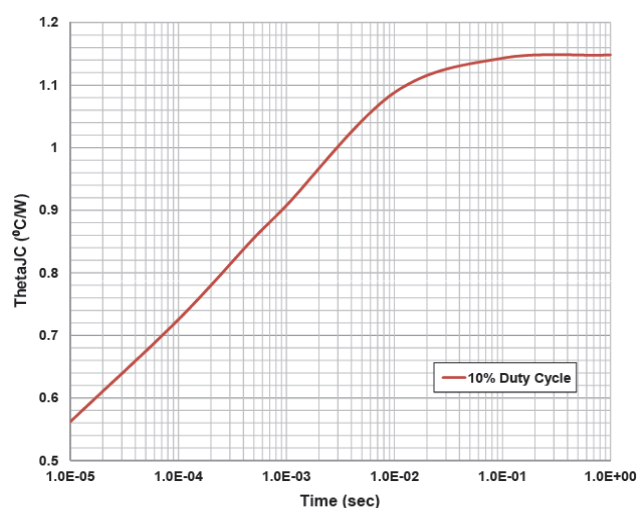
8. See Power Dissipation Derating curve.

Power Dissipation Derating Curve



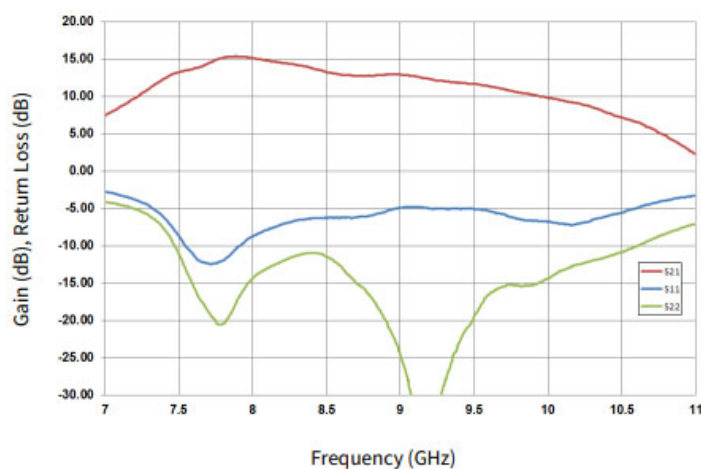
9. Shaded area exceeds maximum case operating temperature.

Transient Curve

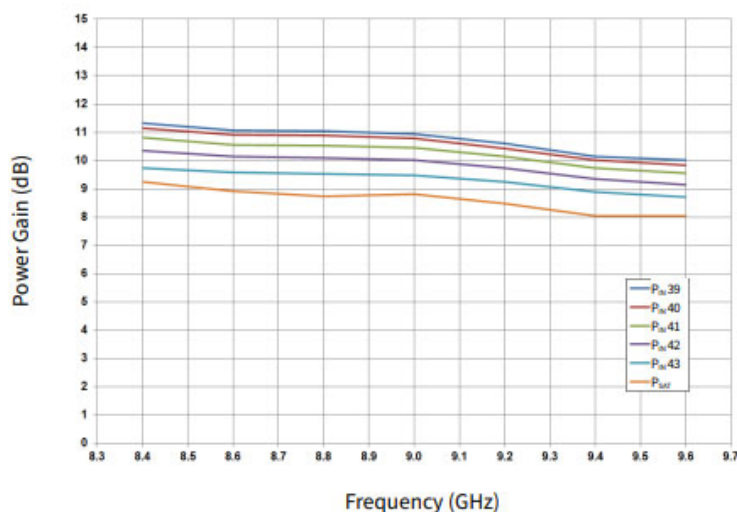


Typical Performance Curves

S-Parameters vs. Freq., $V_{DD} = 40$ V, $I_{DQ} = 1000$ mA

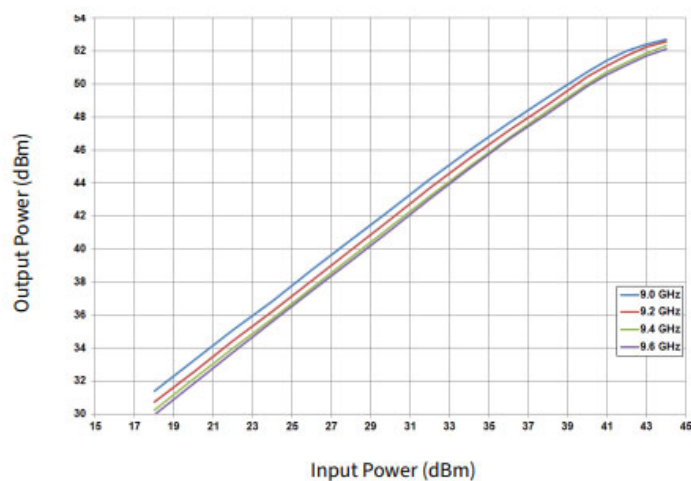


Power Gain vs. Freq. over Input Power, $V_{DD} = 40$ V, $I_{DQ} = 1000$ mA, Pulse Width = 100 μ s, Duty Cycle = 10%

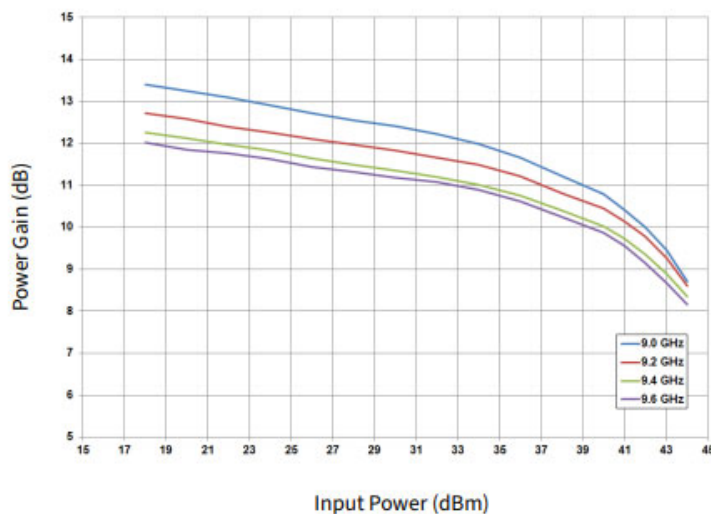


Typical Performance Curves

Output Power vs. Input Power over Freq., $V_{DD} = 40\text{ V}$, $I_{DQ} = 1000\text{ mA}$, Pulse Width = 100 μs , Duty Cycle = 10%

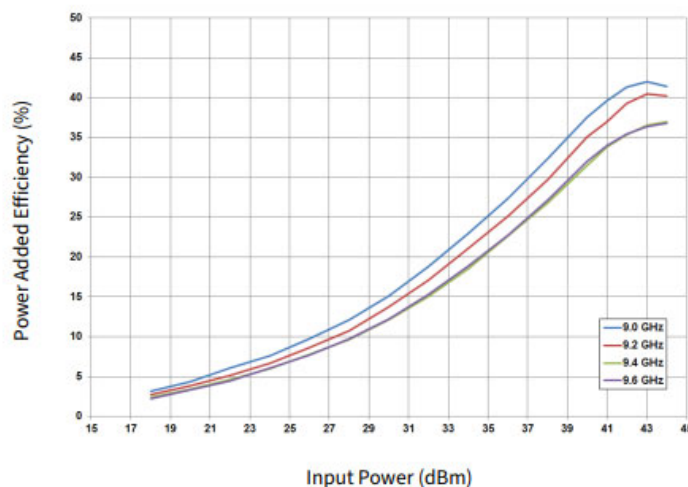


Power Gain vs. Input Power over Freq., $V_{DD} = 40\text{ V}$, $I_{DQ} = 1000\text{ mA}$, Pulse Width = 100 μs , Duty Cycle = 10%

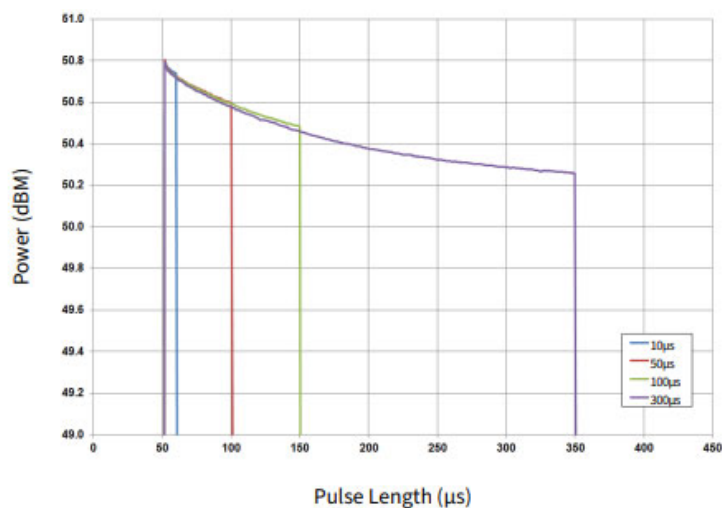


Typical Performance Curves

Power Added Efficiency vs. Input Power over Freq., $V_{DD} = 40$ V, $I_{DQ} = 1000$ mA, Pulse Width = 100 μ s, Duty Cycle = 10%

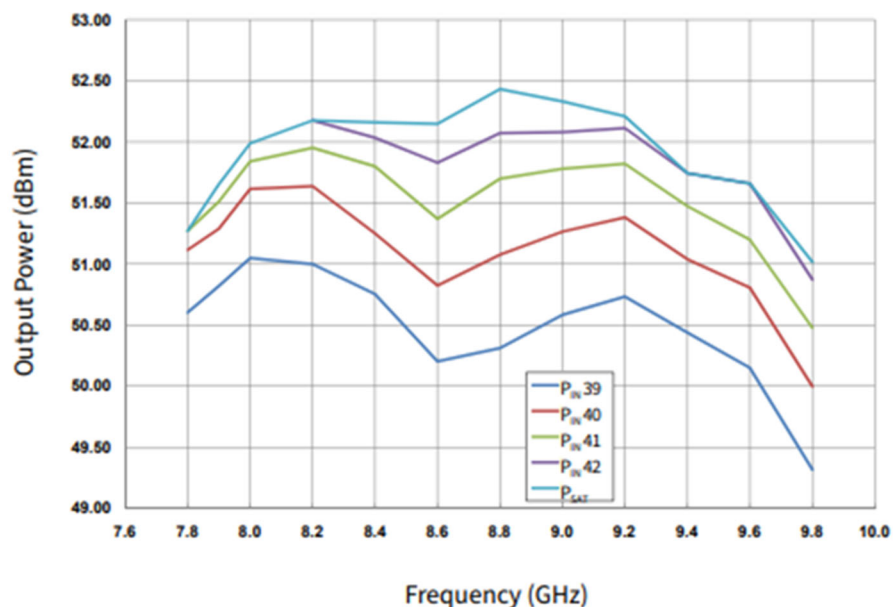


Power vs. Pulse Width, $V_{DD} = 40$ V, $I_{DQ} = 1000$ mA, $P_{IN} = 41$ dBm, Duty Cycle = 10%

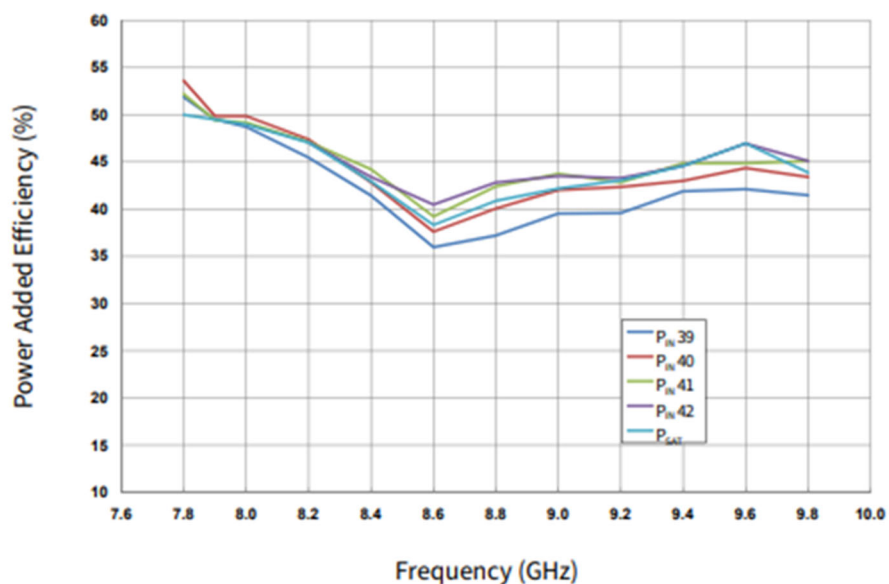


Typical Performance Curves

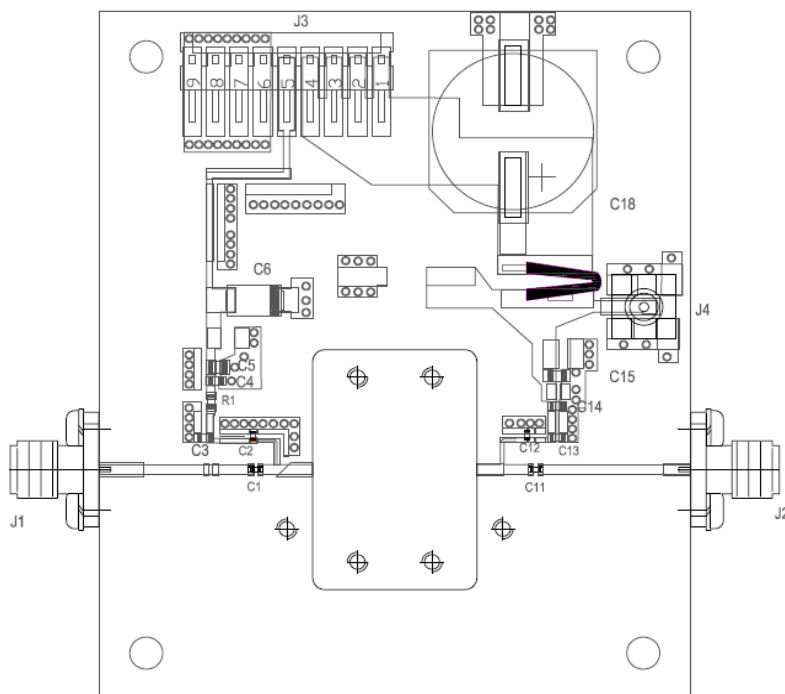
Output Power vs. Freq. over Input Power, $V_{DD} = 40$ V, $I_{DQ} = 1000$ mA, Pulse Width = 100 μ s, Duty Cycle = 10%



Power Added Efficiency vs. Freq. over Input Power, $V_{DD} = 40$ V, $I_{DQ} = 1000$ mA, Pulse Width = 100 μ s, Duty Cycle = 10%



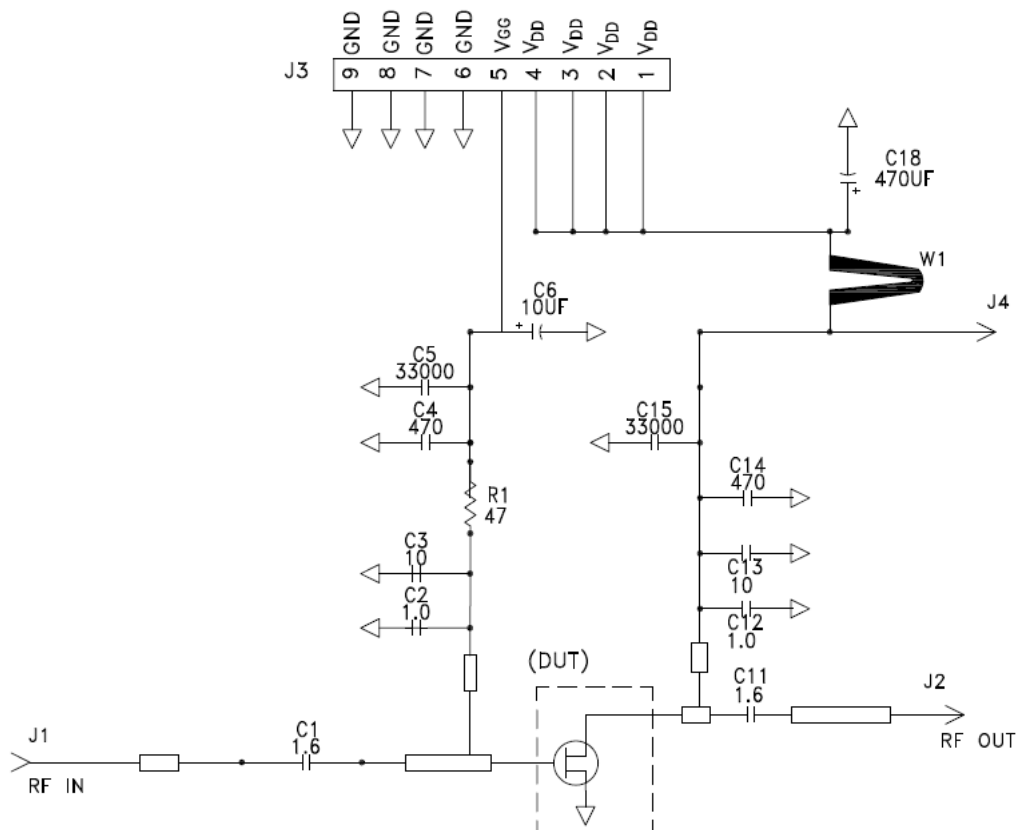
Application Circuit



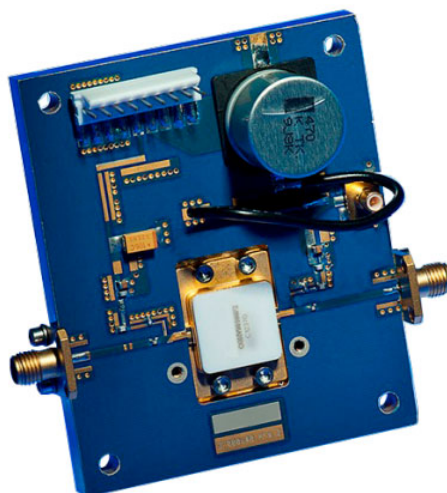
Application Circuit Bill of Materials

Designator	Description	Qty
C1, C11	CAP, 1.6 pF, +/-0.1 pF, 200 V, 0402, ATC 600L	2
C2, C12	CAP, 1.0 pF, +/-0.1 pF, 200 V, 0402, ATC 600L	2
C3, C13	CAP, 10 pF, +/-5%, 250 V, 0603, ATC	2
C4, C14	CAP, 470 pF, 5%, 100 V, 0603	2
C5, C15	CAP, 33000 pF, 0805, 100 V, X7R	2
C6	CAP, 10 µF 16 V TANTALUM	1
C18	CAP, 470 µF, +/-20%, ELECTROLYTIC	1
R1	RES, 47 OHM +/-1%, 1/16 W, 0603, SMD	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20 MIL	2
J3	HEADER, RT>PLZ, 0.1 CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
—	PCB, TEST FIXTURE, TACONICS RF35P, 20 MIL THK, 440210 PKG	1
—	2-56 SOC HD SCREW 1/4 SS	4
—	#2 SPLIT LOCKWASHER SS	4
Q1	CGHV96100F2	1

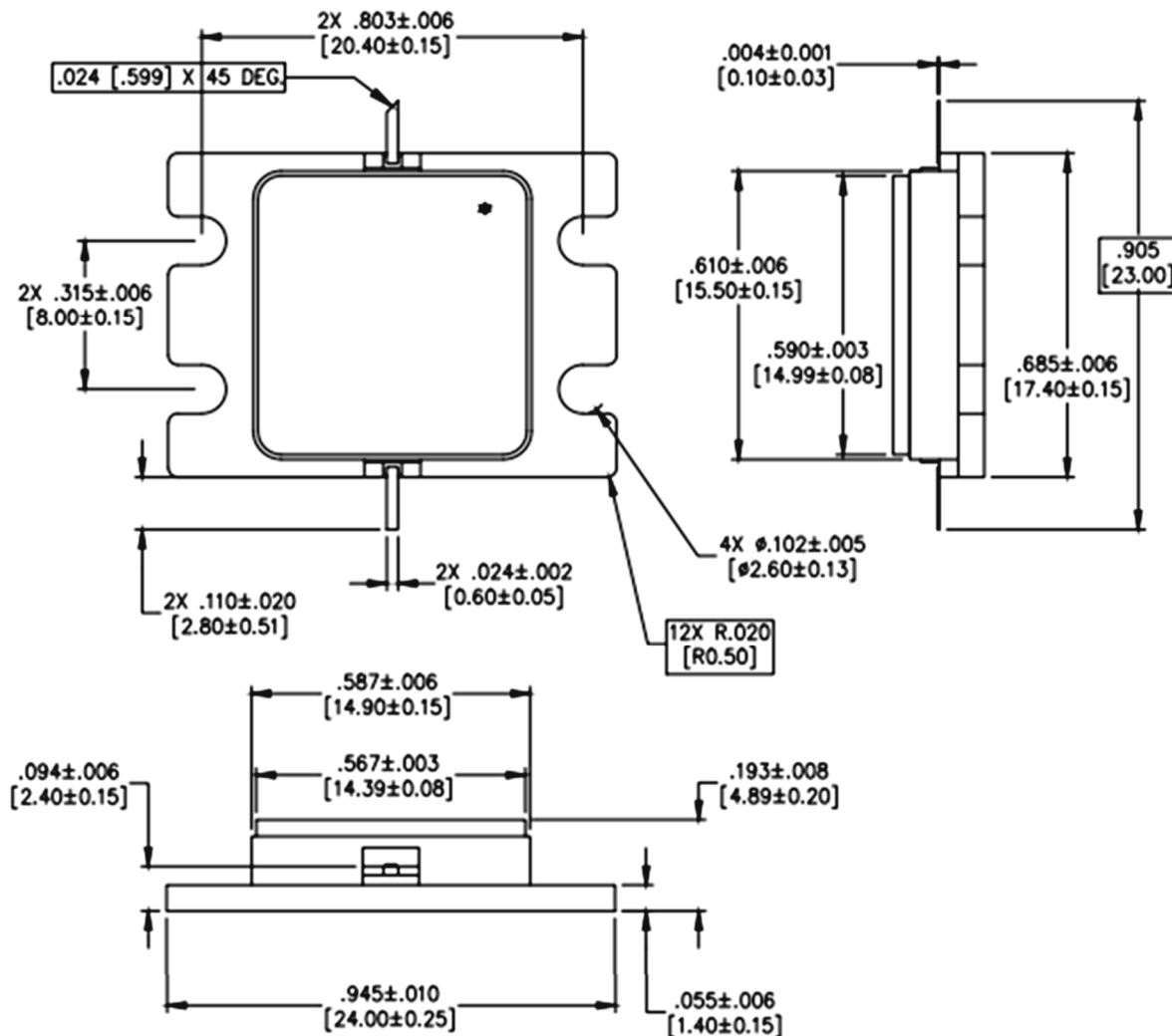
Application Circuit Schematic



CGHV96100F2-AMP Demonstration Amplifier Circuit



Product Dimensions (Package Type AC-587BH-2)



NOTES:

1. ALL DIMENSIONS SHOWN AS in[mm]. CONTROLLING DIMENSIONS ARE IN IN AND CONVERTED mm DIMENSIONS ARE NOT NECESSARILY EXACT.
2. ALL TOLERANCES ARE $\pm .005 \ [0.13]$ UNLESS OTHERWISE NOTED
3. LEAD FINISH: AU
FLANGE FINISH: AU
4. LID SEAL EPOXY MAY FLOW OUT A MAXIMUM OF $.020 \ [0.51]$ FROM EDGE OF LID
5. LID MAY BE MIS-ALIGNED UP TO $.010 \ [0.25]$ FROM PACKAGE IN ANY DIRECTION

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