ME7724-G

N-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7724-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

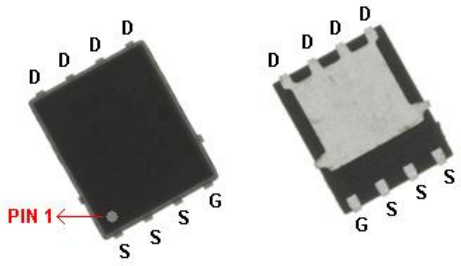
- RDS(ON)≦2.8mΩ@VGS=10V
- RDS(ON)≦4.2mΩ@VGS=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

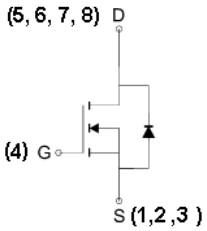
APPLICATIONS

- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

PowerDFN 5x6





N-Channel MOSFET

Ordering Information: ME7724-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	108	A
	T_C=70℃		86	A
	T_A=25℃		24.9	
	T_A=70℃		19.9	
Pulsed Drain Current*		I_{DM}	323	A
Maximum Power Dissipation*	T_C=25℃	P_D	52	W
	T_C=70℃		33	
	T_A=25℃		2.8	
	T_A=70℃		1.8	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	2.4	℃/W
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

*Chip silicon limitation current is 100A

DCC 正式發行

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.2		3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=18A		2.3	2.8	mΩ
		V_{GS}=4.5V, I_D=16A		3.1	4.2	
V_{SD}	Diode Forward Voltage	I_S=18A, V_{GS}=0V			1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V,V_{GS}=10V, I_D=20A		66.9		nC
Qg	Total Gate Charge	V_{DS}=15V,V_{GS}=4.5V, I_D=20A		33		
Qgs	Gate-Source Charge			13.1		
Qgd	Gate-Drain Charge			17.1		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		3040		pF
Coss	Output Capacitance			361		
Crss	Reverse Transfer Capacitance			296		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, R_L=15Ω V_{GS}=10V,R_G=3Ω		25.4		ns
tr	Turn-On Rise Time			24		
$t_{d(off)}$	Turn-Off Delay Time			67.1		
t_f	Turn-Off Fall Time			23.3		

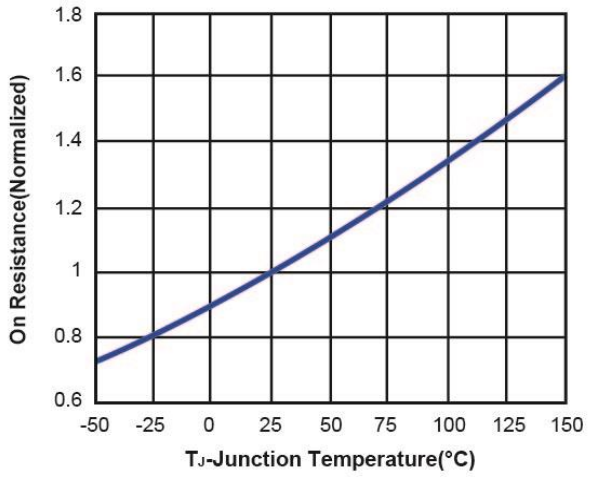
Note: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

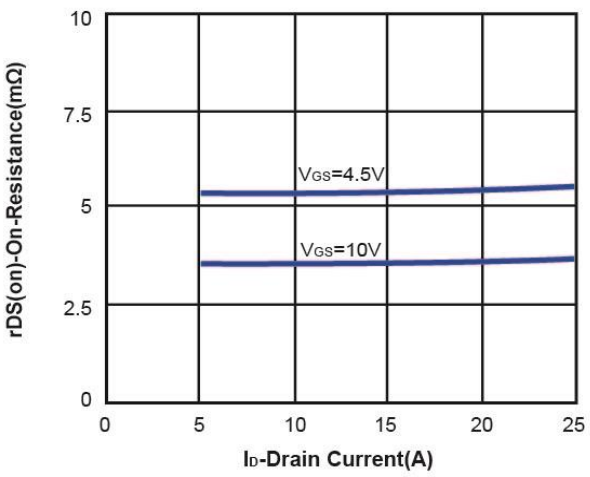
DCC 正式發行

Typical Characteristics (T_J =25℃ Noted)

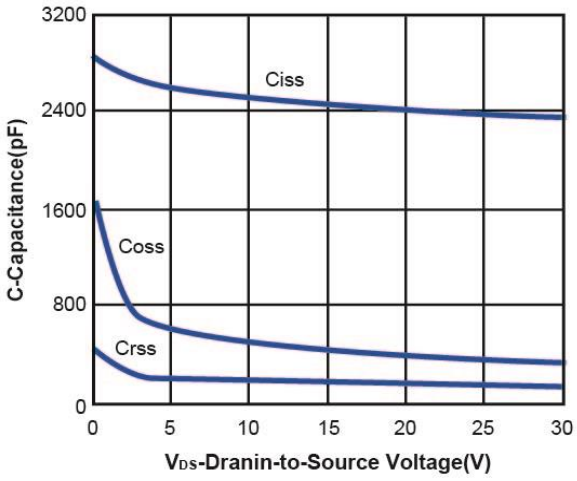
On Resistance vs. Junction Temperature



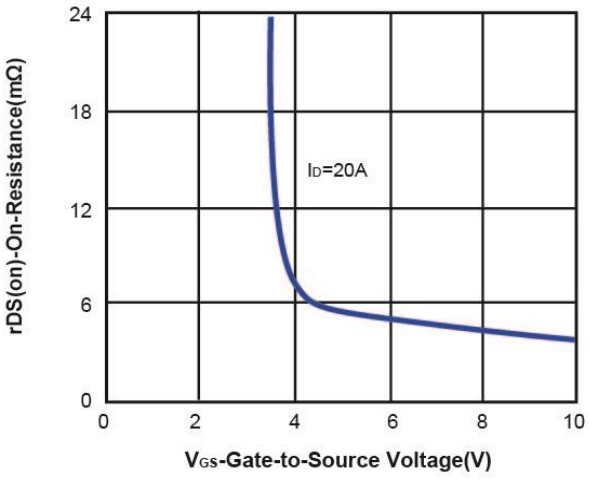
On Resistance vs. Drain Current



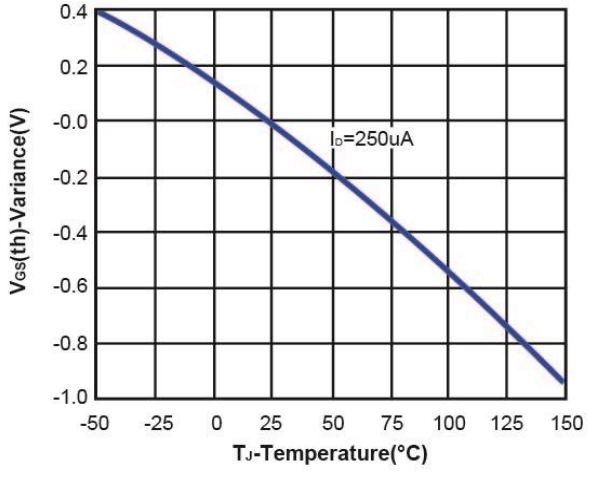
Capacitance



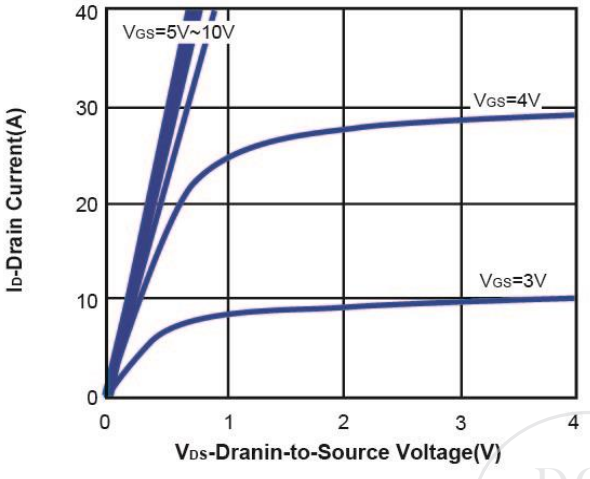
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



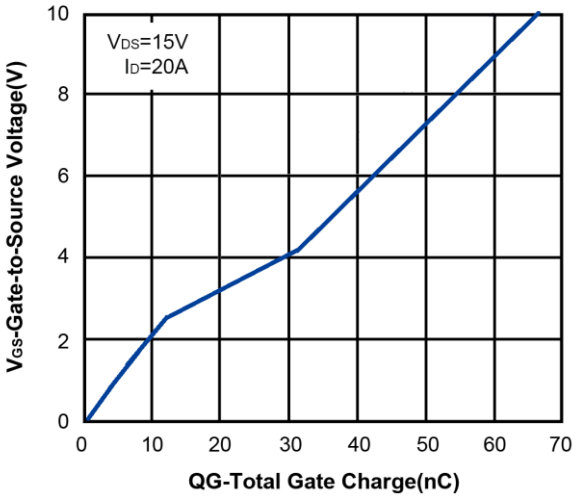
On-Region Characteristics



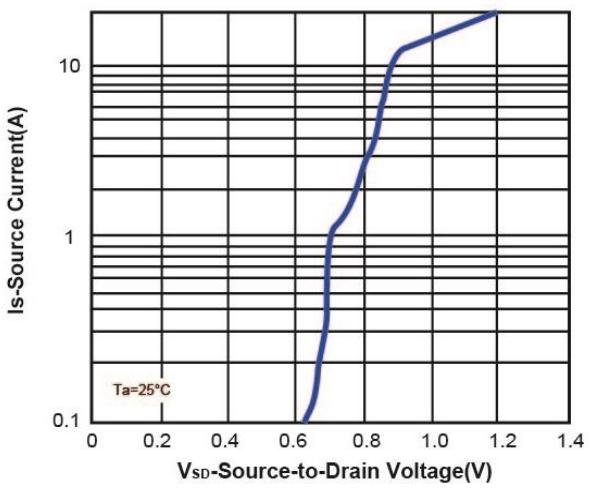
DCC 正式發行

Typical Characteristics (T_J =25℃ Noted)

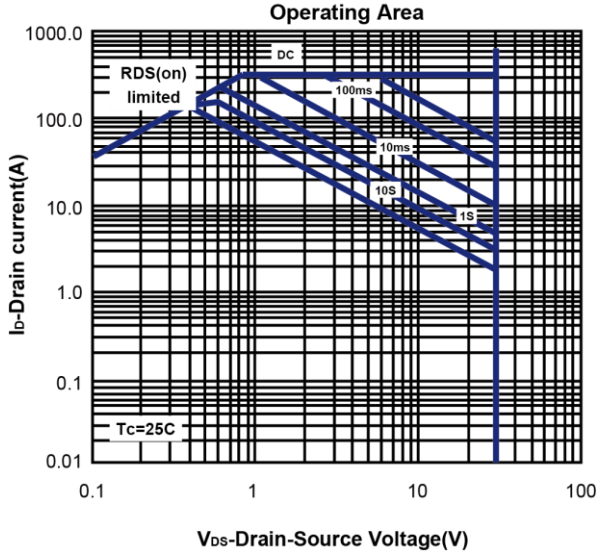
Gate Charge



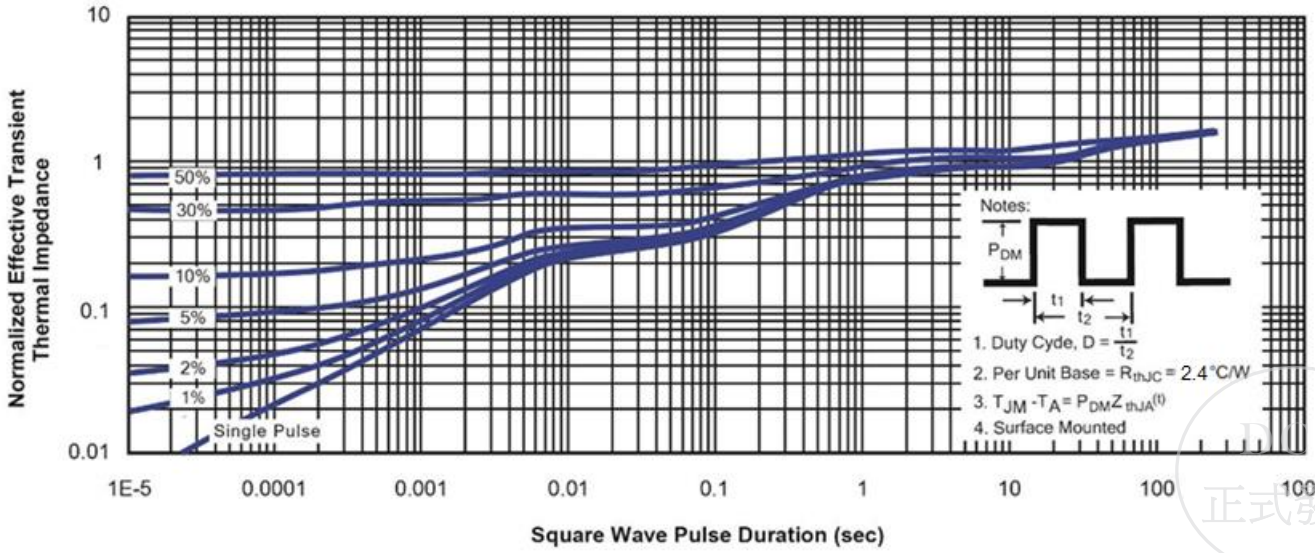
Body-diode characteristics



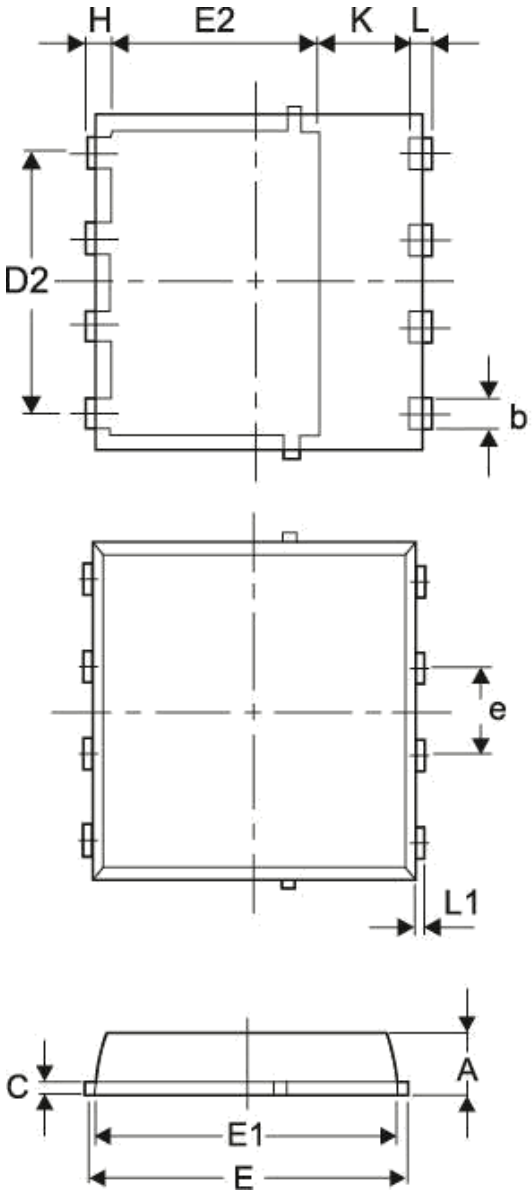
Maximum Forward Biased Safe Operating Area

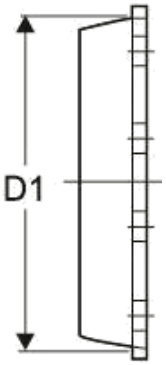


Normalized Thermal Transient Impedance, Junction-to-Case



Power DFN5x6 Package Outline





SYMBOL	MILLIMETERS (mm)		
	MIN	TYP	MAX
A	0.90	1.1	1.20
b	0.33	0.4	0.51
C	0.155	0.2	0.30
D1	4.80	5	5.20
D2	3.61	3.8	3.96
E	5.8	6	6.20
E1	5.6	5.8	5.90
E2	3.35	3.8	4.31
e	1.27 BSC		
H	0.35	0.5	0.7
K	1.20	-	-
L	0.35	0.5	0.71
L1	0.05	0.15	0.30

DCC
正式發行