24Bit 19.2-kSPS, Analog-To-Digital Converters With Programmable Gain Amplifier (PGA) For Sensor Measurement

1 Features

- Programmable Data Rates Up to 19.2 kSPS
- Up to 16/8 single end/differential channels
- Real Single-Cycle Settling (SINGLE_CYCLE bit =1)
- Automatic channel sequencer function
- Low-Noise PGA
- Dual 0.1% Matched Programmable Excitation Current Sources
- Precision 10μA IOUT0 special for NTC measurement
- Internal Reference: 8ppm/°C
- Simultaneous 50Hz and 60Hz Rejection at 25 SPS(Single Cycle Settling)
- Sensor Burn-Out Detection and bias generator
- 4 General-Purpose I/Os
- Internal Temperature Sensor
- Analog Supply: Unipolar (2.7 V to 5.25 V) and Bipolar (±2.5 V) Operation
- Digital Supply: 2.7 V to 5.25 V

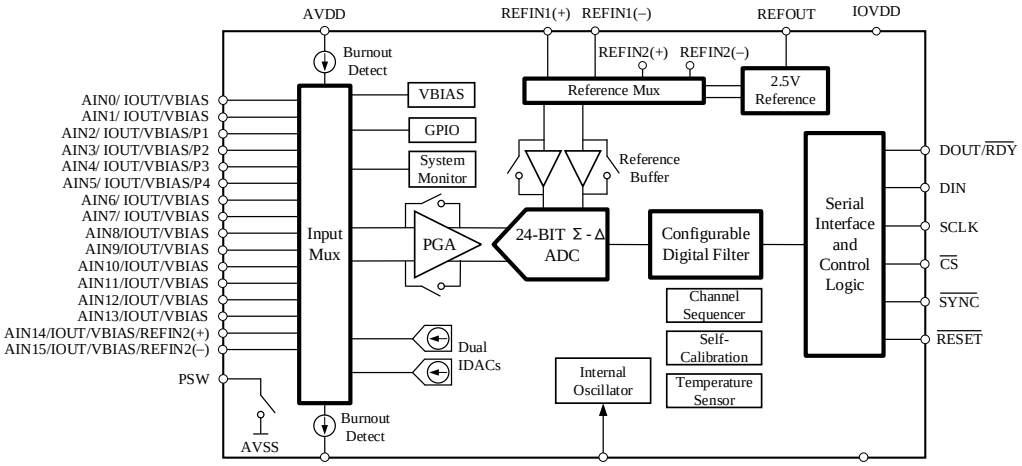
2 Applications

- Temperature Sensor Measurements:
  - RTDs, Thermocouples, and Thermistors
- Pressure Measurements
- Factory Automation and Process Controls
- Instrumentation

Device Information

DEVICE NAME	PACKAGE (PIN)	BODY SIZE
AD7124-8BCPZ	QFN (32)	5.00 mm × 5.00 mm

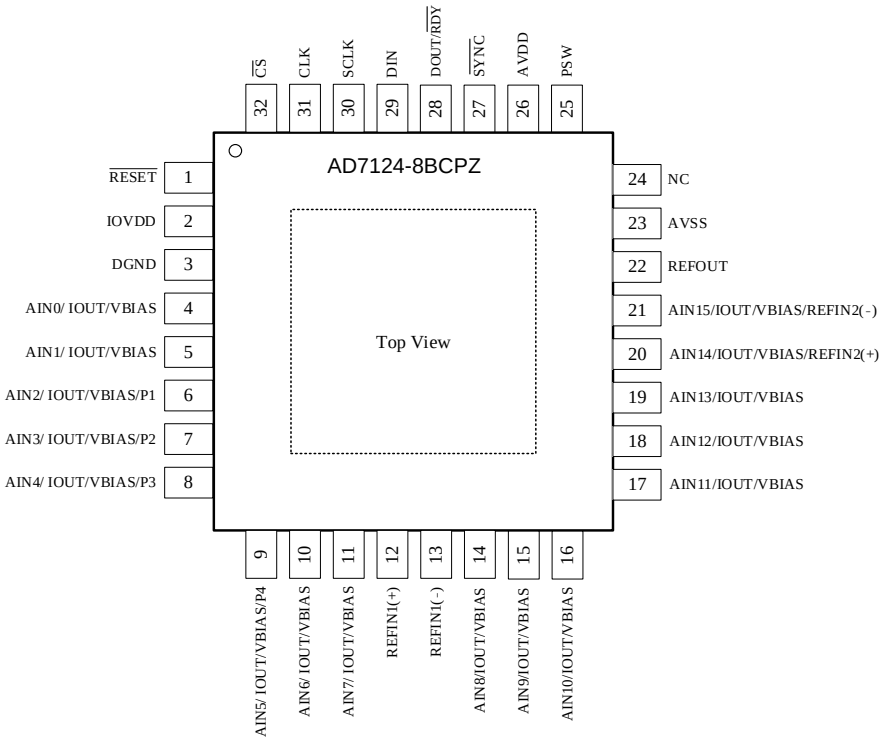
Simplified Schematics



5 Device Comparison Table

Product	Resolution(Bit)	Number of Input	Reference	EXCITATION CURRENT SOURCES	Package
AD7124-8BCPZ	24	16-Input Multiplexer	Internal or External	Yes	QFN (32)

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	AD7124 (QFN32)		
RESET	1	I	Reset(active low), internal pulled up, can be floating or connected to DGND by capacitor.
IOVDD	2	P	Serial Interface and Digital Function supply, connect a 0.1μF capacitor to DGND.
DGND	3	G	Digital ground.
AIN0/IOUT/VBIAS	4	I/O	Analog Input 0/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT1 or IOUT0 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
AIN1/IOUT/VBIAS	5	I/O	Analog Input 1/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.

AIN2/IOUT/VBIAS/P1	6	I/O	Analog Input 2/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 1. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AVSS and AVDD.
AIN3/IOUT/VBIAS/P2	7	I/O	Analog Input 3/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 2. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AVSS and AVDD.
AIN4/IOUT/VBIAS/P3	8	I/O	Analog Input 4/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 3. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AVSS and AVDD.
AIN5/IOUT/VBIAS/P4	9	I/O	Analog Input 5/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 4. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AVSS and AVDD.
AIN6/IOUT/VBIAS	10	I/O	Analog Input 6/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
AIN7/IOUT/VBIAS	11	I/O	Analog Input 7/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
REFIN1(+)	12	I	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). REFIN1(+) can be anywhere between AVDD and AVSS + 0.5 V. The nominal reference voltage (REFIN1(+) − REFIN1(−)) is 2.5 V, but the device functions with a reference from 0.5 V to AVDD.
REFIN1(-)	13	I	Negative Reference Input. This reference input can be anywhere between AVSS and AVDD – 0.5 V.
AIN8/IOUT/VBIAS	14	I/O	Analog Input 8/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
AIN9/IOUT/VBIAS	15	I/O	Analog Input 9/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
AIN10/IOUT/VBIAS	16	I/O	Analog Input 10/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.

AIN11/IOUT/VBIAS	17	I/O	Analog Input 11/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
AIN12/IOUT/VBIAS	18	I/O	Analog Input 12/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
AIN13/IOUT/VBIAS	19	I/O	Analog Input 13/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
AIN14/IOUT/VBIAS/ REFIN2(+)	20	I/O	Analog Input 14/Output of Internal Excitation Current Source/Bias Voltage/Positive Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as a positive reference input for REFIN2(±). REFIN2(+) can be anywhere between AVDD and AVSS + 0.5 V. The nominal reference voltage (REFIN2(+) to REFIN2(−)) is 2.5 V, but the device functions with a reference from 0.5 V to AVDD.
AIN15/IOUT/VBIAS /REFIN2(-)	21	I/O	Analog Input 15/Output of Internal Excitation Current Source/Bias Voltage/Negative Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as the negative reference input for REFIN2(±). This reference input can be anywhere between AVSS and AVDD – 0.5 V.
REFOUT	22	O	Internal Reference Output. The buffered output of the internal 2.5 V voltage reference is available on this pin.
AVSS	23	P	Analog Supply Voltage. The voltage on AVDD is referenced to AVSS. The differential between AVDD and AVSS must be between 2.7 V and 5.25 V in all power mode. AVSS can be taken below 0 V to provide a dual power supply to the AD7124 . For example, AVSS can be tied to −2.5 V and AVDD can be tied to +2.5 V, providing a ±2.5 V supply to the ADC.
NC	24		No internal connection, can be floating or connected to AVSS by capacitor.
PSW	25	O	Low-Side Power Switch to AVSS.
AVDD	26	P	Positive analog power supply, connect a 0.1μF capacitor to AVSS.
$\overline{\text{SYNC}}$	27	I	Synchronization Input. This pin is a logic input that allows synchronization of the digital filters and analog modulators when using a number of SHC6258A devices. When $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic, and the calibration control logic are reset, and the analog modulator is held in a reset state. $\overline{\text{SYNC}}$ does not affect the digital interface but does reset $\overline{\text{RDY}}$ to a high state if it is low. This pin can not be floating, it need pulled up if not using.
DOUT/$\overline{\text{RDY}}$	28	O	Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$ functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can also be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{\text{RDY}}$ pin. When $\overline{\text{CS}}$ is low, the data/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.
DIN	29	I	Serial Data Input to the Input Shift Register on the ADC. Data in the input shift register is transferred to the control registers within the ADC, with the register selection bits of the communications register identifying the appropriate register.

SCLK	30	I	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK pin has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
CLK	31	I	Clock Input/Clock Output. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed.
$\overline{CS}$	32	I	Chip Select Input. This is an active low logic input that selects the ADC. Use $\overline{CS}$ to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low if the serial peripheral interface (SPI) diagnostics are unused, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT interfacing with the device.
EP			Exposed Pad. Leave unconnected or connect to AVSS.

(1), G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Power supply	AVDD to AVSS	-0.3	5.5	V
	AVSS to DGND	-2.8	0.3	V
	IOVDD to DGND	-0.3	5.5	V
Analog input voltage	AINx, REFPx, REFNx, REFOUT	AVSS - 0.3	AVDD + 0.3	V
Digital input voltage	SCLK, DIN, DOUT/$\overline{RDY}$, $\overline{CS}$, $\overline{SYNC}$, CLK	DGND - 0.3	IOVDD + 0.3	V
Input current	Continuous, any pin except power supply pins	-10	10	mA
	Momentary, any pin except power supply pins	-100	100	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	-60	150	°C

7.2 ESD Ratings

		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	V

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
Analog power supply	AVDD to AVSS	2.7		5.25	V
	AVSS to DGND	-2.65		0.1	V
	AVDD to DGND	2.25		5.25	V
Digital power supply	IOVDD to DGND	2.7		5.25	V
ANALOG INPUTS					
V_{IN} Differential input voltage	$V_{(AINP)}$ - $V_{(AINN)}$	-V_{REF} / Gain		V_{REF} / Gain	V
$V_{(AINX)}$ Absolute input voltage	PGA enable, All gain	AVSS + 0.01		AVDD – 0.6	V
	PGA bypass, Gain=1	AVSS - 0.1		AVDD + 0.1	V
VOLTAGE REFERENCE INPUTS					
V_{REF} Differential reference input voltage	REF BUFFER OFF	0.5		AVDD - AVSS	V
	REF BUFFER ON	0.5		AVDD - AVSS - 0.2	V
$V_{(REFNx)}$ Absolute negative reference voltage	REF BUFFER OFF	AVSS - 0.1		$V_{(REFPx)}$ - 0.5	V

	REF BUFFER ON	AVSS + 0.1		$V_{(REFPx)}$ - 0.5	V
$V_{(REFPx)}$ Absolute positive reference voltage	REF BUFFER OFF	$V_{(REFNx)}$ + 0.5		AVDD + 0.1	V
	REF BUFFER ON	$V_{(REFNx)}$ + 0.5		AVDD - 0.1	V
EXTERNAL CLOCK INPUT					
f_{CLK} External clock frequency			2.4576		MHz
External clock duty cycle		45%		55%	
GENERAL-PURPOSE INPUTS/OUTPUTS (GPIO)					
GPIO input voltage		AVSS		AVDD	V
DIGITAL INPUTS					
Digital input voltage		DGND		IOVDD	V
TEMPERATURE RANGE					
T_A Operating ambient temperature		-40		125	°C

7.4 Thermal Information

THERMAL METRIC	AD7124-8BCPZ QFN 32 PINS	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	34	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	24	

7.5 Electrical Characteristics

Minimum and maximum specifications apply from TA = - 40°C to 125°C. Typical specifications are at TA = 25°C.
All specifications are at AVDD = 3.3V, IOVDD = 3.3V, AVSS = 0V, external VREF = 2.5V with reference input buffer enable, and MCLK = 614.4kHz (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS					
Differential input current	PGA enable, Gain=1~128		0.5		nA
	PGA bypass, Gain=1, Full Power Mode		3.1		μA/V
	PGA bypass, Gain=1, Mid Power Mode		0.8		μA/V
	PGA bypass, Gain=1, Low Power Mode		0.4		μA/V
Absolute input current	PGA bypass, Gain=1~128		2		nA
	PGA bypass, Gain=1, Full Power Mode		3.1		μA/V
	PGA bypass, Gain=1, Mid Power Mode		0.8		μA/V
	PGA bypass, Gain=1, Low Power Mode		0.4		μA/V
PGA					
PGA gain settings			1, 2, 4, 8, 16, 32, 64, 128		V/V
SYSTEM PERFORMANCE					
Resolution		24			Bit
DR Data rate	Full Power Mode	9.38		19200	SPS
	Mid Power Mode	2.34		4800	
	Low Power Mode	1.17		2400	
INL Integral nonlinearity			7		ppm
V_{IO} Offset voltage (input referred)	Gain=1/2		±50/Gain		μV
	Gain=4/8/16/32/64/128		±20		
Offset drift (input referred)	Gain=1/2		±0.1		μV/°C
	Gain=4/8/16/32/64/128		±0.05		
Gain error	T_A = 25°C, All gain	-0.05%	0.01%	0.05%	
Gain drift	All gain		3		ppm/°C
CMRR Common-mode rejection	At DC, Gain = 1		90		dB
	At DC, Gain = 16		110		dB
PSRR Power-supply rejection	AVDD / IOVDD at DC, Gain = 1, DR = 20 SPS		100		dB
NMRR Normal-mode rejection			See Table 48		
VOLTAGE REFERENCE INPUTS					
Reference input current	Reference buffer on		3		nA
	Reference buffer off, Full Power Mode		6.2		μA/V
	Reference buffer off, Mid Power Mode		1.6		μA/V
	Reference buffer off, Low Power Mode		0.8		μA/V

INTERNAL VOLTAGE REFERENCE					
V_{REF} Internal reference voltage	T_A = 25°C	2.495	2.500	2.505	V
Reference drift	T_A = –40°C to 125°C		8	15	ppm/°C
Output current			10		mA
Load regulation			400		µV/mA
INTERNAL OSCILLATOR					
Internal oscillator frequency	T_A = –40°C to 125°C	596.0	614.4	632.8	kHz
EXCITATION CURRENT SOURCES (IOUT0/IOUT1)					
Output current settings		10, 50, 100, 250, 500, 750, 1000			µA
Compliance voltage	All current		0.7		V
Absolute error	All currents except 10µA, each IOUT	-5%	1%	5%	
	10µA for IOUT0	-1%	0.5%	1%	
Absolute mismatch(Between IOUT0 and IOUT1)	All currents, between IOUTs , excluding IOUT≦100µA		0.1%		
Temperature drift	All currents except 10µA, each IOUT		50		ppm/°C
Temperature drift matching	Between IOUTs		10		ppm/°C
BURN-OUT CURRENT SOURCES					
Burn-out current source settings			0.5, 2, 4		µA
BIAS VOLTAGE					
Bias voltage			(AVDD + AVSS) / 2		V
Bias voltage output impedance			150		Ω
TEMPERATURE SENSOR					
Accuracy	T_A = 25°C		1.0		°C
Sensitivity			13584		codes/°C
LOW-SIDE POWER SWITCH					
R_{ON} On-resistance			6	10	Ω
Current through switch				30	mA
GENERAL-PURPOSE INPUTS/OUTPUTS (GPIO)					
V_{IL} Low-level input voltage		AVSS		0.3 × AVDD	V
V_{IH} High-level input voltage		0.7 × AVDD		AVDD	V
V_{OL} Low-level output voltage	I_{OL} = 1 mA			0.2 × AVDD	V
V_{OH} High-level output voltage	I_{OH} = 1 mA	0.8 × AVDD			V
DIGITAL INPUTS/OUTPUTS (other than GPIO)					
V_{IL} Low-level input voltage		DGND		0.3 × IOVDD	
V_{IH} High-level input voltage		0.7 × IOVDD		IOVDD	
V_{OL} Low-level output voltage	I_{OL} = 1 mA	DGND		0.2 × IOVDD	

V_{OH} High-level output voltage	I_{OH} = 1 mA	0.8 × IOVDD	
Input leakage	DGND < V_{IN} < IOVDD	1	µA
POWER SUPPLY			
I_{AVDD} Analog supply current	Full power mode, PGA bypass, external reference	380	µA
	Full power mode, PGA=1/2/4, external reference	480	
	Full power mode, PGA=8/16, external reference	560	
	Full power mode, PGA=32, external reference	670	
	Full power mode, PGA=64/128, external reference	810	
	Additional current with REF_BUFP/M enabled, Full power mode	70	
	Mid power mode, PGA bypass, external reference	200	
	Mid power mode, PGA=1/2/4, external reference	330	
	Mid power mode, PGA=8/16, external reference	380	
	Mid power mode, PGA=32, external reference	490	
	Mid power mode, PGA=64/128, external reference	640	
	Additional current with REF_BUFP/M enabled, Mid power mode	40	
	Low power mode, PGA bypass, external reference	120	
	Low power mode, PGA=1/2/4, external reference	200	
	Low power mode, PGA=8/16, external reference	240	
	Low power mode, PGA=32, external reference	290	
	Low power mode, PGA=64/128, external reference	370	
	Additional current with REF_BUFP/M enabled, Low power mode	20	
	Additional current with internal reference enabled, all power mode	150	
	Additional current with internal VBAIS enabled, all power mode	70	
I_{IOVDD} Digital supply current	Full power mode	70	µA
	Mid power mode	40	
	Low power mode	35	
Standby current	I_{AVDD}	0.1	µA
	I_{IOVDD}	11	
Power-Down current	I_{AVDD}	0.1	µA
	I_{IOVDD}	2	

7.6 Timing Requirements

PARAMETER[1,2]			MIN	TYP	MAX	UNIT
SERIAL INTERFACE (SEE Figure 1 TO Figure 6)						
t_3	SCLK high pulse width		100			ns
t_4	SCLK low pulse width		100			ns
t_{12}	Delay between consecutive read/write operations	Full power mode	3/MCLK[3]			ns
		Mid power mode	12/MCLK			ns
		Low power mode	24/MCLK			ns
t_{13}	DOUT/ high time if DOUT/ $\overline{RDY}$ is low and the next conversion is available	Full power mode		6		µs
		Mid power mode		25		µs
		Low power mode		50		µs
t_{14}	SYNC low pulse width	Full power mode	3/MCLK			ns
		Mid power mode	12/MCLK			ns
		Low power mode	24/MCLK			ns
t_1	$\overline{CS}$ falling edge to DOUT/ active time		0		80	ns
t_2[4]	SCLK active edge[5] to data valid delay		0		80	ns
t_5[6,7]	Bus relinquish time after $\overline{CS}$ inactive edge		10		80	ns
t_6	SCLK inactive edge to $\overline{CS}$ inactive edge		50			ns
t_7[8]	SCLK inactive edge to DOUT/$\overline{RDY}$ high	The DOUT_$\overline{RDY}$_DEL bit is cleared, the CS_EN bit is cleared	10			ns
		The DOUT_$\overline{RDY}$_DEL bit is set, the CS_EN bit is cleared	110			ns
t_{7A}	Data valid after $\overline{CS}$ inactive edge, the $\overline{CS}$_EN bit is set		t_5			ns
t_8	$\overline{CS}$ falling edge to SCLK active edge5 setup time		50			ns
t_9	Data valid to SCLK edge setup time		30			ns
t_{10}	Data valid to SCLK edge hold time		25			ns
t_{11}	$\overline{CS}$ rising edge to SCLK edge hold time		50			ns

1. These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with tR = tF = 5 ns (10% to 90% of IOVDD and timed from a voltage level of IOVDD/2.
2. See Figure 1, Figure 2, Figure 3, and Figure 4.
3. MCLK is the master clock frequency.
4. The SCLK active edge is the falling edge of SCLK.
5. $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although subsequent reads must not occur close to the next output update. In continuous read mode, the digital word can be read only once.
6. When the $\overline{CS}$_EN bit is cleared, the DOUT/$\overline{RDY}$ pin changes from its DOUT function to its $\overline{RDY}$ function, following the last inactive edge of the SCLK. When $\overline{CS}$_EN is set, the DOUT pin continues to output the LSB of the data until the $\overline{CS}$ inactive edge.

7.7 Switching Characters

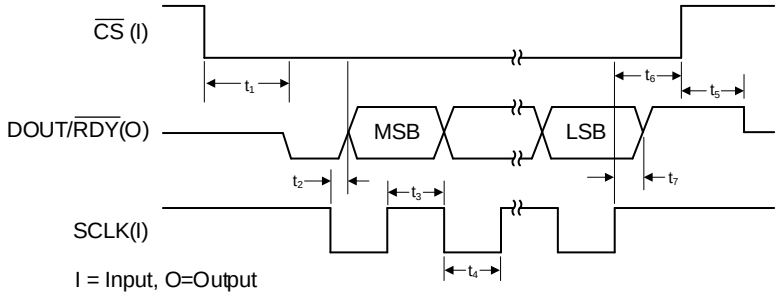


Figure 1: Read Cycle Timing Diagram (CS_EN Bit Cleared)

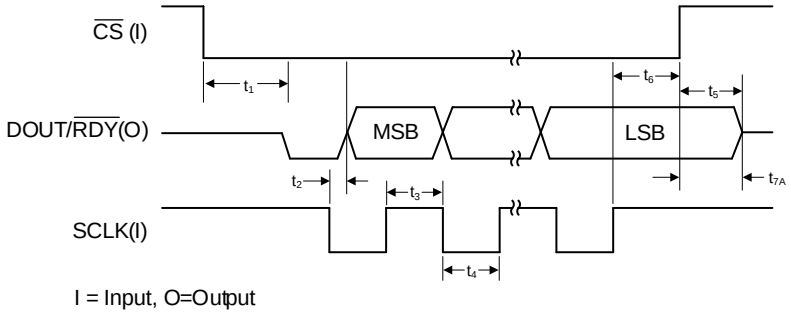


Figure 2: Read Cycle Timing Diagram (CS_EN Bit Set)

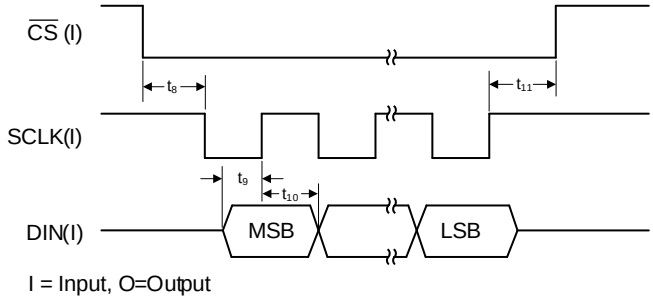


Figure 3: Write Cycle Timing Diagram

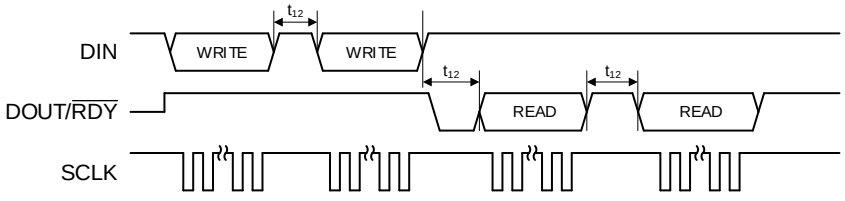


Figure 4: Delay Between Consecutive Serial Operations

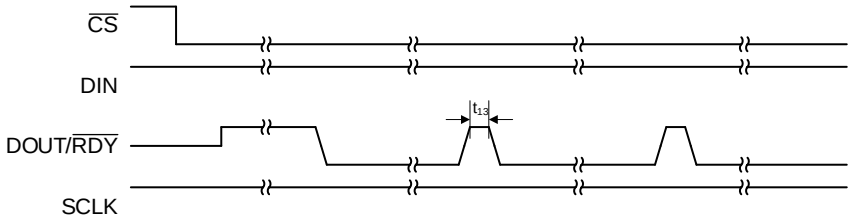


Figure 5: DOUT/RDY High Time when DOUT/RDY is Initially Low and the Next Conversion is Available

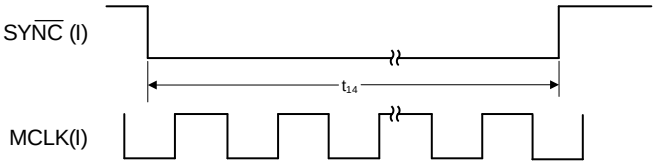


Figure 6: SYNC Pulse Width

7.8 Typical Characteristics

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, AVSS = 0V, external V_{REF} = 2.048V(unless otherwise noted).

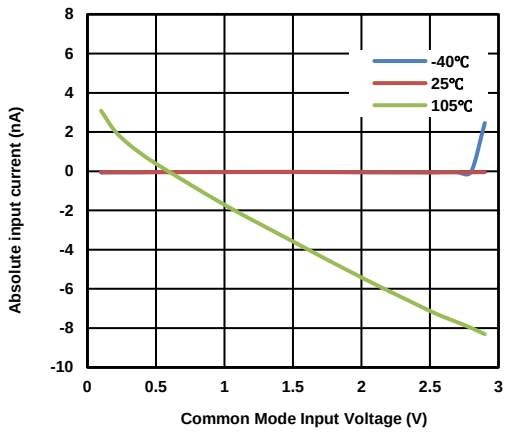


Figure 7: Absolute Input Current vs. Common Mode Input, For All Power Mode

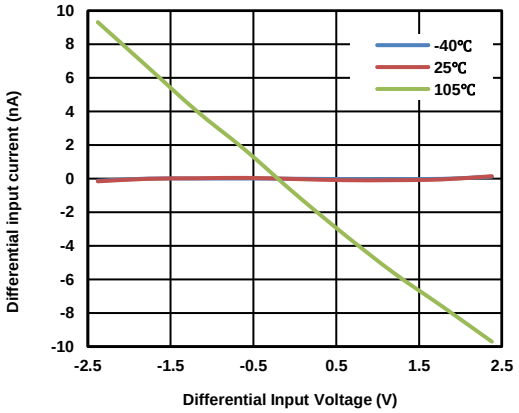


Figure 8:Differential Input Current vs. Input Range , For All Power Mode

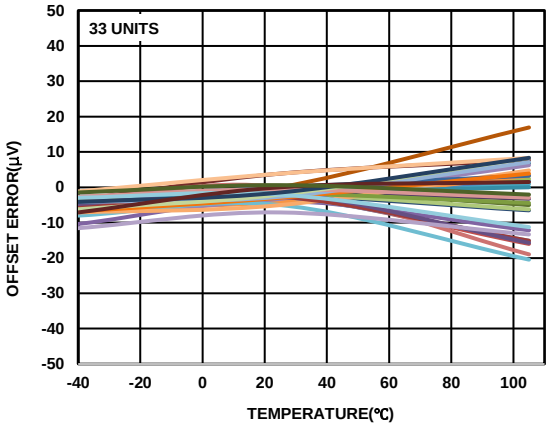


Figure 9: Offset Voltage, PGA=1

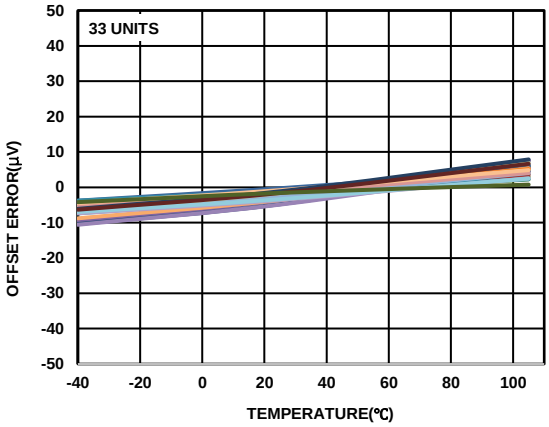


Figure 10: Offset Voltage, PGA=16, Full Power Mode

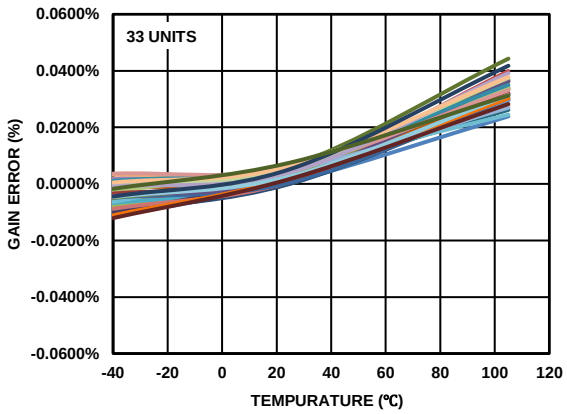


Figure 11: Gain Error G=1, Full Power Mode

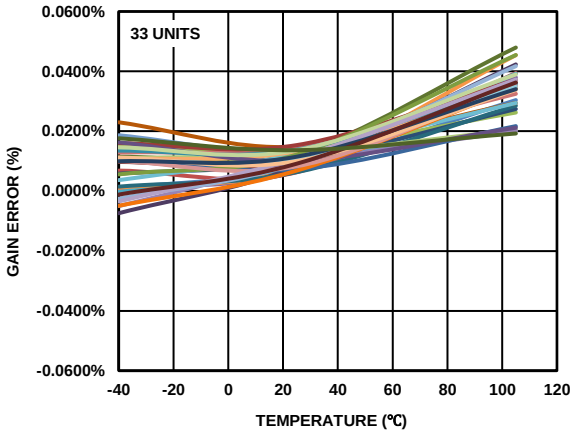


Figure 12: Gain Error G=16, Full Power Mode

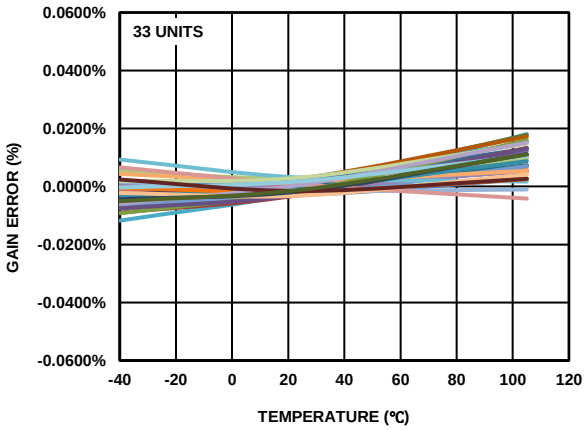


Figure 13: Gain Error G=1, Mid Power Mode

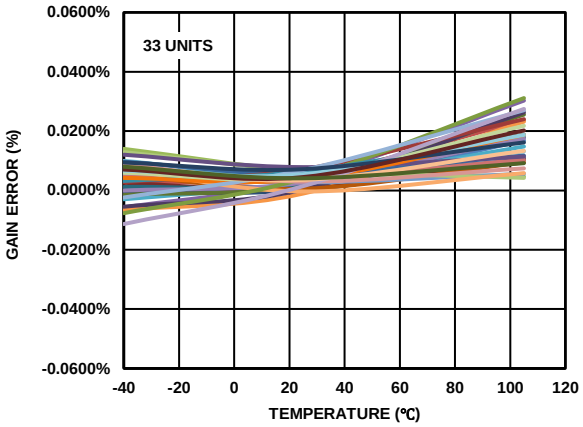


Figure 14: Gain Error G=16, Mid Power Mode

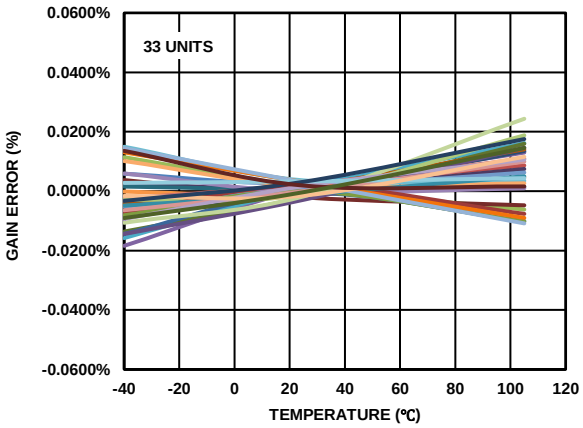


Figure 15: Gain Error G=1, Low Power Mode

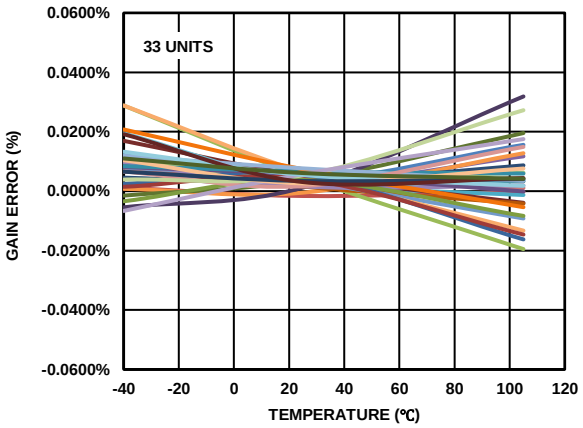


Figure 16: Gain Error G=16, Low Power Mode

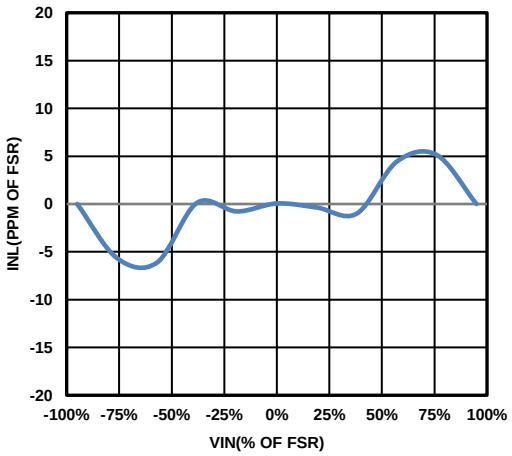


Figure 17: INL Vs Differential Input Signal

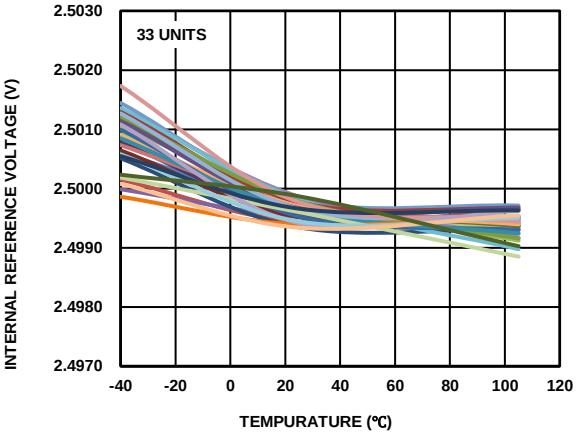


Figure 18: Internal Reference Voltage vs. Temperature

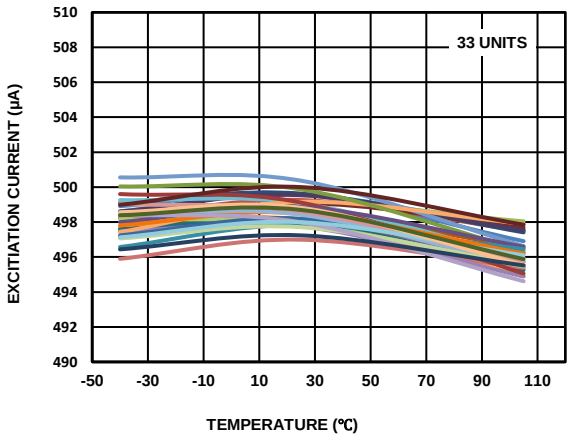


Figure 19: Excitation Current vs. Temperature (500 µA)

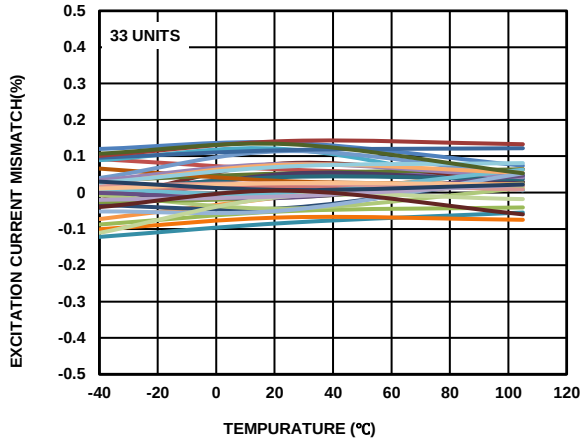


Figure 20: Excitation Current Matching vs. Temperature (500 µA)

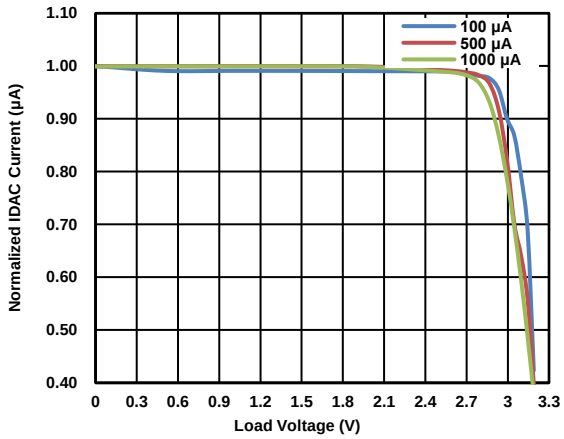


Figure 21: Output Compliance (AVDD = 3.3 V)

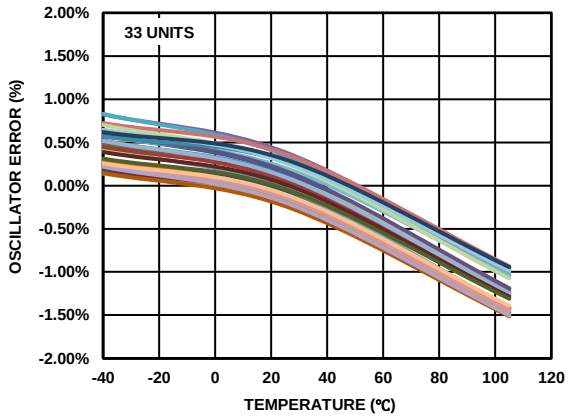


Figure 22: Internal Oscillator Error vs. Temperature

8 Parameter Measurement Information

8.1 Noise Performance

The ADC noise performance is optimized by adjusting the data rate and PGA setting. Generally, the lowest input referred noise is achieved using the highest gain possible, consistent with the input signal range. Do not set the gain too high or the result is ADC overrange. Noise also depends on the output data rate. As the data rate reduces, the ADC bandwidth correspondingly reduces. This reduction in total bandwidth results in lower overall noise. Table 1 to Table 30 summarize the noise performance of the device. The data are representative of typical noise performance at TA = 25°C. The data shown are the result of averaging the readings from multiple devices and were measured with the inputs shorted together. A minimum of 1000 consecutive readings were used to calculate the root mean square (RMS) and peak-to-peak (PP) noise for each reading.
Table 1 to Table 30 list the corresponding data in units of effective resolution and noise free bits, where effective resolution is defined as in Equation 1:

$$Effective\ resolution = In((2 \times V_{REF}/GAIN)/V_{RMS\_Noise})/In(2) \quad (1)$$

Noise free bits is defined as in Equation 2:

$$Noise\ free\ bits = In((2 \times V_{REF}/GAIN)/V_{Peak\_to\_Peak\_Noise})/In(2) \quad (2)$$

FULL POWER MODE At AVDD = 3.3 V, AVSS = 0 V, Internal Reference

SINC4 filter

Table 1: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	PGA SETTING							
				1	2	4	8	16	32	64	128
2047	9.4	2.34	2.16	0.63(4.47)	0.12(0.45)	0.09(0.45)	0.05(0.26)	0.04(0.19)	0.03(0.18)	0.03(0.14)	0.03(0.14)
1920	10	2.5	2.3	0.88(3.58)	0.19(0.89)	0.08(0.37)	0.05(0.22)	0.04(0.22)	0.03(0.16)	0.03(0.15)	0.03(0.16)
960	20	5	4.6	1.31(6.26)	0.32(1.34)	0.11(0.52)	0.06(0.34)	0.05(0.30)	0.04(0.16)	0.04(0.17)	0.04(0.19)
480	40	10	9.2	1.56(7.75)	0.56(2.38)	0.17(0.82)	0.10(0.60)	0.08(0.41)	0.05(0.24)	0.05(0.29)	0.05(0.24)
384	50	12.5	11.5	1.67(8.34)	0.62(2.83)	0.21(1.12)	0.10(0.56)	0.09(0.47)	0.07(0.34)	0.06(0.29)	0.05(0.28)
320	60	15	13.8	1.44(6.26)	0.71(3.28)	0.23(1.12)	0.12(0.75)	0.08(0.35)	0.06(0.37)	0.06(0.30)	0.06(0.27)
240	80	20	18.4	1.67(8.94)	0.72(2.83)	0.28(1.27)	0.13(0.60)	0.11(0.58)	0.07(0.37)	0.08(0.43)	0.07(0.34)
120	160	40	36.8	1.75(9.83)	0.89(4.47)	0.35(1.79)	0.21(1.12)	0.16(0.82)	0.11(0.61)	0.12(0.53)	0.11(0.51)
60	320	80	73.6	2.17(11.03)	1.00(6.26)	0.47(1.94)	0.29(1.53)	0.23(1.23)	0.15(0.80)	0.17(0.90)	0.14(0.75)
30	640	160	147.2	2.13(10.13)	1.45(8.94)	0.76(3.73)	0.34(1.83)	0.26(1.30)	0.24(1.15)	0.23(1.21)	0.19(1.02)
15	1280	320	294.4	2.39(14.90)	1.49(7.15)	0.83(4.40)	0.46(2.27)	0.36(2.25)	0.32(1.59)	0.33(2.06)	0.30(1.40)
8	2400	600	552	2.86(15.80)	2.17(14.45)	1.25(7.75)	0.58(3.39)	0.57(2.79)	0.44(2.42)	0.43(2.07)	0.33(1.86)
4	4800	1200	1104	4.56(21.76)	2.83(13.71)	1.60(7.97)	0.99(5.40)	0.76(4.14)	0.56(2.85)	0.64(2.80)	0.60(2.99)
2	9600	2400	2208	11.62(74.5)	6.56(43.6)	3.11(15.5)	1.80(11.2)	1.31(8.1)	0.93(5.1)	0.74(3.7)	0.87(4.8)
1	19200	4800	4416	130.2(620)	74.7(326.1)	38.1(217.3)	17.5(80.8)	10.1(45.7)	4.7(22.5)	5.0(29.1)	4.3(19.0)

Table 2: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	PGA SETTING							
			1	2	4	8	16	32	64	128
2047	9.4	2.34	22.9(20)	24(22.4)	23.8(21.4)	23.4(21.1)	23(20.6)	22.2(19.7)	21.2(19)	20.4(18.1)
1920	10	2.5	22.4(20.4)	23.6(21.4)	23.9(21.6)	23.5(21.4)	22.7(20.4)	22.3(19.9)	21.3(18.9)	20.4(17.9)
960	20	5	21.8(19.6)	22.9(20.8)	23.4(21.1)	23.2(20.8)	22.5(20)	22(19.9)	20.9(18.7)	19.9(17.6)
480	40	10	21.6(19.3)	22.1(20)	22.8(20.5)	22.5(20)	21.9(19.5)	21.5(19.3)	20.4(18)	19.6(17.3)
384	50	12.5	21.5(19.1)	21.9(19.7)	22.5(20)	22.5(20)	21.7(19.3)	21(18.7)	20.4(18)	19.4(17)
320	60	15	21.7(19.6)	21.7(19.5)	22.3(20)	22.2(19.6)	21.8(19.7)	21.2(18.6)	20.4(18)	19.3(17.1)
240	80	20	21.5(19)	21.7(19.7)	22.1(19.9)	22.1(20)	21.4(19)	21(18.6)	19.9(17.4)	19.1(16.8)
120	160	40	21.4(18.9)	21.4(19)	21.7(19.4)	21.5(19)	20.8(18.5)	20.3(17.9)	19.2(17.1)	18.4(16.2)
60	320	80	21.1(18.7)	21.2(18.6)	21.3(19.3)	21(18.6)	20.3(17.9)	20(17.5)	18.8(16.4)	18.1(15.6)
30	640	160	21.1(18.9)	20.7(18)	20.6(18.3)	20.7(18.3)	20.2(17.8)	19.3(17)	18.4(15.9)	17.6(15.2)
15	1280	320	21(18.3)	20.6(18.4)	20.5(18.1)	20.3(18)	19.7(17)	18.8(16.5)	17.8(15.2)	17(14.7)
8	2400	600	20.7(18.2)	20.1(17.4)	19.9(17.3)	20(17.4)	19(16.7)	18.4(15.9)	17.4(15.2)	16.8(14.3)
4	4800	1200	20(17.8)	19.7(17.4)	19.5(17.2)	19.2(16.8)	18.6(16.2)	18(15.7)	16.9(14.7)	15.9(13.6)
2	9600	2400	18.7(16)	18.5(15.8)	18.6(16.3)	18.4(15.7)	17.8(15.2)	17.3(14.9)	16.6(14.3)	15.4(12.9)
1	19200	4800	15.2(12.9)	15(12.9)	15(12.4)	15.1(12.9)	14.9(12.7)	14.9(12.7)	13.9(11.3)	13.1(11)

SINC3 filter

Table 3: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	PGA SETTING							
				1	2	4	8	16	32	64	128
2047	9.4	3.13	2.56	0.57(2.68)	0.15(0.75)	0.08(0.45)	0.06(0.30)	0.03(0.19)	0.04(0.17)	0.03(0.14)	0.03(0.14)
1920	10	3.33	2.72	0.99(4.17)	0.20(0.89)	0.08(0.37)	0.05(0.22)	0.04(0.24)	0.03(0.14)	0.03(0.14)	0.03(0.17)
1280	15	5	5.44	1.31(6.26)	0.30(1.64)	0.11(0.60)	0.05(0.26)	0.05(0.26)	0.04(0.20)	0.04(0.20)	0.04(0.18)
640	30	10	8.16	1.45(5.96)	0.50(2.24)	0.17(0.82)	0.08(0.37)	0.07(0.37)	0.05(0.25)	0.05(0.27)	0.05(0.25)
384	50	16.67	13.6	1.48(6.85)	0.64(2.53)	0.25(1.34)	0.11(0.52)	0.10(0.50)	0.07(0.33)	0.07(0.36)	0.06(0.31)
320	60	20	16.32	1.55(8.34)	0.68(2.53)	0.27(1.19)	0.14(0.67)	0.09(0.47)	0.08(0.44)	0.06(0.30)	0.06(0.35)
160	120	40	32.64	1.78(8.94)	0.79(3.87)	0.40(1.94)	0.18(0.97)	0.14(0.65)	0.09(0.54)	0.11(0.57)	0.10(0.51)
80	240	80	65.28	2.02(10.43)	0.95(5.07)	0.57(2.76)	0.26(1.42)	0.20(1.01)	0.14(0.74)	0.15(0.68)	0.15(0.78)
40	480	160	130.56	1.97(8.64)	1.14(7.00)	0.67(3.95)	0.39(2.05)	0.25(1.36)	0.19(0.88)	0.20(1.13)	0.19(1.18)
20	960	320	261.12	3.22(22.95)	1.45(8.94)	0.70(4.40)	0.55(2.61)	0.35(1.96)	0.28(1.49)	0.29(1.65)	0.26(1.27)
10	1920	640	522.24	4.28(22.95)	1.99(11.62)	1.24(5.59)	0.86(4.99)	0.59(2.92)	0.45(2.87)	0.44(2.16)	0.38(2.08)
6	3200	1066.67	870.4	13.48(57.5)	7.14(30.70)	3.84(17.88)	1.68(7.23)	0.96(4.17)	0.71(3.59)	0.64(3.46)	0.61(3.73)
3	6400	2133.33	1740.8	101.4(404)	61.0(310)	24.3(126)	12.08(55.1)	5.95(32.50)	3.15(15.13)	3.28(15.82)	3.09(14.24)
2	9600	3200	2611.2	367.8(1899)	163.6(950)	93.3(396)	39.3(189)	23.5(99)	9.0(48)	10.9(50)	11.5(54)
1	19200	6400	5222.4	2683(13052)	1420(8192)	666(3172)	304(1610)	166(926)	86.2(414)	81.0(390)	86.6(469)

Table 4: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Full Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	PGA SETTING							
			1	2	4	8	16	32	64	128
2047	9.4	3.13	23(20.8)	24(21.6)	23.9(21.4)	23.3(21)	23.1(20.6)	22(19.8)	21.3(19)	20.3(18.1)
1920	10	3.33	22.2(20.1)	23.5(21.4)	23.8(21.6)	23.5(21.4)	22.9(20.3)	22.4(20)	21.3(19)	20.3(17.8)
1280	15	5	21.8(19.6)	23(20.5)	23.4(21)	23.4(21.1)	22.5(20.1)	21.9(19.6)	20.8(18.5)	19.9(17.7)
640	30	10	21.7(19.6)	22.2(20)	22.8(20.5)	22.9(20.6)	22(19.6)	21.4(19.2)	20.6(18.1)	19.5(17.2)
384	50	16.67	21.6(19.4)	21.9(19.9)	22.2(19.8)	22.4(20.1)	21.6(19.2)	21.1(18.8)	20.1(17.7)	19.2(16.9)
320	60	20	21.6(19.1)	21.8(19.9)	22.1(20)	22.1(19.8)	21.6(19.3)	20.9(18.4)	20.2(17.9)	19.2(16.7)
160	120	40	21.4(19)	21.6(19.3)	21.5(19.3)	21.7(19.3)	21.1(18.8)	20.6(18.1)	19.3(17)	18.6(16.2)
80	240	80	21.2(18.8)	21.3(18.9)	21(18.7)	21.2(18.7)	20.5(18.2)	20.1(17.7)	19(16.8)	17.9(15.6)
40	480	160	21.2(19.1)	21(18.4)	20.8(18.2)	20.6(18.2)	20.2(17.8)	19.6(17.4)	18.5(16)	17.6(15)
20	960	320	20.5(17.7)	20.7(18)	20.7(18.1)	20.1(17.8)	19.7(17.2)	19.1(16.6)	18(15.5)	17.2(14.9)
10	1920	640	20.1(17.7)	20.2(17.7)	19.9(17.7)	19.4(16.9)	19(16.7)	18.4(15.7)	17.4(15.1)	16.6(14.2)
6	3200	1066.67	18.5(16.4)	18.4(16.3)	18.3(16)	18.5(16.4)	18.3(16.1)	17.7(15.4)	16.8(14.4)	15.9(13.3)
3	6400	2133.33	15.5(13.5)	15.3(12.9)	15.6(13.2)	15.6(13.4)	15.6(13.2)	15.6(13.3)	14.5(12.2)	13.6(11.4)
2	9600	3200	13.7(11.3)	13.9(11.3)	13.7(11.6)	13.9(11.6)	13.7(11.6)	14(11.6)	12.8(10.6)	11.7(9.47)
1	19200	6400	10.8(8.58)	10.7(8.25)	10.8(8.62)	11(8.6)	10.8(8.4)	10.8(8.56)	9.9(7.6)	8.8(6.3)

Post filters

Table 5: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Output Data Rate (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
16.67	2.20(10.73)	0.93(4.77)	0.38(2.01)	0.14(0.71)	0.09(0.45)	0.08(0.47)	0.07(0.36)	0.06(0.31)
20	2.20(9.54)	0.98(5.07)	0.33(1.86)	0.14(0.63)	0.09(0.47)	0.08(0.45)	0.07(0.36)	0.06(0.36)
25	2.20(10.13)	1.01(4.77)	0.38(1.94)	0.17(0.82)	0.10(0.45)	0.07(0.33)	0.08(0.40)	0.07(0.38)
27.27	2.29(11.03)	1.05(5.07)	0.39(2.09)	0.16(0.71)	0.09(0.52)	0.08(0.45)	0.09(0.37)	0.08(0.43)

Table 6: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Output Data Rate (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
16.67	21.1(18.8)	21.3(19)	21.6(19.2)	22(19.7)	21.6(19.4)	20.9(18.3)	20(17.7)	19.3(16.9)
20	21.1(19)	21.2(18.9)	21.8(19.3)	22.1(19.9)	21.7(19.3)	20.9(18.4)	20.1(17.7)	19.2(16.7)
25	21.1(18.9)	21.2(19)	21.6(19.3)	21.8(19.5)	21.5(19.4)	21(18.8)	19.9(17.5)	19.1(16.6)
27.27	21(18.7)	21.1(18.9)	21.6(19.1)	21.9(19.7)	21.7(19.1)	20.8(18.4)	19.8(17.7)	18.9(16.4)

Fast Setting filter(SINC4 + SINC1)

Table 7: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
384	2.63	0.73(2.98)	0.13(0.75)	0.07(0.30)	0.04(0.15)	0.03(0.17)	0.03(0.17)	0.02(0.13)	0.02(0.11)
120	8.42	1.47(5.66)	0.38(1.49)	0.14(0.60)	0.06(0.30)	0.05(0.28)	0.04(0.21)	0.05(0.24)	0.04(0.19)
24	42.11	2.01(11.32)	0.85(4.47)	0.41(1.86)	0.17(0.82)	0.11(0.58)	0.08(0.49)	0.10(0.57)	0.08(0.39)
20	50.53	2.11(9.24)	1.02(4.47)	0.44(2.01)	0.18(0.82)	0.13(0.56)	0.10(0.53)	0.10(0.58)	0.08(0.42)
2	505.26	2.44(16.39)	1.61(7.75)	0.97(6.85)	0.52(2.68)	0.42(1.81)	0.32(1.70)	0.31(1.50)	0.28(1.42)
1	1010.53	7.49(42.62)	4.09(21.31)	2.18(13.34)	1.18(5.85)	0.76(5.18)	0.51(2.56)	0.50(2.98)	0.44(1.92)

Table 8: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
384	2.63	22.7(20.6)	24(21.6)	24(22)	23.9(22)	23.2(20.8)	22.5(19.8)	21.6(19.2)	20.7(18.4)
120	8.42	21.7(19.7)	22.6(20.6)	23.1(21)	23.2(21)	22.4(20)	21.8(19.4)	20.6(18.3)	20(17.6)
24	42.11	21.2(18.7)	21.4(19)	21.5(19.3)	21.8(19.5)	21.4(19)	20.8(18.2)	19.5(17)	18.8(16.6)
20	50.53	21.1(19)	21.2(19)	21.4(19.2)	21.7(19.5)	21.2(19)	20.6(18.1)	19.5(17)	18.8(16.5)
2	505.26	20.9(18.2)	20.5(18.3)	20.3(17.4)	20.1(17.8)	19.5(17.4)	18.8(16.4)	17.9(15.6)	17(14.7)
1	1010.53	19.3(16.8)	19.2(16.8)	19.1(16.5)	19(16.7)	18.6(15.8)	18.2(15.9)	17.2(14.6)	16.4(14.3)

Fast Setting filter(SINC3 + SINC1)

Table 9: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
384	2.78	0.69(3.58)	0.14(0.75)	0.07(0.37)	0.04(0.19)	0.03(0.20)	0.02(0.12)	0.02(0.13)	0.02(0.11)
120	8.89	1.56(6.26)	0.34(1.64)	0.14(0.60)	0.06(0.37)	0.05(0.26)	0.04(0.19)	0.04(0.22)	0.04(0.18)
24	44.44	2.01(8.64)	0.89(3.73)	0.42(1.94)	0.16(0.75)	0.12(0.82)	0.09(0.43)	0.09(0.61)	0.08(0.42)
20	53.33	1.91(7.75)	0.98(4.62)	0.42(2.24)	0.19(0.93)	0.14(0.69)	0.10(0.50)	0.10(0.63)	0.10(0.49)
2	533.33	15.59(87)	8.19(46.49)	4.41(24.36)	1.94(9.72)	0.98(4.66)	0.62(3.24)	0.51(2.71)	0.58(2.95)
1	1066.67	144.5(694)	62.8(256)	29.5(137)	15.7(96.8)	7.2(39.6)	4.2(21.7)	4.0(24.4)	4.3(22.5)

Table 10: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
384	2.78	22.7(20.4)	24(21.6)	24(21.6)	24(21.6)	23.3(20.5)	22.6(20.3)	21.6(19.2)	20.8(18.4)
120	8.89	21.6(19.6)	22.8(20.5)	23(21)	23.2(20.6)	22.5(20.1)	21.8(19.6)	20.7(18.4)	20(17.7)
24	44.44	21.2(19.1)	21.4(19.3)	21.5(19.3)	21.8(19.6)	21.2(18.5)	20.8(18.4)	19.6(16.9)	18.9(16.5)
20	53.33	21.3(19.3)	21.2(19)	21.5(19)	21.6(19.3)	21.1(18.7)	20.5(18.2)	19.5(16.9)	18.6(16.2)
2	533.33	18.2(15.8)	18.2(15.7)	18.1(15.6)	18.2(15.9)	18.2(16)	17.9(15.5)	17.2(14.8)	16(13.6)
1	1066.67	15(12.8)	15.2(13.2)	15.3(13.1)	15.2(12.6)	15.3(12.9)	15.1(12.8)	14.2(11.6)	13.1(10.7)

MID POWER MODE At AVDD = 3.3 V, AVSS = 0 V, Internal Reference

SINC4 filter

Table 11: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), MID Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	PGA SETTING							
				1	2	4	8	16	32	64	128
2047	2.35	0.585	0.54	0.61(3.58)	0.21(1.04)	0.09(0.37)	0.04(0.22)	0.02(0.13)	0.02(0.11)	0.02(0.08)	0.02(0.09)
1920	2.5	0.625	0.575	0.30(1.49)	0.38(1.94)	0.09(0.45)	0.05(0.30)	0.04(0.17)	0.02(0.09)	0.02(0.08)	0.02(0.09)
960	5	1.25	1.15	0.45(2.98)	0.54(2.53)	0.16(0.75)	0.06(0.34)	0.04(0.19)	0.03(0.12)	0.02(0.11)	0.03(0.13)
480	10	2.5	2.3	0.64(2.98)	0.78(4.17)	0.27(1.19)	0.09(0.48)	0.06(0.30)	0.04(0.23)	0.03(0.18)	0.04(0.21)
384	12.5	3.125	2.875	0.73(3.87)	0.88(4.47)	0.32(1.79)	0.11(0.56)	0.06(0.30)	0.04(0.22)	0.04(0.19)	0.04(0.20)
320	15	3.75	3.45	0.80(4.47)	1.02(7.30)	0.35(1.56)	0.14(0.71)	0.07(0.35)	0.04(0.21)	0.04(0.22)	0.04(0.21)
240	20	5	4.6	0.86(5.07)	0.99(5.51)	0.37(2.09)	0.15(0.78)	0.08(0.39)	0.05(0.23)	0.06(0.29)	0.05(0.25)
120	40	10	9.2	1.34(5.96)	1.09(5.36)	0.54(2.68)	0.22(1.01)	0.12(0.60)	0.07(0.36)	0.07(0.40)	0.07(0.34)
60	80	20	18.4	1.69(8.05)	1.19(6.56)	0.68(3.87)	0.35(1.75)	0.19(0.95)	0.10(0.53)	0.11(0.60)	0.10(0.52)
30	160	40	36.8	2.32(12.52)	1.43(7.00)	0.85(4.69)	0.43(2.50)	0.22(1.14)	0.12(0.62)	0.15(0.87)	0.13(0.62)
15	320	80	73.6	4.06(17.88)	2.03(10.43)	0.97(4.54)	0.55(3.32)	0.36(1.83)	0.19(0.93)	0.21(1.16)	0.21(1.20)
8	600	150	138	4.02(24.44)	2.54(12.67)	1.25(6.63)	0.72(3.87)	0.44(2.24)	0.30(1.57)	0.30(1.73)	0.26(1.46)
4	1200	300	276	6.99(32.19)	3.82(28.76)	1.55(6.78)	0.95(4.77)	0.65(3.07)	0.43(2.44)	0.39(2.04)	0.38(1.97)
2	2400	600	552	12.65(60.5)	6.80(36.81)	3.82(19.00)	1.59(8.42)	1.12(5.18)	0.58(3.28)	0.60(2.92)	0.59(2.93)
1	4800	1200	1104	145.3(789)	77.6(333)	36.3(193)	16.0(71.4)	8.1(33.4)	4.9(27.4)	5.2(26.5)	4.5(23.4)

Table 12: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), MID Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	PGA SETTING							
			1	2	4	8	16	32	64	128
2047	2.35	0.585	22.9(20.4)	23.5(21.1)	23.6(21.6)	23.7(21.4)	23.5(21.1)	23.1(20.4)	21.9(19.8)	21.1(18.6)
1920	2.5	0.625	24(21.6)	22.6(20.3)	23.7(21.4)	23.6(21)	23(20.8)	23(20.6)	21.9(19.8)	20.8(18.6)
960	5	1.25	23.4(20.6)	22.1(19.9)	22.8(20.6)	23.2(20.8)	22.9(20.6)	22.4(20.3)	21.5(19.4)	20.5(18.1)
480	10	2.5	22.9(20.6)	21.6(19.1)	22.1(20)	22.6(20.3)	22.3(20)	22(19.3)	21.1(18.7)	19.9(17.5)
384	12.5	3.125	22.7(20.3)	21.4(19)	21.8(19.4)	22.4(20)	22.2(20)	22(19.4)	20.9(18.6)	20(17.5)
320	15	3.75	22.5(20)	21.2(18.3)	21.7(19.6)	22.1(19.7)	22.1(19.7)	21.8(19.4)	20.7(18.4)	19.9(17.4)
240	20	5	22.4(19.9)	21.2(18.7)	21.6(19.1)	21.9(19.6)	21.8(19.6)	21.5(19.3)	20.3(18)	19.7(17.2)
120	40	10	21.8(19.6)	21.1(18.8)	21.1(18.8)	21.4(19.2)	21.3(19)	21(18.7)	20(17.5)	19.1(16.7)
60	80	20	21.5(19.2)	21(18.5)	20.8(18.3)	20.7(18.4)	20.6(18.3)	20.5(18.1)	19.4(17)	18.5(16.2)
30	160	40	21(18.6)	20.7(18.4)	20.4(18)	20.4(17.9)	20.4(18)	20.2(17.9)	18.9(16.4)	18.2(15.9)
15	320	80	20.2(18)	20.2(17.8)	20.2(18)	20.1(17.5)	19.7(17.3)	19.6(17.3)	18.4(16)	17.5(14.9)
8	600	150	20.2(17.6)	19.9(17.5)	19.9(17.5)	19.7(17.3)	19.4(17)	18.9(16.6)	18(15.4)	17.1(14.7)
4	1200	300	19.4(17.2)	19.3(16.4)	19.6(17.4)	19.3(17)	18.8(16.6)	18.4(15.9)	17.6(15.2)	16.6(14.2)
2	2400	600	18.5(16.3)	18.4(16)	18.3(16)	18.5(16.1)	18(15.8)	18(15.5)	16.9(14.7)	16(13.7)
1	4800	1200	15(12.6)	14.9(12.8)	15(12.6)	15.2(13)	15.2(13.1)	14.9(12.4)	13.8(11.5)	13(10.7)

SINC3 filter

Table 13: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), MID Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	PGA SETTING							
				1	2	4	8	16	32	64	128
2047	2.35	0.7825	0.64	0.32(2.09)	0.27(1.19)	0.09(0.52)	0.05(0.26)	0.03(0.15)	0.02(0.11)	0.02(0.09)	0.02(0.09)
1920	2.5	0.8325	0.68	0.23(0.89)	0.41(1.79)	0.10(0.60)	0.05(0.30)	0.04(0.19)	0.02(0.09)	0.02(0.10)	0.02(0.09)
1280	3.75	1.25	1.36	0.38(1.79)	0.52(2.68)	0.14(0.75)	0.05(0.30)	0.04(0.22)	0.02(0.13)	0.02(0.14)	0.02(0.12)
640	7.5	2.5	2.04	0.61(2.68)	0.76(3.28)	0.28(1.42)	0.08(0.45)	0.05(0.28)	0.03(0.18)	0.03(0.20)	0.03(0.20)
384	12.5	4.1675	3.4	0.72(3.87)	0.94(5.07)	0.33(1.71)	0.12(0.56)	0.06(0.32)	0.04(0.20)	0.04(0.20)	0.04(0.19)
320	15	5	4.08	1.59(8.64)	1.01(5.81)	0.38(2.01)	0.15(0.78)	0.09(0.47)	0.04(0.21)	0.04(0.24)	0.04(0.20)
160	30	10	8.16	1.15(5.36)	1.30(6.41)	0.53(2.61)	0.22(1.12)	0.11(0.60)	0.06(0.40)	0.07(0.36)	0.07(0.36)
80	60	20	16.32	1.56(8.05)	1.23(6.41)	0.57(2.76)	0.30(1.53)	0.17(0.82)	0.09(0.47)	0.09(0.61)	0.08(0.40)
40	120	40	32.64	2.56(14.01)	1.67(9.24)	0.86(4.47)	0.33(1.94)	0.24(1.12)	0.13(0.70)	0.12(0.64)	0.13(0.62)
20	240	80	65.28	3.40(23.84)	1.51(9.24)	1.01(5.07)	0.54(3.28)	0.31(1.60)	0.20(0.99)	0.18(1.03)	0.16(0.80)
10	480	160	130.56	4.94(28.31)	3.50(22.95)	1.50(7.53)	0.75(3.73)	0.44(2.53)	0.24(1.35)	0.30(1.68)	0.25(1.44)

6	800	266.6675	217.6	13.60(64.67)	6.61(34.72)	3.35(18.70)	1.99(10.02)	0.90(5.18)	0.47(2.28)	0.51(2.34)	0.47(2.17)
3	1600	533.3325	435.2	91.23(455.3)	43.61(206.6)	25.59(115)	11.86(59.72)	5.52(26.26)	2.94(14.26)	3.09(15.37)	3.23(17.38)
2	2400	800	652.8	348.55(1656)	170.24(829)	78.49(318)	39.68(216)	19.28(91.62)	9.71(51.13)	10.96(49.63)	11.22(65.42)
1	4800	1600	1305.6	2676(14404)	1376(6441)	705(3223)	292(1540)	172(877)	70(366)	79(499)	76(427)

Table 14: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, MID Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	PGA SETTING							
			1	2	4	8	16	32	64	128
2047	2.35	0.7825	23.9(21.1)	23.1(21)	23.6(21.1)	23.5(21.1)	23.2(21)	22.7(20.4)	22(19.7)	20.9(18.6)
1920	2.5	0.8325	24(22.4)	22.5(20.4)	23.6(21)	23.7(21)	23(20.6)	22.9(20.6)	21.9(19.6)	20.9(18.6)
1280	3.75	1.25	23.6(21.4)	22.1(19.8)	23.1(20.6)	23.7(21)	22.8(20.4)	22.5(20.1)	21.5(19)	20.5(18.2)
640	7.5	2.5	22.9(20.8)	21.6(19.5)	22.1(19.7)	22.9(20.4)	22.5(20)	22.1(19.7)	21.1(18.6)	20.1(17.5)
384	12.5	4.1675	22.7(20.3)	21.3(18.9)	21.8(19.4)	22.3(20)	22.2(19.9)	21.7(19.5)	20.9(18.5)	19.8(17.6)
320	15	5	21.5(19.1)	21.2(18.7)	21.6(19.2)	22(19.6)	21.7(19.3)	22(19.4)	20.7(18.3)	19.7(17.5)
160	30	10	22(19.8)	20.8(18.5)	21.1(18.8)	21.4(19)	21.4(19)	21.2(18.5)	20(17.7)	19.1(16.7)
80	60	20	21.6(19.2)	20.9(18.5)	21(18.7)	20.9(18.6)	20.8(18.5)	20.7(18.3)	19.7(16.9)	18.8(16.5)
40	120	40	20.9(18.4)	20.5(18)	20.4(18)	20.8(18.3)	20.3(18)	20.1(17.7)	19.2(16.9)	18.2(15.9)
20	240	80	20.4(17.6)	20.6(18)	20.2(17.9)	20.1(17.5)	19.9(17.5)	19.5(17.2)	18.7(16.2)	17.9(15.5)
10	480	160	19.9(17.4)	19.4(16.7)	19.6(17.3)	19.6(17.3)	19.4(16.9)	19.3(16.8)	18(15.5)	17.2(14.7)
6	800	266.6675	18.4(16.2)	18.5(16.1)	18.5(16)	18.2(15.9)	18.4(15.8)	18.3(16)	17.2(15)	16.3(14.1)
3	1600	533.3325	15.7(13.4)	15.8(13.5)	15.5(13.4)	15.6(13.3)	15.7(13.5)	15.7(13.4)	14.6(12.3)	13.5(11.1)
2	2400	800	13.8(11.5)	13.8(11.5)	13.9(11.9)	13.9(11.4)	13.9(11.7)	13.9(11.5)	12.8(10.6)	11.7(9.22)
1	4800	1600	10.8(8.4)	10.8(8.6)	10.7(8.6)	11(8.6)	10.8(8.4)	11.1(8.7)	9.94(7.2)	9(6.5)

Post filters

Table 15: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), MID Power Mode

Output Data Rate (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
16.67	1.95(10.73)	1.27(6.71)	0.65(3.13)	0.33(1.49)	0.16(0.78)	0.09(0.41)	0.08(0.38)	0.08(0.37)
20	2.77(14.90)	1.31(7.15)	0.66(3.35)	0.33(1.86)	0.15(0.65)	0.10(0.54)	0.10(0.50)	0.09(0.43)
25	1.97(10.43)	1.23(6.56)	0.62(3.13)	0.30(1.42)	0.18(0.93)	0.09(0.39)	0.10(0.53)	0.10(0.58)
27.27	2.44(13.11)	1.29(8.05)	0.68(3.80)	0.36(1.60)	0.19(1.04)	0.10(0.59)	0.11(0.55)	0.09(0.49)

Table 16: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), MID Power Mode

Output Data Rate (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
16.67	21.2(18.8)	20.9(18.5)	20.8(18.6)	20.8(18.6)	20.9(18.6)	20.6(18.5)	19.9(17.6)	18.9(16.6)
20	20.7(18.3)	20.8(18.4)	20.8(18.5)	20.8(18.3)	21(18.8)	20.5(18.1)	19.6(17.2)	18.8(16.4)
25	21.2(18.8)	20.9(18.5)	20.9(18.6)	21(18.7)	20.7(18.3)	20.7(18.6)	19.6(17.1)	18.6(16)
27.27	20.9(18.5)	20.8(18.2)	20.8(18.3)	20.7(18.5)	20.6(18.1)	20.5(18)	19.4(17.1)	18.7(16.2)

Fast Setting filter(SINC4 + SINC1)

Table 17: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), MID Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.63	0.44(2.38)	0.67(3.28)	0.18(0.97)	0.06(0.34)	0.04(0.22)	0.03(0.14)	0.03(0.16)	0.03(0.15)
30	8.42	0.90(4.77)	1.01(4.92)	0.42(2.38)	0.16(0.78)	0.08(0.41)	0.05(0.26)	0.06(0.29)	0.05(0.24)
6	42.11	1.65(9.83)	1.27(7.00)	0.67(3.28)	0.34(1.64)	0.21(1.08)	0.12(0.64)	0.10(0.57)	0.12(0.74)
5	50.53	2.03(10.43)	1.41(7.75)	0.75(4.40)	0.42(1.97)	0.20(1.06)	0.13(0.55)	0.13(0.62)	0.12(0.66)
2	126.32	3.87(21.16)	2.06(9.69)	0.99(6.41)	0.51(2.57)	0.32(1.56)	0.19(1.10)	0.20(1.12)	0.20(1.05)
1	252.63	8.48(42.92)	4.78(25.03)	2.29(11.85)	1.11(6.00)	0.64(3.37)	0.38(1.70)	0.35(1.97)	0.31(1.61)

Table 18: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), MID Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.63	23.4(21)	21.8(19.5)	22.7(20.3)	23.2(20.8)	22.8(20.4)	22.3(20)	21.5(18.9)	20.3(17.9)
30	8.42	22.4(20)	21.2(18.9)	21.4(19)	21.8(19.6)	21.8(19.5)	21.6(19.1)	20.4(18)	19.6(17.3)

6	42.11	21.5(18.9)	20.9(18.4)	20.8(18.5)	20.8(18.5)	20.5(18.1)	20.3(17.8)	19.5(17)	18.3(15.6)
5	50.53	21.2(18.8)	20.7(18.3)	20.6(18.1)	20.5(18.2)	20.5(18.1)	20.1(18.1)	19.2(16.9)	18.3(15.8)
2	126.32	20.3(17.8)	20.2(17.9)	20.2(17.5)	20.2(17.8)	19.8(17.6)	19.6(17.1)	18.5(16)	17.6(15.1)
1	252.63	19.1(16.8)	19(16.6)	19(16.6)	19.1(16.6)	18.9(16.5)	18.6(16.4)	17.7(15.2)	16.9(14.5)

Fast Setting filter(SINC3 + SINC1)

Table 19: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), MID Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.78	0.47(2.68)	0.63(2.98)	0.16(0.97)	0.07(0.37)	0.05(0.22)	0.03(0.14)	0.03(0.14)	0.03(0.15)
30	8.89	0.97(4.47)	0.97(5.07)	0.40(2.24)	0.17(0.78)	0.08(0.41)	0.05(0.24)	0.05(0.21)	0.05(0.26)
6	44.44	1.96(11.62)	1.48(7.75)	0.72(4.54)	0.38(1.90)	0.19(0.89)	0.11(0.77)	0.10(0.44)	0.12(0.56)
5	53.33	2.29(11.03)	1.60(9.24)	0.83(4.32)	0.44(1.97)	0.23(1.12)	0.13(0.77)	0.14(0.63)	0.13(0.71)
2	133.33	18.16(84)	8.32(45.75)	3.79(17.66)	1.91(9.02)	1.06(5.77)	0.53(2.54)	0.57(2.97)	0.60(3.19)
1	266.67	130.83(708)	68.66(324)	31.67(174)	17.53(78.2)	8.10(39.8)	3.86(17.6)	3.66(23.3)	4.06(21.4)

Table 20: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), MID Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.78	23.3(20.8)	21.9(19.6)	22.8(20.3)	23(20.6)	22.6(20.4)	22.4(20)	21.5(19)	20.4(17.9)
30	8.89	22.3(20)	21.3(18.9)	21.5(19)	21.8(19.6)	21.8(19.5)	21.5(19.3)	20.6(18.5)	19.6(17.2)
6	44.44	21.2(18.7)	20.6(18.3)	20.7(18)	20.6(18.3)	20.6(18.4)	20.3(17.6)	19.5(17.4)	18.3(16)
5	53.33	21(18.7)	20.5(18)	20.5(18.1)	20.4(18.2)	20.4(18)	20.2(17.6)	19.1(16.9)	18.2(15.7)
2	133.33	18(15.8)	18.2(15.7)	18.3(16.1)	18.3(16)	18.1(15.7)	18.1(15.9)	17(14.6)	16(13.5)
1	266.67	15.2(12.7)	15.1(12.9)	15.2(12.8)	15.1(12.9)	15.2(12.9)	15.3(13.1)	14.3(11.7)	13.2(10.8)

LOW POWER MODE At AVDD = 3.3 V, AVSS = 0 V, Internal Reference

SINC4 filter

Table 21: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), LOW Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	PGA SETTING							
				1	2	4	8	16	32	64	128
2047	1.175	0.2925	0.27	0.47(3.28)	1.17(4.02)	0.11(0.60)	0.06(0.34)	0.04(0.19)	0.03(0.16)	0.03(0.16)	0.02(0.13)
1920	1.25	0.3125	0.2875	0.46(3.87)	2.13(7.45)	0.12(0.67)	0.06(0.30)	0.04(0.15)	0.03(0.16)	0.03(0.13)	0.03(0.12)
960	2.5	0.625	0.575	1.64(11.92)	2.80(9.09)	0.25(1.19)	0.08(0.45)	0.05(0.28)	0.03(0.17)	0.03(0.15)	0.03(0.17)
480	5	1.25	1.15	0.87(5.07)	3.16(10.43)	0.93(3.58)	0.12(0.63)	0.06(0.32)	0.05(0.20)	0.04(0.23)	0.04(0.19)
384	6.25	1.5625	1.4375	1.29(5.96)	3.18(10.43)	1.07(4.02)	0.19(0.82)	0.07(0.41)	0.06(0.28)	0.05(0.34)	0.05(0.26)
320	7.5	1.875	1.725	1.35(6.26)	3.18(10.73)	1.19(4.54)	0.28(1.30)	0.07(0.32)	0.05(0.27)	0.06(0.27)	0.05(0.28)
240	10	2.5	2.3	1.24(6.56)	3.31(11.77)	1.29(5.22)	0.40(1.64)	0.09(0.39)	0.07(0.41)	0.07(0.33)	0.06(0.32)
120	20	5	4.6	4.11(19.37)	3.29(10.88)	1.50(5.29)	0.59(2.50)	0.20(0.91)	0.09(0.45)	0.09(0.54)	0.07(0.34)
60	40	10	9.2	2.13(10.43)	3.62(13.11)	1.57(6.63)	0.74(3.02)	0.34(1.53)	0.13(0.60)	0.16(0.85)	0.13(0.64)
30	80	20	18.4	2.84(16.69)	3.73(14.31)	1.68(7.45)	0.81(3.54)	0.41(1.92)	0.22(0.93)	0.22(0.96)	0.20(0.98)
15	160	40	36.8	3.42(19.67)	3.10(15.20)	1.77(9.16)	0.87(4.40)	0.52(2.66)	0.31(1.73)	0.27(1.45)	0.28(1.37)
8	300	75	69	5.09(27.12)	2.36(9.98)	2.12(10.21)	0.94(4.32)	0.60(3.67)	0.37(1.97)	0.34(1.88)	0.32(1.63)
4	600	150	138	6.25(34.87)	3.52(17.58)	2.12(10.65)	1.40(6.71)	0.74(3.76)	0.53(2.64)	0.39(2.03)	0.45(2.27)
2	1200	300	276	10.74(50.6)	7.00(46.94)	3.56(18.40)	2.10(10.21)	1.20(6.33)	0.69(4.00)	0.75(3.38)	0.67(3.60)
1	2400	600	552	149.19(699)	68.68(329)	31.78(152)	19.69(107)	8.29(39.67)	4.80(22.86)	4.55(23.79)	4.06(17.80)

Table 22: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), LOW Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	PGA SETTING							
			1	2	4	8	16	32	64	128
2047	1.175	0.2925	23.3(20.5)	21(19.2)	23.4(21)	23.2(20.8)	22.9(20.6)	22.2(19.9)	21.4(18.8)	20.6(18.2)
1920	1.25	0.3125	23.3(20.3)	20.1(18.3)	23.2(20.8)	23.3(21)	23(21)	22.3(19.9)	21.5(19.2)	20.5(18.3)
960	2.5	0.625	21.5(18.6)	19.7(18)	22.2(20)	22.8(20.4)	22.5(20)	22.1(19.8)	21.2(19)	20.3(17.7)
480	5	1.25	22.4(19.9)	19.5(17.8)	20.3(18.4)	22.2(19.9)	22.3(19.9)	21.7(19.5)	20.9(18.3)	19.9(17.6)
384	6.25	1.5625	21.8(19.6)	19.5(17.8)	20.1(18.2)	21.6(19.5)	22(19.5)	21.3(19)	20.4(17.8)	19.6(17.2)
320	7.5	1.875	21.8(19.6)	19.5(17.8)	20(18)	21.1(18.8)	21.9(19.9)	21.5(19.1)	20.3(18.1)	19.6(17)
240	10	2.5	21.9(19.5)	19.5(17.7)	19.8(17.8)	20.5(18.5)	21.7(19.6)	21.1(18.5)	20.1(17.8)	19.3(16.8)
120	20	5	20.2(17.9)	19.5(17.8)	19.6(17.8)	20(17.9)	20.5(18.3)	20.7(18.4)	19.6(17.1)	19(16.7)
60	40	10	21.1(18.8)	19.4(17.5)	19.6(17.5)	19.6(17.6)	19.7(17.6)	20.1(18)	18.9(16.4)	18.2(15.8)
30	80	20	20.7(18.1)	19.3(17.4)	19.5(17.3)	19.5(17.4)	19.5(17.3)	19.4(17.3)	18.4(16.3)	17.5(15.2)
15	160	40	20.4(17.9)	19.6(17.3)	19.4(17)	19.4(17.1)	19.1(16.8)	18.9(16.4)	18.1(15.7)	17.1(14.8)
8	300	75	19.9(17.4)	20(17.9)	19.1(16.9)	19.3(17.1)	19(16.3)	18.7(16.2)	17.8(15.3)	16.8(14.5)
4	600	150	19.6(17.1)	19.4(17.1)	19.1(16.8)	18.7(16.5)	18.6(16.3)	18.1(15.8)	17.6(15.2)	16.4(14)
2	1200	300	18.8(16.5)	18.4(15.7)	18.4(16)	18.1(15.9)	17.9(15.5)	17.8(15.2)	16.6(14.5)	15.8(13.4)
1	2400	600	15(12.8)	15.1(12.8)	15.2(13)	14.9(12.5)	15.2(12.9)	14.9(12.7)	14(11.6)	13.2(11.1)

SINC3 filter

Table 23: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), LOW Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	f_{3dB} (Hz)	PGA SETTING							
				1	2	4	8	16	32	64	128
2047	1.18	0.39	0.32	0.55(3.87)	1.44(5.07)	0.10(0.52)	0.07(0.30)	0.04(0.22)	0.03(0.12)	0.07(0.33)	0.03(0.17)
1920	1.25	0.42	0.34	0.54(3.87)	2.21(7.60)	0.12(0.60)	0.06(0.26)	0.05(0.28)	0.03(0.14)	0.05(0.22)	0.03(0.19)
1280	1.88	0.63	0.68	0.73(4.47)	2.64(9.39)	0.18(0.89)	0.07(0.41)	0.04(0.26)	0.03(0.18)	0.04(0.18)	0.04(0.19)
640	3.75	1.25	1.02	1.12(6.26)	3.02(10.43)	0.78(2.98)	0.11(0.63)	0.06(0.32)	0.04(0.23)	0.04(0.23)	0.04(0.20)
384	6.25	2.08	1.70	1.38(7.15)	3.14(10.58)	1.14(4.02)	0.24(1.04)	0.08(0.41)	0.05(0.31)	0.05(0.22)	0.05(0.27)
320	7.50	2.50	2.04	1.56(7.75)	3.20(11.03)	1.21(4.25)	0.33(1.38)	0.09(0.60)	0.05(0.28)	0.06(0.34)	0.06(0.30)
160	15.00	5.00	4.08	1.78(7.15)	3.14(11.92)	1.42(5.22)	0.58(2.31)	0.18(0.84)	0.08(0.43)	0.09(0.40)	0.08(0.37)
80	30.00	10.00	8.16	1.74(9.54)	3.46(13.86)	1.66(6.56)	0.63(2.53)	0.31(1.27)	0.12(0.61)	0.12(0.54)	0.11(0.49)
40	60.00	20.00	16.32	2.43(15.80)	3.16(15.05)	1.72(7.30)	0.81(3.65)	0.46(1.90)	0.21(1.05)	0.20(1.17)	0.18(0.75)
20	120.00	40.00	32.64	3.42(20.56)	3.05(15.05)	1.95(9.24)	0.86(3.99)	0.46(2.55)	0.27(1.42)	0.29(1.37)	0.25(1.33)
10	240.00	80.00	65.28	5.25(24.44)	3.18(15.05)	2.39(12.14)	1.27(6.26)	0.64(3.09)	0.35(1.82)	0.34(1.88)	0.34(1.99)

6	400.00	133.33	108.80	14.51(70.93)	6.68(35.46)	3.83(21.98)	1.76(8.87)	0.96(4.88)	0.68(3.50)	0.64(2.94)	0.56(2.58)
3	800.00	266.67	217.60	92.71(503)	42.98(234)	25.66(140)	11.99(58.64)	5.84(27.51)	2.93(15.31)	3.32(16.87)	2.99(13.55)
2	1200.00	400.00	326.40	360.18(1721)	163.34(694)	83.31(377)	45.51(221)	19.36(113)	10.59(50.20)	11.21(62.20)	12.45(66.69)
1	2400.00	800.00	652.80	2547(12822)	1222(6035)	741(3451)	297(1846)	164(862)	62.96(401)	78.74(371)	65.90(401)

Table 24: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, LOW Power Mode

Filter Word	DATA RATE (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	PGA SETTING							
			1	2	4	8	16	32	64	128
2047	1.18	0.39	23.1(20.3)	20.7(18.9)	23.5(21.1)	23.1(21)	22.9(20.4)	22.4(20.3)	20.1(17.8)	20.3(17.8)
1920	1.25	0.42	23.1(20.3)	20.1(18.3)	23.2(21)	23.4(21.1)	22.5(20)	22.4(20)	20.4(18.4)	20.1(17.6)
1280	1.88	0.63	22.7(20)	19.8(18)	22.7(20.4)	23(20.5)	22.7(20.1)	22.2(19.7)	20.8(18.7)	20(17.6)
640	3.75	1.25	22(19.6)	19.6(17.8)	20.6(18.6)	22.4(19.9)	22.3(19.9)	21.7(19.3)	20.7(18.3)	19.7(17.5)
384	6.25	2.08	21.7(19.4)	19.6(17.8)	20(18.2)	21.3(19.1)	21.8(19.5)	21.4(18.9)	20.6(18.4)	19.5(17.1)
320	7.50	2.50	21.6(19.3)	19.5(17.7)	19.9(18.1)	20.8(18.7)	21.6(19)	21.5(19)	20.3(17.7)	19.4(16.9)
160	15.00	5.00	21.4(19.4)	19.6(17.6)	19.7(17.8)	20(18)	20.7(18.5)	20.8(18.4)	19.7(17.5)	18.9(16.6)
80	30.00	10.00	21.4(19)	19.4(17.4)	19.5(17.5)	19.9(17.9)	19.9(17.9)	20.2(17.9)	19.3(17.1)	18.4(16.2)
40	60.00	20.00	20.9(18.2)	19.5(17.3)	19.4(17.3)	19.5(17.3)	19.3(17.3)	19.5(17.1)	18.5(16)	17.7(15.6)
20	120.00	40.00	20.4(17.8)	19.6(17.3)	19.2(17)	19.4(17.2)	19.3(16.9)	19.1(16.7)	18(15.8)	17.2(14.8)
10	240.00	80.00	19.8(17.6)	19.5(17.3)	19(16.6)	18.9(16.6)	18.8(16.6)	18.7(16.3)	17.8(15.3)	16.8(14.2)
6	400.00	133.33	18.3(16.1)	18.5(16.1)	18.3(15.8)	18.4(16.1)	18.3(15.9)	17.8(15.4)	16.9(14.7)	16(13.8)
3	800.00	266.67	15.7(13.2)	15.8(13.3)	15.5(13.1)	15.6(13.3)	15.7(13.4)	15.7(13.3)	14.5(12.1)	13.6(11.4)
2	1200.00	400.00	13.7(11.5)	13.9(11.8)	13.8(11.6)	13.7(11.4)	13.9(11.4)	13.8(11.6)	12.7(10.2)	11.6(9.19)
1	2400.00	800.00	10.9(8.6)	11(8.6)	10.7(8.5)	11(8.4)	10.8(8.5)	11.2(8.6)	9.9(7.7)	9.2(6.6)

Post filters

Table 25: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), LOW Power Mode

Output Data Rate (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
16.67	3.30(16.09)	4.76(17.88)	1.95(9.39)	0.90(4.14)	0.40(2.01)	0.18(0.84)	0.17(0.88)	0.16(0.82)
20	8.45(44.11)	5.72(25.48)	2.67(14.75)	1.30(6.18)	0.71(3.87)	0.31(1.60)	0.34(2.24)	0.28(1.48)
25	3.31(20.27)	4.83(18.33)	1.96(9.46)	0.86(4.25)	0.45(2.25)	0.21(1.07)	0.21(1.06)	0.21(1.02)
27.27	3.51(19.67)	4.56(18.03)	1.99(9.61)	0.94(4.25)	0.45(2.40)	0.22(1.13)	0.19(0.96)	0.18(1.05)

Table 26: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), LOW Power Mode

Output Data Rate (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
16.67	20.5(18.2)	19(17)	19.2(17)	19.4(17.2)	19.5(17.2)	19.7(17.5)	18.7(16.4)	17.8(15.5)
20	19.1(16.7)	18.7(16.5)	18.8(16.3)	18.8(16.6)	18.7(16.3)	18.9(16.5)	17.8(15)	17(14.6)
25	20.5(17.9)	18.9(17)	19.2(17)	19.4(17.1)	19.4(17)	19.5(17.1)	18.5(16.1)	17.5(15.2)
27.27	20.4(17.9)	19(17)	19.2(16.9)	19.3(17.1)	19.4(16.9)	19.4(17)	18.6(16.3)	17.7(15.1)

Fast Setting filter(SINC4 + SINC1)

Table 27: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), LOW Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.27	1.15(7.15)	3.49(12.22)	1.05(3.80)	0.15(0.71)	0.08(0.41)	0.05(0.27)	0.05(0.25)	0.04(0.26)
30	7.27	2.33(9.83)	3.83(14.01)	1.56(5.66)	0.61(2.72)	0.19(0.89)	0.09(0.50)	0.10(0.52)	0.08(0.39)
6	36.36	3.12(20.56)	4.16(16.09)	1.91(8.94)	0.98(4.58)	0.48(2.07)	0.25(1.31)	0.24(1.14)	0.25(1.16)
5	43.64	3.49(19.07)	4.16(18.63)	1.89(8.27)	0.97(4.88)	0.52(2.51)	0.26(1.68)	0.25(1.26)	0.22(1.20)
2	109.1	4.49(23.25)	3.84(19.37)	2.07(10.36)	1.22(5.03)	0.62(3.41)	0.35(1.63)	0.34(1.97)	0.32(1.92)
1	218.18	17.41(92.3)	7.55(43.06)	4.68(22.50)	2.14(11.21)	1.18(6.35)	0.63(3.85)	0.68(3.39)	0.63(3.60)

Table 28: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), LOW Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.27	22(19.4)	19.4(17.6)	20.1(18.3)	22(19.7)	21.9(19.5)	21.6(19.1)	20.6(18.2)	19.7(17.1)
30	7.27	21(18.9)	19.3(17.4)	19.6(17.7)	19.9(17.8)	20.6(18.4)	20.6(18.2)	19.6(17.1)	18.8(16.6)
6	36.36	20.6(17.8)	19.2(17.2)	19.3(17)	19.2(17)	19.3(17.2)	19.2(16.8)	18.2(16)	17.2(15)
5	43.64	20.4(18)	19.2(17)	19.3(17.2)	19.3(16.9)	19.1(16.9)	19.2(16.5)	18.2(15.9)	17.4(14.9)

2	109.1	20(17.7)	19.3(16.9)	19.2(16.8)	18.9(16.9)	18.9(16.4)	18.7(16.5)	17.8(15.2)	16.9(14.3)
1	218.18	18.1(15.7)	18.3(15.8)	18(15.7)	18.1(15.7)	18(15.5)	17.9(15.3)	16.8(14.4)	15.9(13.4)

Fast Setting filter(SINC3 + SINC1)

Table 29: RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), LOW Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.5	1.10(6.85)	3.45(11.03)	1.04(3.80)	0.14(0.75)	0.08(0.45)	0.05(0.23)	0.05(0.23)	0.05(0.25)
30	8	1.68(8.34)	3.63(13.41)	1.58(6.85)	0.63(2.50)	0.18(0.89)	0.10(0.43)	0.10(0.44)	0.08(0.43)
6	40	3.76(19.37)	4.35(20.41)	2.05(9.31)	0.88(4.02)	0.47(2.38)	0.24(1.38)	0.24(0.95)	0.25(1.44)
5	48	3.87(23.25)	4.74(21.90)	2.04(9.31)	0.96(4.58)	0.53(2.68)	0.28(1.35)	0.26(1.31)	0.24(1.25)
2	120	32.33(137)	15.77(83.8)	8.84(44.18)	4.43(23.21)	2.00(9.91)	1.06(5.90)	1.04(4.40)	1.07(5.25)
1	240	255.4(1244)	126.8(694)	65.0(347.6)	34.1(173.8)	15.73(82.3)	7.40(38.20)	8.48(44.95)	9.52(47.21)

Table 30: Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), LOW Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	PGA SETTING							
		1	2	4	8	16	32	64	128
96	2.5	22.1(19.4)	19.4(17.7)	20.2(18.3)	22(19.6)	21.9(19.4)	21.6(19.3)	20.5(18.3)	19.7(17.2)
30	8	21.5(19.1)	19.3(17.5)	19.5(17.4)	19.9(17.9)	20.7(18.4)	20.6(18.4)	19.6(17.4)	18.8(16.4)
6	40	20.3(17.9)	19.1(16.9)	19.2(17)	19.4(17.2)	19.3(17)	19.3(16.7)	18.2(16.3)	17.2(14.7)
5	48	20.3(17.7)	19(16.8)	19.2(17)	19.3(17)	19.1(16.8)	19(16.8)	18.1(15.8)	17.3(14.9)
2	120	17.2(15.1)	17.2(14.8)	17.1(14.7)	17.1(14.7)	17.2(14.9)	17.1(14.6)	16.2(14.1)	15.1(12.8)
1	240	14.2(11.9)	14.2(11.8)	14.2(11.8)	14.1(11.8)	14.2(11.8)	14.3(12)	13.1(10.7)	12(9.6)

9 Detailed Description

9.1 Overview

The AD7124-8B is a low power ADC that incorporates a Σ-Δ modulator, buffer, reference, gain stage, and on-chip digital filtering, which is intended for the measurement of wide dynamic ranges, low frequency signals (such as those in pressure transducers), weigh scales, and temperature measurement applications.

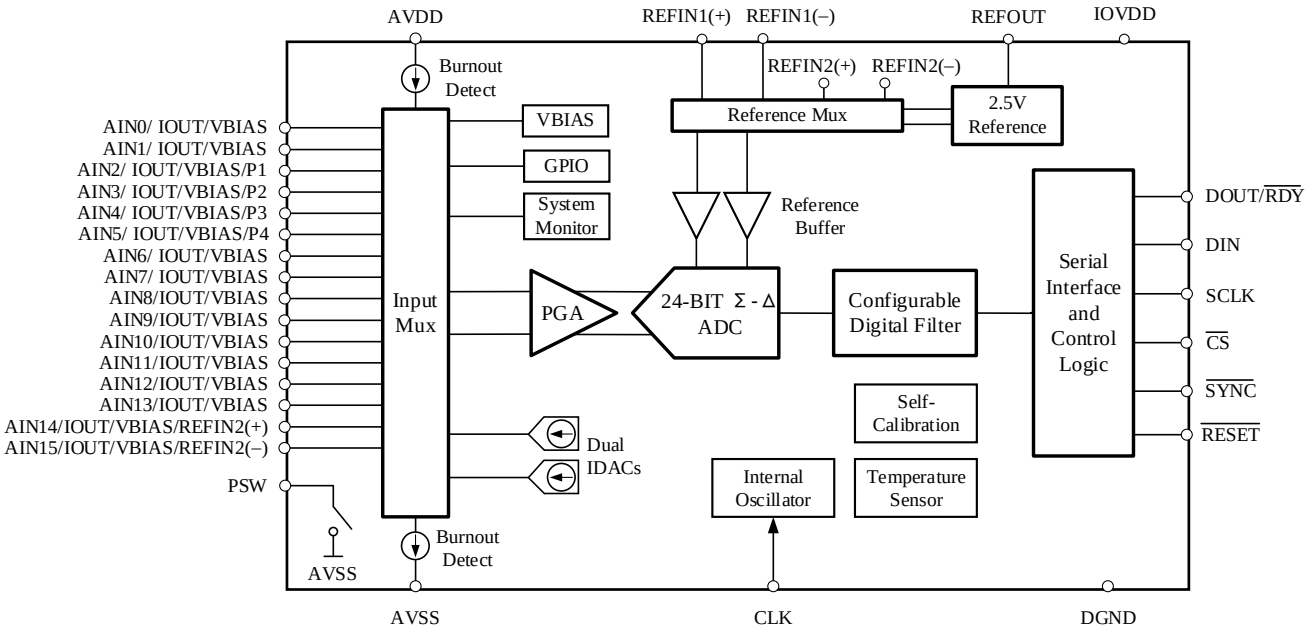


Figure 23: Block Diagrams for AD7124

9.2 Feather Description

9.2.1 Power Modes

The AD7124 offers three power modes: high power mode, mid power mode, and low power mode. This allows the user total flexibility in terms of speed, rms noise, and current consumption.

9.2.2 Analog Inputs

The device can have 8 differential or 15 pseudo differential analog inputs. The analog inputs can be buffered or unbuffered. The AD7124-8B uses flexible multiplexing; thus, any analog input pin can be selected as a positive input (AINP) and any analog input pin can be selected as a negative input (AINM).

9.2.3 Multiplexer

The on-chip multiplexer increases the channel count of the device. Because the multiplexer is included on chip, any channel changes are synchronized with the conversion process.

9.2.4 Reference

AD7124-8B contains a 2.5 V reference, which has a drift of 15 ppm/°C maximum. Reference buffers are also included on chip, which can be used with the internal reference and externally applied references.

9.2.5 Programmable Gain Array (PGA)

The analog input signal can be amplified using the PGA. The PGA allows gains of 1, 2, 4, 8, 16, 32, 64, and 128.

9.2.6 Burnout Currents

Two burnout currents, which can be programmed to 500 nA, 2 µA, or 4 µA, are included on chip to detect the presence of the external sensor.

9.2.7 Σ-Δ ADC and Filter

The AD7124-8 contains a fourth -order Σ-Δ modulator followed by a digital filter. The device has the following filter options:

- $Sinc^4$
- $Sinc^3$
- Fast filter
- Post filter
- Zero latency

9.2.8 Channel Sequencer

The AD7124 allows up to 16 configurations, or channels. These channels can consist of analog inputs, reference inputs, or power supplies such that diagnostic functions, such as power supply monitoring, can be interleaved with conversions. The sequencer automatically converts all enabled channels. When each enabled channel is selected, the time required to generate the conversion is equal to the settling time for the selected channel.

9.2.9 Per Channel Configuration

The AD7124-8 allows up to eight different setups, each setup consisting of a gain, output data rate, filter type, and a refer ence source. Each channel is then linked to a setup.

9.2.10 Serial Interface

The AD7124-8 has a 3 -wire or 4-wire SPI. The on-chip registers are accessed via the serial interface.

9.2.11 Clock

The device has an internal 614.4 kHz clock. Use either this clock or an external clock as the clock source for the device. The internal clock can also be made available on a pin if a clock source is required for external circuitry.

9.2.12 Temperature Sensor

The on-chip temperature sensor monitors the die temperature.

9.2.13 Digital Outputs

The AD7124-8 has four general -purpose digital outputs. These can be used for driving external circuitry. For example, an external multiplexer can be controlled by these outputs.

9.2.14 Calibration

Both internal calibration and system calibration are included on chip; therefore, the user has the option of removing offset or gain errors internal to the device only or removing the offset or gain errors of the complete end system.

9.2.15 Excitation Currents

The device contains two excitation currents that can be set independently to 10 µA, 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, or 1 mA.

9.2.16 Bias Voltage

A bias voltage generator is included on chip so that signals from thermocouples can be biased suitably. The bias voltage is set to (AVDD − AVSS)/2 and can be made available on any input. It can supply multiple channels.

9.2.17 Bridge Power Switch (PSW)

A low-side power switch allows the user to power down bridges that are interfaced to the ADC.

9.2.18 Diagnostics

The AD7124 includes numerous diagnostics features such as

- CRC on SPI communications
- CRC on the memory map
- SPI read/write checks

These diagnostics allow a high level of fault coverage in an application.

9.2.19 POWER SUPPLIES

The AD7124-8 operates with an analog power supply voltage from 2.7 V to 5.25 V in all power mode. The device accepts a digital power supply from 2.7 V to 5.25 V.
The device has two independent power supply pins: AVDD and IOVDD.

- AVDD is referred to AVSS. AVDD powers the internal analog regulator that supplies the ADC.
- IOVDD is referred to DGND. This supply sets the interface logic levels on the SPI interface and powers an internal regulator for operation of the digital processing.

9.2.20 Single Supply Operation (AV_{SS} = DGND)

When the AD7124 is powered from a single supply that is connected to AVDD, AVSS and DGND can be shorted together on one single ground plane. With this setup, an external level shifting circuit is required when using truly bipolar inputs to shift the common-mode voltage.

9.2.21 Split Supply Operation ($AV_{SS} \neq$ DGND)

The AD7124-8 can operate with AV_{SS} set to a negative voltage, allowing true bipolar inputs to be applied. This allows a truly fully differential input signal centered around 0 V to be applied to the AD7124-8 without the need for an external level shifting circuit. For example, with a 5.0 V split supply, AVDD = +2.5 V and AVSS = −2.5 V. In this use case, the AD7124-8 internally level shifts the signals, allowing the digital output to function between DGND (nominally 0 V) and IOVDD.
When using a split supply for AV_{DD} and AV_{SS}, the absolute maximum ratings must be considered (see the Absolute Maximum Ratings section). Ensure that IOV_{DD} is set below 5.25 V to stay within the absolute maximum ratings for the device.

9.3 DIGITAL COMMUNICATION

The AD7124-8 has a 3-wire or 4-wire SPI interface that is compatible with QSPI, MICROWIRE, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

Figure 24: SPI Mode 3, SCLK Edges

9.3.1 Accessing the ADC Register Map

The communications register controls access to the full register map of the ADC. This register is an 8-bit, write only register. On power-up or after a reset, the digital interface defaults to a state where it expects a write to the communications register; therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is accessed and if the next operation is a read or write. The register address bits (Bit 5 to Bit 0) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its default state, where it expects a write operation to the communications register.

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is used with the digital interface, returning $\overline{CS}$ high resets the digital interface to its default state and aborts any current operation.

Figure 25 and Figure 26 illustrate writing to and reading from a register by first writing the 8-bit command to the communications register followed by the data for the addressed register.

Reading the ID register is the recommended method for verifying correct communication with the device. The ID register is a read only register and contains the value of 0x14. The communication register and ID register details are described in Table 31 and Table 32.

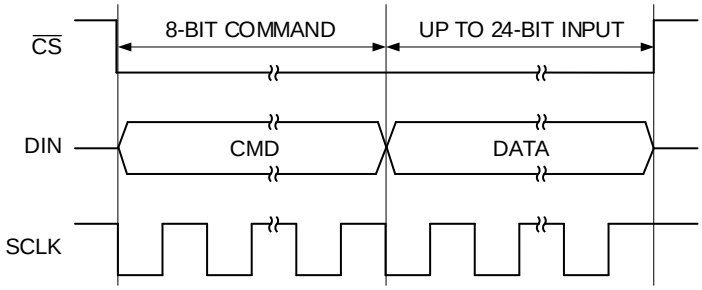


Figure 25: Writing to a Register (8-Bit Command with Register Address Followed by Data of 8 Bits, 16 Bits, or 24 Bits; Data Length Is Dependent on the Register Selected)

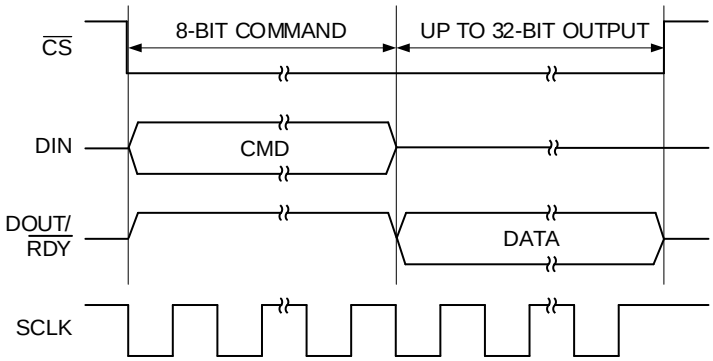


Figure 26: Reading from a Register (8-Bit Command with Register Address Followed by Data of 8 Bits, 16 Bits, 24 Bits, or 32 Bits; Data Length on DOUT Is Dependent on the Register Selected, CRC Enabled)

Table 31: Communications Register

Addr.	Name	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	COMMS	W	0x00	WEN	R/W	RS[5:0]					

Table 32: ID Register

Addr.	Name	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	ID	R	0x14	DEVICE_ID				SILICON_REVISION			

9.4 ADC CIRCUIT INFORMATION

9.4.1 ANALOG INPUT CHANNEL

The AD7124-8 uses flexible multiplexing; thus, any of the analog input pins, AIN0 to AIN15, can be selected as a positive inp ut or a negative input. This feature allows the user to perform diagnostics such as checking that pins are connected. It also simplifies printed circuit board (PCB) design. For example, the same PCB can accommodate 2-wire, 3-wire, and 4-wire resistance temperature detectors (RTDs).

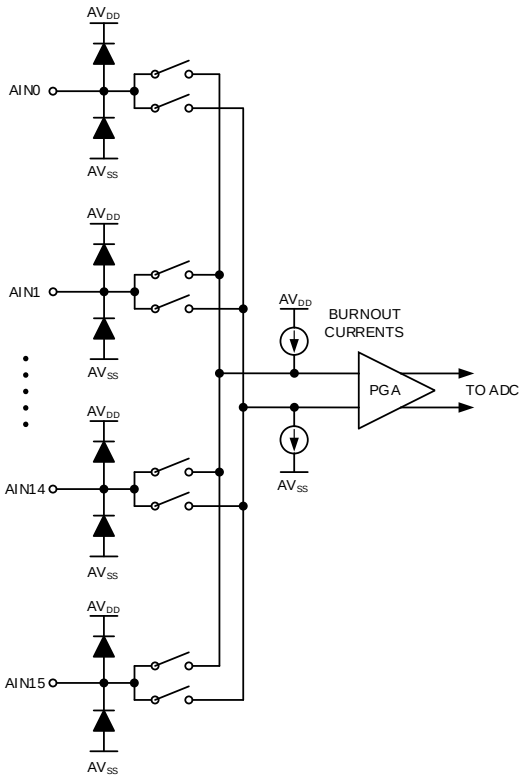


Figure 27: Analog Input Multiplexer Circuit

The channels are configured using the AINP[4:0] bits and the AINM[4:0] bits in the channel registers (see Table 33). The device can be configured to have 8 differential inputs, 15 pseudo differential inputs, or a combination of both. When using differential inputs, use adjacent analog input pins to form the input pair. Using adjacent pins minimizes any mismatch between the channels.

The PGA can be bypassed at a gain of 1 but are automatically enabled when the gain exceeds 1. The PGA is enabled/bypassed using the PGA_CONTROL bits in the configuration register (see Table 34).

In PGA enable mode, the input channel feeds into a high impedance input stage. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive type sensors such as strain gages or RTDs.

When the device is operated in PGA bypass mode, the device has a higher analog input current. Note that this PGA bypassed input path provides a dynamic load to the driving source. Therefore, resistor/capacitor (RC) combinations on the input pins can cause gain errors, depending on the output impedance of the source that is driving the ADC input.

The absolute input voltage in PGA bypass mode (gain = 1) includes the range between AV_{SS} − 100 mV and AV_{DD} + 100 mV. The absolute input voltage range in PGA enable mode at a gain of 1 is restricted to a range between AV_{SS} + 10 mV and AV_{DD} − 600 mV. The common-mode voltage must not exceed these limits; otherwise, linearity and noise performance degrade.

When the gain is greater than 1, the PGA are automatically enabled. Note the common-mode voltage should meet the PGA input requirements.

Table 33: Channel Register

Addr.	Name	R/W	Default	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	CHANNEL0	R	0x8001	[15:8]	Enable	Setup			0		AINP[4:3]	
To 0x18	To CHANNEL15			[7:0]	AINP[2:0]			AINM[4:0]				

Table 34: Configuration Register

Addr.	Name	R/W	Default	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x19 To 0x20	CONFIG0 To CONFIG7	R	0x0860	[15:8]	0				Bipolar	Burnout		REF_BUFP
				[7:0]	REF_BUFM	PGA_CONTROL		REF_SEL		PGA		

9.4.2 PROGRAMMABLE GAIN AMPLIFIER (PGA)

The AD7124-8 features a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64 or 128 by configuration register (see Table 34). Figure 28 shows a simplified diagram of the PGA. The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the gain of the PGA. The PGA input is equipped with an electromagnetic interference (EMI) filter.

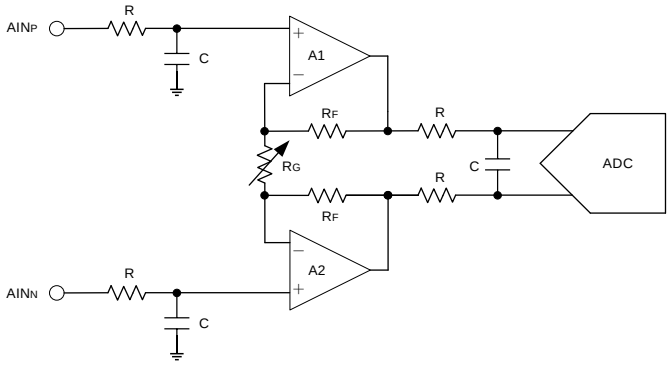


Figure 28: Simplified Diagram of the PGA

Note that as with any PGA, ensure that the input voltage stays within the specified common-mode input range. The common-mode input voltage (V_{CM}) must be within the range shown in Equation 3.

$$\left(\boldsymbol{AVSS} + \boldsymbol{0.1V} + \frac{\boldsymbol{V_{INMAX} \times GAIN}}{\boldsymbol{2}}\right) < \boldsymbol{V_{CM}} < \left(\boldsymbol{AVDD} - \boldsymbol{0.1V} - \frac{\boldsymbol{V_{INMAX} \times GAIN}}{\boldsymbol{2}}\right) \qquad (3)$$

To make sure the PGA is working in the linear range, please also note the Absolute input voltage in Recommended Operating Conditions, which also shown in Equation 4.

$$\boldsymbol{AVSS} + \boldsymbol{0.01V} < \boldsymbol{V_{(AINX)}} < \boldsymbol{AVDD} - \boldsymbol{1.0V} \qquad (4)$$

Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in Equation 5.

$$\boldsymbol{FSR} = \frac{\boldsymbol{\pm V_{REF}}}{\boldsymbol{GAIN}} \qquad (5)$$

Table 35 shows the corresponding full-scale input ranges when using the internal 2.5V reference

Table 35: PGA Full Scale Range

PGA GAIN Setting	FSR
1	±2.5 V
2	±1.25 V
4	±625 mV
8	±312.5 mV
16	±156.25 V
32	±78.125 mV
64	±39.0625 mV
128	±19.53125 mV

9.4.3 SINGLE END APPLICATION

As special common mode voltage compensation function designed in PGA, AD7124-8 can support single-end application even worked in single supply operation, configuring AINP or AINM to AVSS enable the single end application. In single end application PGA can be worked at gain exceeds 1, but please note some special feather of this application:

- Gain exceeds 1 supported in single end application, but higher gain will decrease ENOB of AD7124-8B.
- When AD7124-8B worked in single supply operation with PGA enabled, take care the Absolute input voltage in Recommended Operating Conditions.
- Configuring AINP or AINM to AVSS is the only way for single end application, that means user can not connect AINP or AINM pin to AVSS externally.

9.4.4 REFERENCE

The AD7124-8 has an embedded 2.5 V reference. The embedded reference is a low noise, low drift reference with 15 ppm/°C drift maximum on the AD7124-8. Including the reference on the AD7124-8 reduces the number of external components needed in applications such as thermocouples, leading to a reduced PCB size.

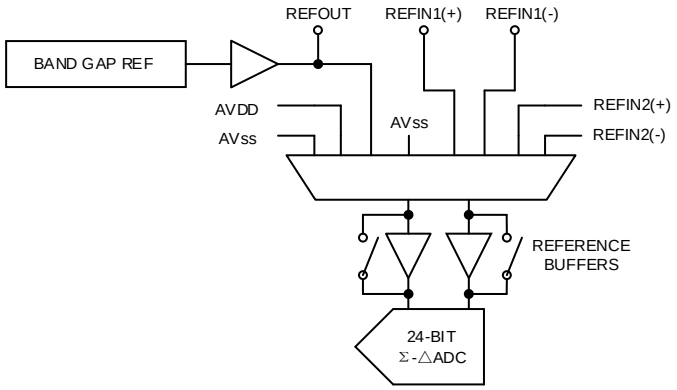


Figure 29: Reference Connections

This reference can be used to supply the ADC (by setting the REF_EN bit in the ADC_CONTROL register to 1) or an external reference can be applied. For external references, the ADC has a fully differential input capability for the channel. In addition, the user can select one of two external reference options (REFIN1 or REFIN2). The reference source for the AD7124-8 is selected using the REF_SEL bits in the configuration register (see Table 34). When the internal reference is selected, it is internally connected to the modulator. It can also be made available on the REFOUT pin. A 0.1 µF decoupling capacitor is required on REFOUT when the internal reference is active.

The common-mode range for the differential reference inputs is from AVSS – 0.1V to AVDD + 0.1V when the reference buffers are disabled. The reference inputs can also be buffered on-chip. The buffers require 100 mV of headroom. The reference voltage of REFIN (REFINx(+) − REFINx(−)) is 2.5 V nominal, but the AD7124 is functional with reference voltages from 0.5 V to AVDD.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the devices, the effect of the low frequency noise in the excitation source is removed, because the application is ratio metric. If the AD7124-8B is used in non-ratio metric applications, use a low noise reference.

Note that the reference input provides a high impedance, dynamic load when unbuffered. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations

unbuffered, depending on the output impedance of the source driving the reference inputs.

Reference voltage sources typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFINx(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. In this situation, using the reference buffers is required.

9.4.5 BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7124-8B can accept either unipolar or bipolar input voltage ranges, which allows the user to tune the ADC input range to the sensor output range. When a split power supply is used, the device accepts truly bipolar inputs. When a single power supply is used, a bipolar input range does not imply that the device can tolerate negative voltages with respect to system AVSS. Unipolar and bipolar signals on the AINP input are referenced to the voltage on the AINM input. For example, if AINM is 1.5 V and the ADC is configured for unipolar mode with a gain of 1, the input voltage range on the AINP input is 1.5 V to 3 V when VREF = AVDD = 3 V. If the ADC is configured for bipolar mode, the analog input range on the AINP input is 0 V to AVDD. The bipolar/unipolar option is chosen by programming the bipolar bit in the configuration register.

9.4.6 DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00 … 00, a midscale voltage resulting in a code of 100 … 000, and a full-scale input voltage resulting in a code of 111 … 111. The output code for any analog input voltage can be represented as:

$$Code = (2^N \times AIN \times Gain)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000 … 000, a zero differential input voltage resulting in a code of 100 … 000, and a positive full-scale input voltage resulting in a code of 111 … 111. The output code for any analog input voltage can be represented as:

$$Code = 2^{N-1} \times [(AIN \times Gain/V_{REF}) + 1]$$

where: N = 24.

AIN is the analog input voltage.

Gain is the gain setting (1 to 128).

9.4.7 EXCITATION CURRENTS

The AD7124 also contains two matched, software configurable, constant current sources that can be programmed to equal 10 µA, 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, or 1 mA. These current sources can be used to excite external resistive bridges

or RTD sensors. Both current sources source currents from AVDD and can be directed to any of the analog input pins (see Figure 30).
The pins on which the currents are made available are programmed using the IOUT1_CH and IOUT0_CH bits in the IO_CONTROL_1 register (see Table 36). The magnitude of each current source is individually programmable using the IOUT1 and IOUT0 bits in the IO_CONTROL_1 register. In addition, both currents can be output to the same analog input pin.
Note that the on-chip reference does not need to be enabled when using the excitation currents.

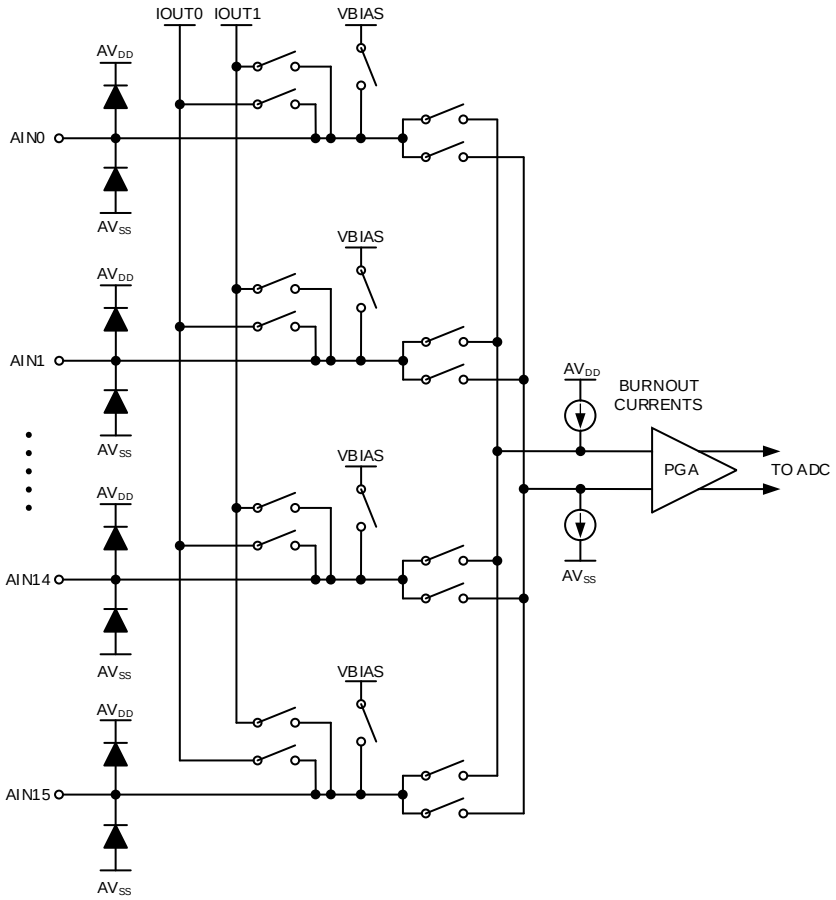


Figure 30: Excitation Current and Bias Voltage Connections

9.4.8 BRIDGE POWER-DOWN SWITCH

In bridge applications such as strain gages and load cells, the bridge itself consumes the majority of the current in the system. For example, a 350 Ω load cell requires 8.6 mA of current when excited with a 3 V supply. To minimize the current consumption of the system, the bridge can be disconnected (when it is not being used) using the bridge power-down switch. The switch can withstand 30 mA of continuous current, and it has an on resistance of 10 Ω maximum. The PDSW bit in the IO_CONTROL_1 register controls the switch.

9.4.9 LOGIC OUTPUTS

The AD7124-8B has four general-purpose digital outputs: P1 to P4. These are enabled using the GPIO_CTRL bits in the IO_CONTROL_1 register (see Table 36). The pins can be pulled high or low using the GPIO_DATx bits in the register; that is, the value at the pin is determined by the setting of the GPIO_DATx bits. The logic levels for these pins are determined by AVDD rather than by IOVDD.

Table 36: Input/Output control 1 Register

Addr.	Name	R/W	Default	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03	IO_CONTROL_1	R/W	0x000000	[23:16]	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1
				[15:8]	PDSW	0	IOUT1			IOUT0		
				[7:0]	IOUT1_CH				IOUT0_CH			

These pins can be used to drive external circuitry, for example, an external multiplexer. If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled via the AD7124-8B general-purpose output pins. The general-purpose output pins can be used to select the active multiplexer pin.
Because the operation of the multiplexer is independent of the AD7124-8, reset the modulator and filter using the SYNC pin or by writing to the mode or configuration register each time that the multiplexer channel is changed.

9.4.10 BIAS VOLTAGE GENERATOR

A bias voltage generator is included on the AD7124-8B (see Figure 30). It biases the selected input pin to (AVDD − AVSS)/2. This function is useful in thermocouple applications, as the voltage generated by the thermocouple must be biased around some dc voltage if the ADC operates from a single power supply. The bias voltage generator is controlled using the VBIASx bits in the IO_CONTROL_2 register (see Table 37).

Table 37: Input/Output Control 2 Register

Addr.	Name	R/W	Default	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	IO_CONTROL_2	R/W	0x0000	[15:8]	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8
				[7:0]	VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0

9.4.11 CLOCK

The AD7124-8 includes an internal 614.4 kHz clock on chip. This internal clock has a tolerance of ± 3%. Use either the internal clock or an external clock as the clock source to the AD7124-8. The clock source is selected using the CLK_SEL bits in the ADC_CONTROL register (see Table 38).
The internal clock can also be made available at the CLK pin. This is useful when several ADCs are used in an application and the devices must be synchronized. The internal clock from one device can be used as the clock source for all ADCs in the system. Using a common clock, the devices can be synchronized by applying a common reset to all devices, or the SYNC pin can be pulsed.

Table 38: ADC Control Register

Addr.	Name	R/W	Default	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	ADC_CONTROL	R/W	0x0000	[15:8]	0			DOUT_$\overline{\text{RDY}}$_DEL	CONT_READ	DATA_STATUS	$\overline{\text{CS}}$_EN	REF_EN
				[7:0]	POWER_MODE		MODE				CLK_SEL	

9.4.12 POWER MODES

The AD7124 has three power modes:

- full power mode
- mid power mode
- low power mode

The mode is selected using the POWER_MODE bits in the ADC_CONTROL register. The power mode affects the power consumption of the device as well as changing the master clock frequency. A 614.4 kHz clock is used by the device. However, this clock is internally divided, the division factor being dependent on the power mode. Thus, the range of output data rates and performance is affected by the power mode.

Table 39: Power Modes

Power Mode	Master Clock(kHz)	Output Data Rate(SPS)[1]	Current
Full Power	614.4	9.37 to 19200	
Mid Power	153.6	2.34 to 4800	
Low Power	76.8	1.17 to 2400	

1. Unsettled, using a $sinc^3$/$sinc^4$ filter.

9.4.13 STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDOs remain active so that registers maintain their contents. If enabled, the reference, internal oscillator, digital outputs P1 to P4, the bias voltage generator and the low-side power switch remain active. The excitation currents, if enabled, also remain active in standby mode. These blocks can be disabled, if required, by setting the corresponding bits appropriately. Other diagnostics remain active if enabled when the ADC is in standby mode. Diagnostics can be enabled or disabled while in standby mode. However, any diagnostics that require the master clock (memory map CRC, and MCLK counter) must be enabled when the ADC is in continuous conversion mode or idle mode; these diagnostics do not function if enabled in standby mode.

The internal oscillator, if disabled in standby mode, requires an additional 40 µs to power up and settle. If an external master clock is being used, ensure that it is active before issuing the command to exit standby mode. Do not write to the ADC_ CONTROL register again until the ADC has powered up and settled.

In power-down mode, all blocks are powered down, including the LDOs. All registers lose their contents, and the digital outputs P1 to P4 are placed in tristate. To prevent accidental entry to power-down mode, the ADC must first be placed into standby mode. If an external master clock is being used, keep it active until the device is placed in power-down mode. Exiting power-down mode requires 64 SCLK cycles with $\overline{CS}$ = 0 and DIN = 1, that is, a serial interface reset. The AD7124-8 requires 2 ms typically to power up and settle. After this time, the user can access the on-chip registers. The power-down current is 0.1 µA typically.

9.4.14 DIGITAL INTERFACE

The programmable functions of the AD7124-8 are controlled using a set of on -chip registers. Data is written to these registers via the serial interface. Read access to the on-chip registers is also provided by this interface. All communications with the device must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the devices begins with a write operation to the communications register, followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register, followed by a read operation from the selected register.

The serial interface of the AD7124-8B consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line transfers data into the on-chip registers, whereas DOUT/$\overline{RDY}$. accesses data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT/$\overline{RDY}$.) occur with respect to the SCLK signal. The DOUT/$\overline{RDY}$.. pin also operates as a data ready signal; the line goes low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high before the data register updates to indicate when not to read from the device, to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can decode the AD7124 in systems where several components are connected to the serial bus.

Figure 2 and Figure 3 show timing diagrams for interfacing to the AD7124-B with $\overline{CS}$ decoding the devices. Figure 2 shows the timing for a read operation from the output shift register of the AD7124-8. Figure 3 shows the timing for a write operation to the input shift register. A delay is required between consecutive SPI communications. Figure 4 shows the delay required between SPI read/write operations. It is possible to read the same word from the data register several times, even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations are complete before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines communicate with the AD7124-8. The end of the conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idle high between data transfers.

The AD7124-8 can be operated with $\overline{CS}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$, because $\overline{CS}$ normally occurs after the falling edge of SCLK in DSPs. SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

$\overline{CS}$ must be used to frame read and write operations and the $\overline{CS}$_EN bit in the ADC_CONTROL register must be set when the diagnostics SPI_READ_ERR, SPI_WRITE_ERR, or SPI_SCLK_CNT_ERR are enabled.

The serial interface can be reset by writing a series of 1s on the DIN input. See the Reset section for more details. Reset returns the interface to the state in which it is expecting a write to the communications register.

The AD7124-8B can be configured to continuously convert or perform a single conversion (see Figure 31 through Figure 33).

9.4.15 Single Conversion Mode

In single conversion mode, the AD7124 performs a single conversion and is placed in standby mode after the conversion is complete. If a master clock is present (external master clock or the internal oscillator is enabled), DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word is read from the data register, DOUT/$\overline{RDY}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ is high. Do not read the ADC_CONTROL register close to the completion of a conversion because the mode bits are being updated by the ADC to indicate that the ADC is in standby mode.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{RDY}$ goes high and remains high until a valid conversion is available and $\overline{CS}$ is low.

As soon as the conversion is available, DOUT/$\overline{RDY}$ goes low. The ADC then selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is being performed. As soon as the next conversion is complete, the data register is updated; therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to standby mode.
If the DATA_STATUS bit in the ADC_CONTROL register is set to 1, the contents of the status register are output along with the conversion each time that the data read is performed. The four LSBs of the status register indicate the channel to which the conversion corresponds.

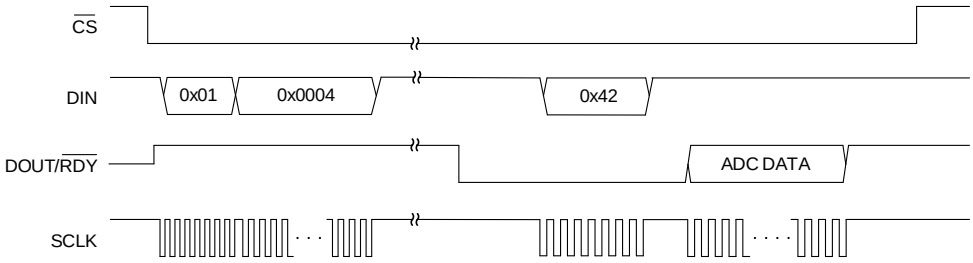


Figure 31: Single Conversion Configuration

9.4.16 Continuous Conversion Mode

Continuous conversion is the default power-up mode. The AD7124-8B converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, write to the communications register, indicating that the next operation is a read of the data register. When the data-word is read from the data register, DOUT/$\overline{RDY}$ goes high. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion; otherwise, the new conversion word is lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all channels are converted, the sequence starts again with the first channel. The channels are converted in order from lowest enabled channel to highest enabled channel. The data register is updated as soon as each conversion is available. The DOUT/$\overline{RDY}$ pin pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel.

If the DATA_STATUS bit in the ADC_CONTROL register is set to 1, the contents of the status register, along with the conversion data, are output each time the data register is read. The status register indicates the channel to which the conversion corresponds.

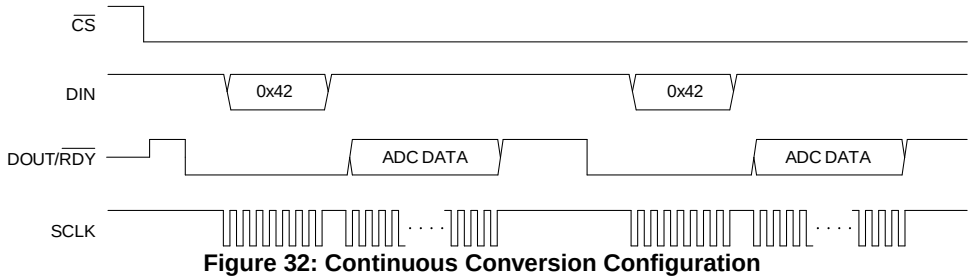


Figure 32: Continuous Conversion Configuration

9.4.17 Continuous Read Mode

In continuous read mode, it is not required to write to the communications register before reading ADC data; apply the required number of SCLKs after DOUT/$\overline{RDY}$ goes low to indicate the end of a conversion. When the conversion is read, DOUT/$\overline{RDY}$ returns high until the next conversion is available. In this mode, the data can be read only once. Ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7124-8B to read the word, the serial output register is reset when the next conversion is complete, and the new conversion is placed in the output serial register. The ADC must be configured for continuous conversion mode to use continuous read mode.

To enable continuous read mode, set the CONT_READ bit in the ADC_CONTROL register. When this bit is set, the only serial inter- face operations possible are reads from the data register. To exit continuous read mode, write a read data command (0x42) while the DOUT/$\overline{RDY}$ pin is low. Alternatively, apply a software reset, that is, 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1. This resets the ADC and all register contents. These are the only commands that the interface recognizes after it is placed in continuous read mode. DIN must be held low in continuous read mode until an instruction is to be written to the device. If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if DATA_ STATUS is set in the ADC_CONTROL register. The status register indicates the channel to which the conversion corresponds.

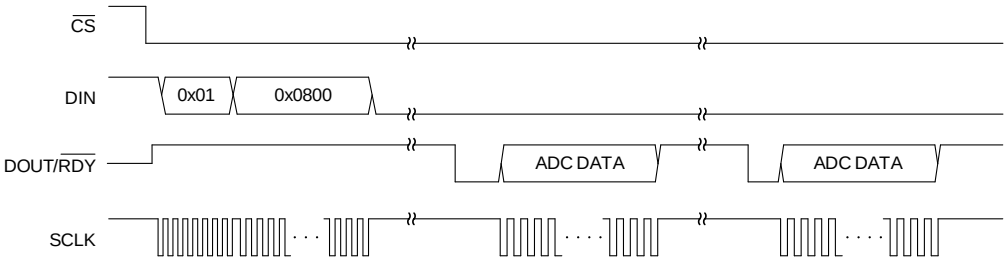


Figure 33: Continuous Read Configuration

9.4.18 DATA_STATUS

The contents of the status register can be appended to each conversion on the AD7124-8. This is a useful function if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The four LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are being flagged via the ERROR_FLAG bit. To append the status register contents to every conversion, the DATA_STATUS bit in the ADC_CONTROL register is set to 1.

9.4.19 SERIAL INTERFACE RESET (DOUT_$\overline{RDY}$_DEL and $\overline{CS}$_EN BITS)

The instant at which the DOUT/$\overline{RDY}$ pin changes from being a DOUT pin to a $\overline{RDY}$ pin is programmable on the A7124-8. By default, the DOUT/$\overline{RDY}$ pin changes functionality after a period following the last SCLK rising edge, the SCLK edge on which the LSB is read by the processor. This time is 10 ns minimum by default, and by setting the DOUT/$\overline{RDY}$_DEL bit in the ADC_ CONTROL register to 1, can be extended to 110 ns minimum.

By setting the $\overline{CS}$_EN bit in the ADC_CONTROL register to 1, the DOUT/$\overline{RDY}$ pin continues to output the LSB of the register being read until $\overline{CS}$ is taken high. This configuration is useful if the $\overline{CS}$ signal is used to frame all read operations. If $\overline{CS}$ is not used to frame all read operations, set $\overline{CS}$_EN to 0 so that DOUT/$\overline{RDY}$ changes functionality following the last SCLK edge in the read operation.

$\overline{CS}$_EN must be set to 1 and the $\overline{CS}$ signal must be used to frame all read and write operations when the SPI_READ_ERR, SPI_WRITE_ERR, and SPI_SCLK_CNT_ERR diagnostic functions are enabled.

The serial interface is always reset on the $\overline{CS}$ rising edge, that is, the interface is reset to a known state whereby it awaits a write to the communications register. Therefore, if a read or write operation is performed by performing multiple 8-bit data transfers, $\overline{CS}$ must be held low until all the bits are transferred.

9.4.20 RESET

The circuitry and serial interface of the AD7124-8B can be reset by writing 64 consecutive 1s to the device. This resets the logic, the digital filter, and the analog modulator, and all on-chip registers are reset to their default values. A reset is automatically performed on power-up. A reset requires a time of 90 MCLK cycles. A reset is useful if the serial interface becomes asynchronous due to noise on the SCLK line.

9.4.21 CALIBRATION

The AD7124-8 provides three calibration modes that can be used to eliminate the offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x800000, and the nominal value of the gain register is 0x500000. The calibration range of the ADC gain is from 0.35 × VREF/gain to 1.06 × VREF/gain.

The following equations show the calculations that are used in each calibration mode. In unipolar mode, the ideal relationship—that is, not considering the ADC gain error and offset error—is as follows:

$$Data = \left(\frac{0.8 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000)\right) \times \frac{Gain}{0x400000} \times 2 \quad (1)$$

In bipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left(\frac{0.8 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000)\right) \times \frac{Gain}{0x400000} + 0x800000 \quad (2)$$

To start a calibration, write the relevant value to the mode bits in the ADC_CONTROL register. The DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register are updated, the $\overline{RDY}$ bit in the status register is reset, the DOUT/$\overline{RDY}$ pin returns low (if $\overline{CS}$ is low), and the AD7124 reverts to idle mode.

During an internal offset calibration, the selected positive analog input pin is disconnected, and it is connected internally to the selected negative analog input pin. For this reason, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference.

Note that AD7124-8B do not have internal full-scale calibration, as it's factory calibrated for all gains, the factory gain calibrated coefficients are not open to user.

System calibrations expect the system zero-scale (offset) and system full-scale (gain) voltages to be applied to the ADC pins before initiating the calibration modes. As a result, errors external to the ADC are removed. The system zero-scale calibration must be performed before the system full-scale calibration.

From an operational point of view, treat a calibration like another ADC conversion. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of a calibration via a polling sequence or an interrupt-driven routine.

An internal/system offset calibration and system full-scale calibration requires a time equal to the settling time of the selected filter to be completed.

A calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. A new calibration is required for a given channel if the reference source or the gain for that channel is changed. Offset and system full-scale calibrations can be performed in any power mode.

The offset error is typically ±50μV/Gain. An internal or system offset calibration reduces the offset error to the order of the noise. The gain error is factory calibrated at ambient temperature for all gains. Following these calibrations, the gain error is ±0.01% typically. Therefore, there is no internal full-scale calibrations function for AD7124-8. A system full -scale calibration reduces the gain error to the order of the noise.

The AD7124-8B provides the user with access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device and to write its own calibration coefficients from prestored values in the EEPROM. A read or write of the offset and gain registers can be performed at any time except during an internal or self-calibration. The values in the calibration registers are 24 bits wide. The span and offset of the device can also be manipulated using the registers.

9.4.22 SPAN AND OFFSET LIMITS

Whenever a system calibration mode is used, the amount of offset and span that can be accommodated is limited. The overriding requirement in determining the amount of offset and gain that can be accommodated by the device is the requirement that the positive full-scale calibration limit is ⩽1.05 × VREF/gain. This allows the input range to go 5% above the nominal range. The built-in headroom in the AD7124-8B analog modulator ensures that the device still operates correctly with a positive full-scale voltage, which is 5% beyond the nominal.

The range of input span in both the unipolar and bipolar modes have a minimum value of 0.8 × VREF/gain and a maximum value of 2.1 × VREF/gain. However, the span, which is the difference between the bottom of the AD7124-8 input range and the top of its input range, must account for the limitation on the positive full-scale voltage. The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. The offset must account for the limitation on the positive full-scale voltage. In unipolar mode, there is considerable flexibility in handling negative (with respect to AINM) offsets. In both unipolar and bipolar modes, the range of positive offsets that can be handled by the device depends on the selected span. Therefore, in determining the limits for system zero-scale and full-scale calibrations, the user must ensure that the offset range plus the span range does exceed 1.05 × VREF/gain. This is best illustrated by looking at a few examples. If the device is used in unipolar mode with a required span of 0.8 × VREF/gain, the offset range that the system calibration can handle is from −1.05 × VREF/gain to +0.25 × VREF/gain. If the device is used in unipolar mode with a required span of VREF/gain, the offset range that the system calibration can handle is from −1.05 × VREF/gain to +0.05 × VREF/gain. Similarly, if the device is

used in unipolar mode and required to remove an offset of 0.2 × VREF/gain, the span range that the system calibration can handle is 0.85 × VREF/gain.
If the device is used in bipolar mode with a required span of ±0.4 × VREF/gain, then the offset range that the system calibration can handle is from −0.65 × VREF/gain to +0.65 × VREF/gain. If the device is used in bipolar mode with a required span of ±VREF/gain, the offset range the system calibration can handle is from −0.05 × VREF/gain to +0.05 × VREF/gain. Similarly, if the device is used in bipolar mode and required to remove an offset of ±0.2 × VREF/gain, the span range that the system calibration can handle is ±0.85 × VREF/gain.

9.4.23 SYSTEM SYNCHRONIZATION

The SYNC input allows the user to reset the modulator and the digital filter without affecting any of the setup conditions on the device. This allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of SYNC. Take SYNC low for at least four master clock cycles to implement the synchronization function.

If multiple AD7124-8 devices are operated from a common master clock, they can be synchronized so that their data registers are updated simultaneously. A falling edge on the SYNC pin resets the digital filter and the analog modulator and places the AD7124-8B into a consistent, known state. While the SYNC pin is low, the AD7124-8 is maintained in this state. On the SYNC rising edge, the modulator and filter exit this reset state, and, on the next clock edge, the device starts to gather input samples again. In a system using multiple AD7124-8 devices, a common signal to their SYNC pins synchronizes their operation. This is normally performed after each AD7124-8 has performed its own calibration or has calibration coefficients loaded into its calibration registers. The conversions from the AD7124-8 devices are then synchronized.

The device exits reset on the master clock falling edge following the SYNC low to high transition. Therefore, when multiple devices are being synchronized, pull the SYNC pin high on the master clock rising edge to ensure that all devices begin sampling on the master clock falling edge. If the SYNC pin is not taken high in sufficient time, it is possible to have a difference of one master clock cycle between the devices; that is, the instant at which conversions are available differs from device to device by a maximum of one master clock cycle.

The SYNC pin can also be used as a start conversion command. In this mode, the rising edge of SYNC starts conversion and the falling edge of $\overline{RDY}$ indicates when the conversion is complete. The settling time of the filter must be allowed for each data register update. For example, if the ADC is configured to use the sinc4 filter and zero latency is disabled, the settling time equals $4/f_{ADC}$ where f_{ADC} is the output data rate when continuously converting on a single channel.

9.5 DIGITAL FILTER

The AD7124-8 offers a great deal of flexibility in the digital filter. The device has several filter options. The option sele cted affects the output data rate, settling time, and 50 Hz and 60 Hz rejection. The following sections describe each filter type, indicating the available output data rates for each filter option. The filter response along with the settling time and 50 Hz and 60 Hz rejection is also discussed.
The filter bits in the filter register select between the sinc type filter.

Table 40: Filter Registers

Addr.	Name	R/W	Default	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x21 To 0x28	FILTER_0 To FILTER_7	R/W	0x060180	[23:16]	FILTER			REJ60	POST_FILTER			SINGLE_ CYCLE
				[15:8]	0					FS[10:8]		
				[7:0]	FS[7:0]							

9.5.1 SINC^4 FILTER

When the AD7124-8B is powered up, the sinc^4 filter is selected by default. This filter gives excellent noise performance over the complete range of output data rates. It also gives the best 50 Hz/ 60 Hz rejection, but it has a long settling time. In Figure 34 the blocks shown in gray are unused.

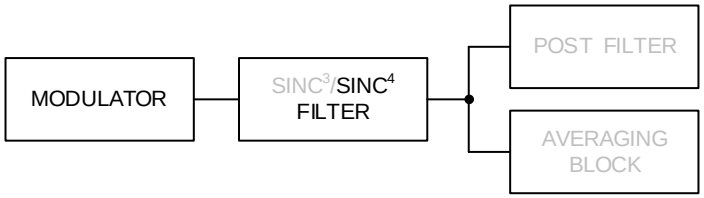


Figure 34: Sinc^4 Filter

9.5.1.1 Sinc^4 Output Data Rate/Settling Time

The output data rate (the rate at which conversions are available on a single channel when the ADC is continuously converting) is equal to:

$$f_{ADC} = f_{CLK}/(32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency (614.4 kHz in full power mode, 153.6 kHz in mid power mode, and 76.8 kHz in low power mode).
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.
The output data rate can be programmed from:

- 9.38 SPS to 19,200 SPS for full power mode
- 2.35 SPS to 4800 SPS for mid power mode
- 1.17 SPS to 2400 SPS for low power mode

The settling time for the sinc^4 filter is equal to

$$t_{SETTLE} = (4 \times 32 \times FS[10:0] + Dead\ Time + C)/f_{CLK}$$

Where: C = 0 when FS[10:0] $\leqslant$ 2, and C = 16 when FS[10:0] > 2. For Dead Time, which is related to Power Mode:
In Full Power Mode, Dead Time = 77 when FS[10:0] $\leqslant$ 12, and Dead Time = 90 when FS[10:0] > 12. In Mid Power Mode, Dead Time = 54 when FS[10:0] $\leqslant$ 6, and Dead Time = 43 when FS[10:0] > 6. In Low Power Mode, Dead Time = 67 when FS[10:0] $\geqslant$ 2 and FS[10:0] $\leqslant$ 8, Dead Time = 29 when FS[10:0] = 1 or FS[10:0] $>$8.

When a channel change occurs, the modulator and filter are reset. The settling time is allowed to generate the first conversion after the channel change. Subsequent conversions on this channel occur at $1/f_{ADC}$.

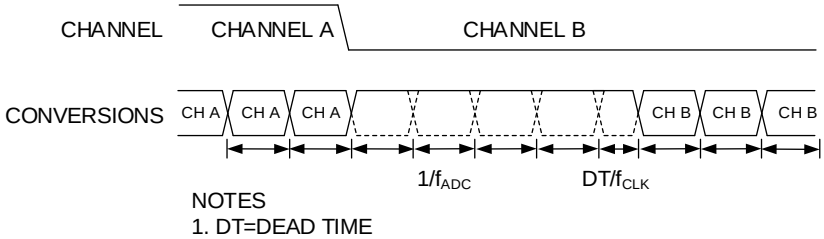


Figure 35: Sinc^4 Channel Change

When conversions are performed on a single channel and a step change occurs, the ADC does not detect the change in the analog input. Therefore, it continues to output conversions at the programmed output data rate. However, it is at least four conversions later before the output data accurately reflects the analog input. If the step change occurs while the ADC is processing a conversion, then the ADC takes five conversions after the step change to generate a fully settled result.

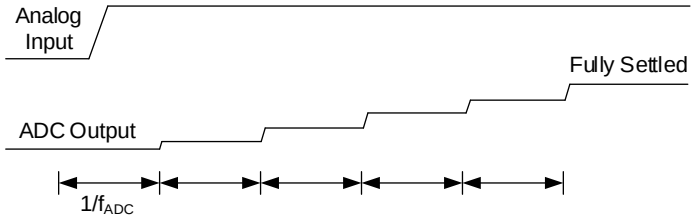


Figure 36: Asynchronous Step Change in the Analog Input

Table 41 gives some examples of the relationship between the values in the FS[10:0] bits and the corresponding output data rate and settling time.

Table 41: Examples of Output Data Rates and the Corresponding Settling Times for the Sinc^4 Filter

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (fCLK = 614.4 kHz)	1920	10	400.13
	384	50	80.15
	320	60	66.81
Mid Power (fCLK = 153.6 kHz)	480	10	400.25
	96	50	80.25
	80	60	66.92
Low Power (fCLK = 76.8 kHz)	240	10	400.33
	48	50	80.33
	40	60	66.99

9.5.1.2 Sinc^4 Zero Latency

Zero latency is enabled by setting the SINGLE_CYCLE bit in the filter register to 1. With zero latency, the conversion time when continuously converting on a single channel approximately equals the settling time. The benefit of this mode is that a similar period of time elapses between all conversions irrespective of whether the conversions occur on one channel or whether several channels are used. When the analog input is continuously sampled on a single channel, the output data rate equals

$$f_{ADC} = f_{CLK}/(4 \times 32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency.
FS[10:0] is the decimal equivalent of the FS[10:0] bits in the setup filter register.

When the user selects another channel, there is an extra delay in the first conversion of Dead Time/f_{CLK} where Dead Time is related to Power Mode:
In Full Power Mode, Dead Time = 85 when FS[10:0] $\leqslant$ 12, and Dead Time = 98 when FS[10:0] > 12. In Mid Power Mode, Dead Time = 61 when FS[10:0] $\leqslant$ 6, and Dead Time = 50 when FS[10:0] > 6. In Low Power Mode, Dead Time = 74 when FS[10:0] $\geqslant$ 2 and FS[10:0] $\leqslant$ 8, Dead Time = 36 when FS[10:0]=1 or FS[10:0] > 8.

At low output data rates, this extra delay has little impact on the value of the settling time. However, at high output data rates, the delay must be considered. Table 42 summarizes the output data rate when continuously converting on a single channel and the settling time when switching between channels for a sample of FS[10:0] values.

When switching between channels, the AD7124-8 allows the complete settling time to generate the first conversion after the channel change. Therefore, the ADC automatically operates in zero latency mode when several channels are enabled—setting the SINGLE_CYCLE bit has no benefits.

Table 42: Examples of Output Data Rates and the Corresponding Settling Times for the Sinc^4 Filter(Zero Latency)

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (fCLK = 614.4 kHz)	1920	2.5	400.13
	384	12.5	80.15
	320	15	66.81
Mid Power (fCLK = 153.6 kHz)	480	2.5	400.25
	96	12.5	80.25

	80	15	66.92
Low Power (fCLK = 76.8 kHz)	240	2.5	400.33
	48	12.5	80.33
	40	15	66.99

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate.

When conversions are being performed on a single channel and a step change occurs on the analog input, the ADC continues to output fully settled conversions if the step change is synchronized with the conversion process. If the step change is asynchronous, one conversion is output from the ADC, which is not completely settled (see Figure 37).

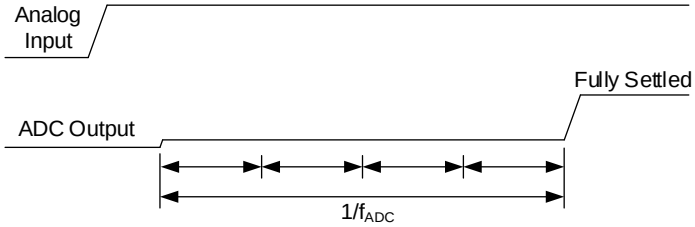


Figure 37: Sinc^4 Zero Latency Operation

9.5.1.3 Sequencer

The description in the Sinc^4 Filter section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 41. For all subsequent conversions, the time needed for each conversion is the settling time also, but the dead time is reduced to

- In Full Power Mode, Dead Time = 73 when FS[10:0] $\leqslant$ 12, and Dead Time = 86 when FS[10:0] > 12;
- In Mid Power Mode, Dead Time = 30 when FS[10:0] $\leqslant$ 6, and Dead Time = 39 when FS[10:0] > 6;
- In Low Power Mode, Dead Time = 25.

9.5.2 SINC^3 FILTER

A sinc^3 filter can be used instead of the sinc^4 filter. The filter is selected using the filter bits in the filter register. This filter has good noise performance, moderate settling time, and moderate 50 Hz and 60 Hz (±1 Hz) rejection. In Figure 38, the blocks shown in gray are unused.

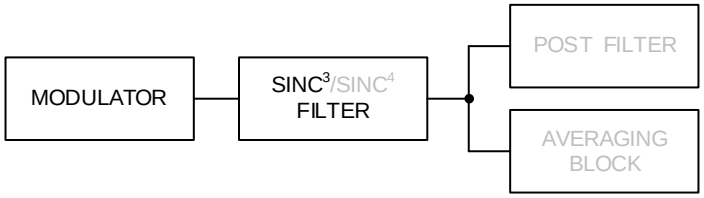


Figure 38: Sinc^3 Filter

9.5.2.1 Sinc^3 Output Data Rate and Settling Time

The output data rate (the rate at which conversions are available on a single channel when the ADC is continuously converting) equals:

$$f_{ADC} = f_{CLK}/(32 \times FS[10:0])$$

where:

f_{ADC} is the output data rate.

f_{CLK} is the master clock frequency (614.4 kHz in full power mode,153.6 kHz in mid power mode and 76.8 kHz in low power mode).

FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

The output data rate can be programmed from:

- 9.38 SPS to 19,200 SPS for full power mode
- 2.35 SPS to 4800 SPS for mid power mode
- 1.17 SPS to 2400 SPS for low power mode

The settling time for the sinc^3 filter is equal to

$$t_{SETTLE} = (3 \times 32 \times FS[10:0] + Dead\ Time + C)/f_{CLK}$$

Where: C = 0 when FS[10:0] $\leqslant$ 2, and C = 16 when FS[10:0] > 2. For Dead Time, which is relate to Power Mode:

In Full Power Mode, Dead Time = 90. In Mid Power Mode, Dead Time = 62 when FS[10:0] ⩽ 8 and FS[10:0] ⩾ 2, and Dead Time = 43 when FS[10:0] = 1 or FS[10:0] > 8. In Low Power Mode, Dead Time = 71 when FS[10:0] ⩽ 10 and FS[10:0] ⩾ 2, and Dead Time = 29 when FS[10:0] = 1 or FS[10:0] > 10.

Table 43 gives some examples of FS[10:0] settings and the corresponding output data rates and settling times.

Table 43: Examples of Output Data Rates and the Corresponding Settling Times for the Sinc³ Filter

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (fCLK = 614.4 kHz)	1920 384 320	10 50 60	300.15 60.15 50.15
Mid Power (fCLK = 153.6 kHz)	480 96 80	10 50 60	300.28 60.28 50.28
Low Power (fCLK = 76.8 kHz)	240 48 40	10 50 60	300.38 60.38 50.38

When a channel change occurs, the modulator and filter are reset. The complete settling time is allowed to generate the first conversion after the channel change (see Figure 39). Subsequent conversions on this channel are available at $1/f_{ADC}$.

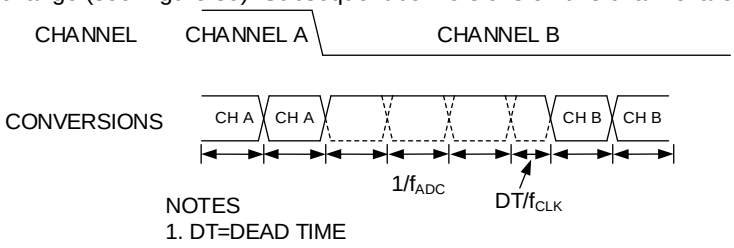


Figure 39: Sinc³ Channel Change

When conversions are performed on a single channel and a step change occurs, the ADC does not detect the change in the analog input. Therefore, it continues to output conversions at the program- med output data rate. However, it is at least three conversions later before the output data accurately reflects the analog input. If the step change occurs while the ADC is processing a conversion, the ADC takes four conversions after the step change to generate a fully settled result.

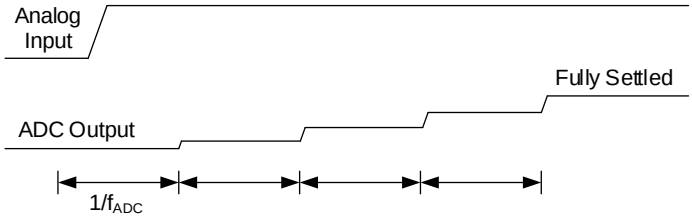


Figure 40: Asynchronous Step Change in the Analog Input

9.5.2.2 Sinc³ Zero Latency

Zero latency is enabled by setting the SINGLE_CYCLE bit in the filter register to 1. With zero latency, the conversion time when continuously converting on a single channel approximately equals the settling time. The benefit of this mode is that a similar period elapses between all conversions irrespective of whether the conversions occur on one channel or whether several channels are used.

When the analog input is continuously sampled on a single channel, the output data rate equals:

$$f_{ADC} = f_{CLK}/(3 \times 32 \times FS[10:0])$$

where:

f_{ADC} is the output data rate.

f_{CLK} is the master clock frequency.

FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register.

When switching channels, there is an extra delay in the first conversion of Dead Time/f_{CLK}

where Dead Time is related to Power Mode:

In Full Power Mode, Dead Time = 98. In Mid Power Mode, Dead Time = 69 when FS[10:0] ⩽ 8 and FS[10:0] > 1, and Dead Time = 50 when FS[10:0] = 1 or FS[10:0] > 8. In Low Power Mode, Dead Time = 78 when FS[10:0] ⩾ 2 and FS[10:0] ⩽ 8, Dead Time = 36 when FS[10:0]=1 or FS[10:0] > 8.

At low output data rates, this extra delay has little impact on the value of the settling time. However, at high output data rates, the delay must be considered. Table 44 summarizes the output data rate when continuously converting on a single channel and the settling time when switching between channels for a sample of FS[10:0].

When the user selects another channel, the AD7124-8 allows the complete settling time to generate the first conversion after the channel change. Therefore, the ADC automatically operates in zero latency mode when several channels are enabled—setting the SINGLE_CYCLE bit has no benefits.

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate. When conversions are being performed on a single channel and a step change occurs on the analog input, the ADC continues to output fully settled conversions if the step change is synchronized with the conversion process. If the step change is asynchronous, one conversion is output from the ADC that is not completely settled (see Figure 41).

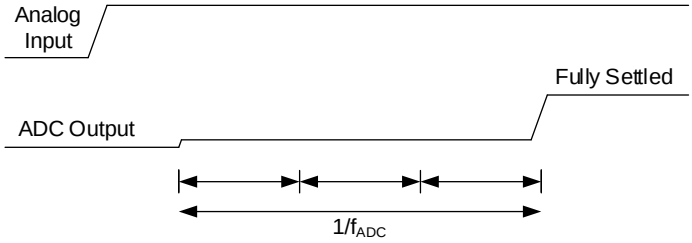


Figure 41: Sinc^3 Zero Latency Operation

Table 44: Examples of Output Data Rates and the Corresponding Settling Times for the Sinc3 Filter (Zero Latency)

Power Mode	FS[10:0]	Output Data Rate (SPS)	Settling Time (ms)
Full Power (fCLK = 614.4 kHz)	1920 384 320	3.33 16.67 20	300.15 60.15 50.15
Mid Power (fCLK = 153.6 kHz)	480 96 80	3.33 16.67 20	300.28 60.28 50.28
Low Power (fCLK = 76.8 kHz)	240 48 40	3.33 16.67 20	300.38 60.38 50.38

9.5.2.3 Sequencer

The description in the Sinc^3 Filter section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 58. For all subsequent conversions, the time needed for each conversion is also the settling time, but the dead time is reduced to:

- In Full Power Mode, Dead Time = 86;
- In Mid Power Mode, Dead Time = 30 when FS[10:0] ⩽ 6, and Dead Time = 39 when FS[10:0] > 6;
- In Low Power Mode, Dead Time = 25.

9.5.3 FAST SETTLING MODE (SINC^4 + SINC^1 FILTER)

In fast settling mode, the settling time is close to the inverse of the first filter notch; therefore, the user can achieve 50 Hz and/or 60 Hz rejection at an output data rate close to 1/50 Hz or 1/60 Hz. The settling time is approximately equal to 1/output data rate. Therefore, the conversion time is near constant when converting on a single channel or when converting on several channels. Enable the fast settling mode using the filter bits in the filter register. In fast settling mode, a sinc1 filter is included after the sinc^4 filter.

The sinc^1 filter averages by 16 in the full power and mid power modes and averages by 8 in the low power mode. In Figure 42, the blocks shown in gray are unused.

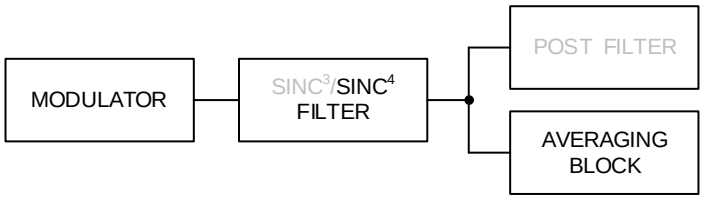


Figure 42: Fast Settling Mode, Sinc⁴ + Sinc¹ Filter

9.5.3.1 Output Data Rate and Settling Time, Sinc⁴ + Sinc¹ Filter

When continuously converting on a single channel, the output data rate is:

$$f_{ADC} = f_{CLK}/(Avg \times 32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency (614.4 kHz in full power mode,153.6 kHz in mid power mode, and 76.8 kHz in low power mode). Avg is 16 for the full or mid power mode and 8 for low power mode. FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

When another channel is selected by the user, there is an extra delay in the first conversion. The settling time is equal to:

$$t_{SETTLE} = \big((4 + Avg - 1) \times 32 \times FS[10:0] + Dead\ Time + 2 + C\big)/f_{CLK}$$

Where: C = 0 when FS[10:0] ⩽ 2, and C = 16 when FS[10:0] > 2. For Dead Time and Avg, which is relate to Power Mode: In Full Power Mode, Avg = 16, Dead Time = 90. In Mid Power Mode, Avg = 16, Dead Time = 55 when FS[10:0] = 1, and Dead Time = 43 when FS[10:0] > 1. In Low Power Mode, Avg = 8, Dead Time = 68 when FS[10:0] ⩽ 2, and Dead Time = 29 when FS[10:0] > 2.

Table 45 lists sample FS[10:0] settings and the corresponding output data rates and settling times.

Table 45: Examples of Output Data Rates and the Corresponding Settling Times (Fast Settling Mode, Sinc⁴ + Sinc¹)

Power Mode	FS[10:0]	First Notch (Hz)	Output Data Rate (SPS)	Settling Time (ms)
Full Power (fCLK = 614.4 kHz, Average by 16)	120	10	10	118.9
	24	50	50	23.9
	20	60	60	19.94
Mid Power (fCLK = 153.6 kHz, Average by 16)	30	10	10	119.04
	6	50	50	24.04
	5	60	60	20.8
Low Power (fCLK = 76.8 kHz, Average by 8)	30	10	10	137.9
	6	50	50	27.9
	5	60	60	23.32

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate.

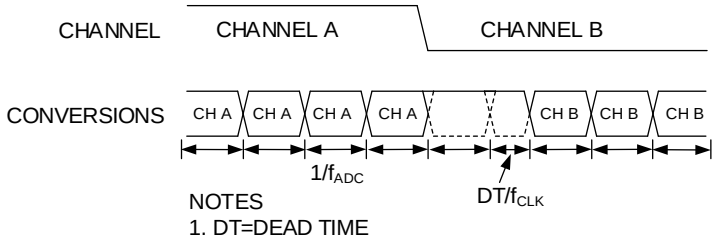


Figure 43: Fast Setting, Sinc⁴ + Sinc¹ Filter

When the device is converting on a single channel and a step change occurs on the analog input, the ADC does not detect the change and continues to output conversions. If the step change is synchronized with the conversion, there is one intermediate result, which is not completely settled (see Figure 44). If the step change is asynchronous to the conversion process, there is one or two intermediate results which are not completely settled.

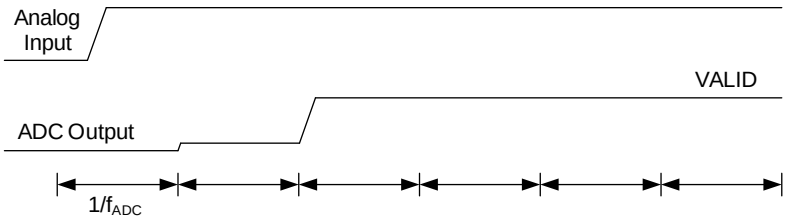


Figure 44: Step Change on the Analog Input, Sinc^4 + Sinc^1 Filter

9.5.3.2 Sequencer

The description in the Fast-Settling Mode (Sinc^4 + Sinc^1 Filter) section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 45. For all subsequent conversions, the time needed for each conversion is also the settling time, but the dead time is reduced to:

- In Full Power Mode, Dead Time = 86;
- In Mid Power Mode, Dead Time = 51 when FS[10:0] = 1, and Dead Time = 39 when FS[10:0] > 1;
- In Low Power Mode, Dead Time = 25.

9.5.4 FAST SETTLING MODE (SINC^3 + SINC^1 FILTER)

In fast settling mode, the settling time is close to the inverse of the first filter notch; therefore, the user can achieve 50 Hz and/or 60 Hz rejection at an output data rate close to 1/50 Hz or 1/60 Hz. The settling time is approximately equal to 1/output data rate. Therefore, the conversion time is near constant when converting on a single channel or when converting on several channels. Enable the fast-settling mode using the filter bits in the filter register. In fast settling mode, a sinc1 filter is included after the sinc^3 filter.
The sinc^1 filter averages by 16 in the full power and mid power modes and averages by 8 in low power mode. In Figure 45, the blocks shown in gray are unused.

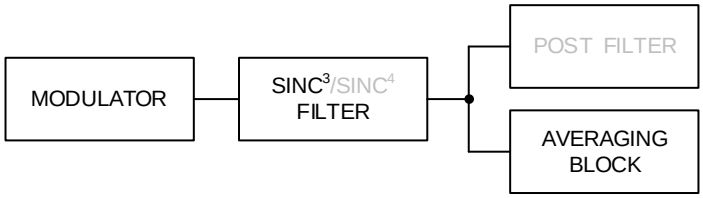


Figure 45: Fast Settling Mode, Sinc^3 + Sinc^1 Filter

9.5.4.1 Output Data Rate and Settling Time, Sinc^3 + Sinc^1 Filter

When continuously converting on a single channel, the output data rate is:

$$f_{ADC} = f_{CLK}/(Avg \times 32 \times FS[10:0])$$

where:
f_{ADC} is the output data rate.
f_{CLK} is the master clock frequency (614.4 kHz in full power mode, 153.6 kHz in mid power mode, and 76.8 kHz in low power mode).

Avg is 16 in full or mid power mode and 8 in low power mode.

FS[10:0] is the decimal equivalent of the FS[10:0] bits in the filter register. FS[10:0] can have a value from 1 to 2047.

When another channel is selected by the user, there is an extra delay in the first conversion. The settling time is equal to:

$$t_{SETTLE} = \left((3 + Avg - 1) \times 32 \times FS[10:0] + Dead\ Time + 2 + C\right)/f_{CLK}$$

Where: C = 0 when FS[10:0] $\leqslant$ 2, and C = 16 when FS[10:0] > 2. For Dead Time and Avg, which is relate to Power Mode:
In Full Power Mode, Avg = 16, Dead Time = 90. In Mid Power Mode, Avg = 16, Dead Time = 55 when FS[10:0] = 1, and Dead Time = 43 when FS[10:0] > 1. In Low Power Mode, Avg = 8, Dead Time = 68 when FS[10:0] $\leqslant$ 2, and Dead Time = 29 when FS[10:0] > 2.

Table 46 lists some sample FS[10:0] settings and the corresponding output data rates and settling times.

Table 46: Examples of Output Data Rates and the Corresponding Settling Times (Fast Settling Mode, Sinc^3 + Sinc^1)

Power Mode	FS[10:0]	First Notch (Hz)	Output Data Rate (SPS)	Settling Time (ms)

Full Power (fCLK = 614.4 kHz, Average by 16)	120 24 20	10 50 60	10 50 60	112.65 22.65 18.9
Mid Power (fCLK = 153.6 kHz, Average by 16)	30 6 5	10 50 60	10 50 60	113.1 23.1 19.35
Low Power (fCLK = 76.8 kHz, Average by 8)	30 6 5	10 50 60	10 50 60	126.2 26.2 22.03

When the analog input is constant or a channel change occurs, valid conversions are available at a near constant output data rate.

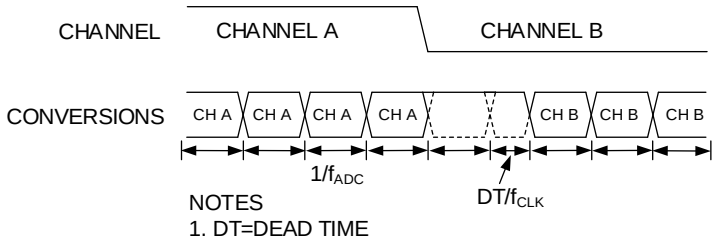


Figure 46: Fast Setting, Sinc^3 + Sinc^1 Filter

When the device is converting on a single channel and a step change occurs on the analog input, the ADC does not detect the change and continues to output conversions. When the step change is synchronized with the conversion, one intermediate result is not completely settled (see Figure 47). If the step change is asynchronous to the conversion process, one or two intermediate results are not completely settled.

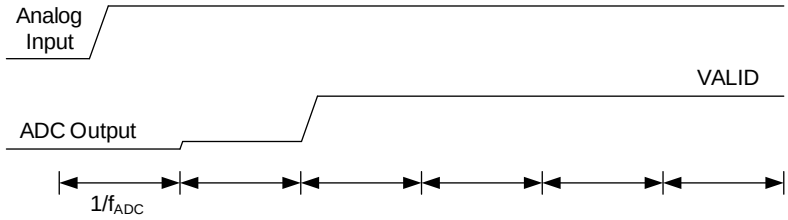


Figure 47: Step Change on the Analog Input, Sinc^3 + Sinc^1 Filter

9.5.4.2 Sequencer

The description in the Fast-Settling Mode (Sinc^3 + Sinc^1 Filter) section is valid when manually switching channels, for example, writing to the device to change channels. When multiple channels are enabled, the on-chip sequencer is automatically used; the device automatically sequences between all enabled channels. In this case, the first conversion takes the complete settling time as listed in Table 46. For all subsequent conversions, the time needed for each conversion is also the settling time, but the dead time is reduced to:

- In Full Power Mode, Dead Time = 86;
- In Mid Power Mode, Dead Time = 51 when FS[10:0] = 1, and Dead Time = 39 when FS[10:0] > 1;
- In Low Power Mode, Dead Time = 25.

9.5.5 POST FILTERS

The post filters provide rejection of 50 Hz and 60 Hz simultaneously and allow the user to trade off settling time and rejection. These filters can operate up to 27.27 SPS or can reject up to 90 dB of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz interference. These filters are realized by post filtering the output of the sinc^3 filter. The filter bits must be set to all 1s to enable the post filter. The post filter option to use is selected using the POST_FILTER bits in the filter register. In Figure 48, the blocks shown in gray are unused.

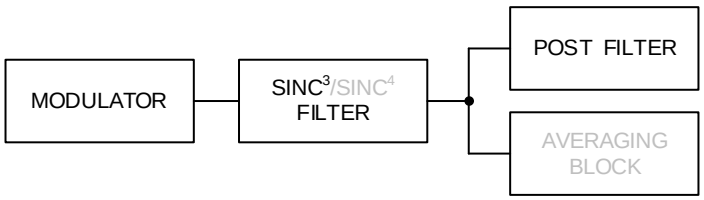


Figure 48: Post Filters

Table 47 shows the output data rates with the accompanying settling times and the rejection.

When continuously converting on a single channel, the first conversion requires a time of t_{SETTLE}. Subsequent conversions occur at $1/f_{ADC}$. When multiple channels are enabled(either manually or using the sequencer), the settling time is required to generate a valid conversion on each enabled channel.

Table 47: Post Filters, Output Data Rate, Setting Time(t_{SETTLE}), and Rejection

Output Data Rate (SPS)	f_{3dB} (Hz)	t_{SETTLE}, Full Power Mode(ms)	t_{SETTLE}, Mid Power Mode(ms)	t_{SETTLE}, Low Power Mode(ms)	Simultaneous Rejection of 50Hz ± 1 Hz and 60 Hz ± 1 Hz(dB)[1]
27.27	17.28	38.364	38.457	38.372	47
25	15.12	41.704	41.816	41.758	62
20	13.38	51.717	51.868	51.862	86
16.67	12.66	61.715	61.862	61.849	92

1. Stable master clock used.

9.5.6 50Hz and 60Hz Line Cycle Rejection(NMRR) for Different Filters

If the ADC connection leads are in close proximity to industrial motors and conductors, coupling of 50Hz and 60Hz power line frequencies can occur. The coupled noise interferes with the signal voltage, and can lead to inaccurate or unstable conversions. The digital filter provides rejection of power-line-coupled noise for data rates of 60 SPS and less. Different filter architecture and different data rate will have different rejection. Table 48 summarize the ADC 50Hz and 60Hz line-cycle rejection for different filters. The best possible power-line rejection is provided by using an accurate ADC clock.

Table 48: 50Hz and 60Hz Line Cycle Rejection for different filter

Filter	Power Mode	Output Data Rate(SPS)	REJ60	50Hz Rejection(dB)[1,2]
Sinc4	All	10	0	120 dB (50 Hz and 60 Hz)
	All	50	0	120 dB (50 Hz only)
	All	50	1	75 dB (50 Hz and 60 Hz)
	All	60	0	120 dB (60 Hz only)
Sinc4, Zero Latency	All	12.5	0	120 dB (50 Hz only)
	All	12.5	1	75 dB (50 Hz and 60 Hz)
	All	15	0	120 dB (60 Hz only)
Sinc3	All	10	0	100 dB (50 Hz and 60 Hz)
	All	50	0	95 dB (50 Hz only)
	All	50	1	61 dB (50 Hz and 60 Hz)
	All	60	0	95 dB (60 Hz only)
Fast Setting(Sinc4 + Sinc1)	Full / mid	60	0	40 dB (60 Hz only)
	Low	50	0	40 dB (60 Hz only)
	Full / mid	50	0	40 dB (50 Hz only)
	Low	50	0	40 dB (50 Hz only)
	Full / mid	10	0	40 dB (50 Hz and 60 Hz)
	Low	10	0	40 dB (50 Hz and 60 Hz)
Fast Setting(Sinc3 + Sinc1)	Full / mid	60	0	40 dB (60 Hz only)
	Low	60	0	40 dB (60 Hz only)
	Full / mid	50	0	40 dB (50 Hz only)
	Low	50	0	40 dB (50 Hz only)
	Full / mid	10	0	40 dB (50 Hz and 60 Hz)
	Low	10	0	40 dB (50 Hz and 60 Hz)
Post Filter	All	27.27	0	48 dB (50 Hz and 60 Hz)
	All	25	0	63 dB (50 Hz and 60 Hz)
	All	20	0	88 dB (50 Hz and 60 Hz)
	All	16.67	0	93 dB (50 Hz and 60 Hz)

1. These calculations assume a stable master clock.
2. For fast settling mode, the 50 Hz/60 Hz rejection is measured in a band of ±0.5 Hz around 50 Hz and/or 60 Hz. For all other modes, a region of ±1 Hz around 50 Hz and/or 60 Hz is used.

9.6 DIAGNOSTICS

The AD7124 has numerous diagnostic functions on chip. Use these features to ensure :

- Read/write operations are to valid registers only
- Only valid data is written to the on-chip registers
- The external reference, if used, is present
- The ADC modulator and filter are working within specification

9.6.1 CALIBRATION, CONVERSION, AND SATURATION ERRORS

The conversion process and calibration process can also be monitored by the AD7124-8. These diagnostics check the analog input used as well as the modulator and digital filter during conversions or calibration. The functions can be enabled using the ADC_CAL_ERR_EN, ADC_CONV_ERR_EN, and ADC_SAT_ERR_EN bits in the ERROR_EN register. With these functions enabled, the ADC_ CAL_ERR, ADC_CONV_ERR, and ADC_SAT_ERR bits are set if an error occurs.

The ADC_CONV_ERR flag is set if there is an overflow or under- flow in the digital filter. The ADC conversion clamps to all 0s or all 1s also. This flag is updated in conjunction with the update of the data register and can be cleared only by a read of the error register.

The ADC_SAT_ERR flag is set if the modulator outputs 20 consecutive 1s or 0s. This indicates that the modulator has saturated.

When an offset calibration is performed, the resulting offset coefficient must be between 0x7FFFF and 0xF80000. If the coefficient is outside this range, the offset register is updated anyway and the ADC_CAL_ERR flag is set. During a full-scale calibration, overflow of the digital filter is checked. If an overflow occurs, the error flag is set and the gain register is updated any way.

9.6.2 POWER SUPPLY MONITORS

Along with converting external voltages, the ADC can monitor the voltage on the AVDD pin and the IOVDD pin. When the inputs of AVDD to AVSS or IOVDD to DGND are selected, the voltage (AVDD to AVSS or IOVDD to DGND) is internally attenuated by 6, and the resulting voltage is applied to the Σ-Δ modulator. This is useful because variations in the power supply voltage can be monitored.

9.6.3 MCLK COUNTER

A stable master clock is important as the output data rate, filter settling time, and the filter notch frequencies are dependent on the master clock. The AD7124-8 allows the user to monitor the master clock. When the MCLK_CNT_EN bit in the ERROR_EN register is set, the MCLK_COUNT register increments by 1 every 131 master clock cycles. The user can monitor this register over a fixed period of time. The master clock frequency can be determined from the result in the MCLK_COUNT register. The MCLK_COUNT register wraps around after it reaches its maximum value.

Note that the incrementation of the register is asynchronous to the register read. If a register read coincides with the register incrementation, it is possible to read an invalid value. To prevent this, read the register four times rather than once, then read the register four times again at a later point. By reading four values, it is possible to identify the correct register value at the start and at the end of the timing instants.

9.6.4 SPI SCLK COUNTER

The SPI SCLK counter counts the number of SCLK pulses used in each read and write operation. $\overline{CS}$ must frame every read and write operation when this function is used. All read and write operations are multiples of eight SCLK pulses (8, 16, 32, 40, 48). If the SCLK counter counts the SCLK pulses and the result is not a multiple of eight, an error is flagged; the SPI_SCLK_CNT_ERR bit in the error register is set. If a write operation is being performed and the SCLK contains an incorrect number of SCLK pulses, the value is not written to the addressed register and the write operation is aborted.

The SCLK counter is enabled by setting the SPI_SCLK_ CNT_ERR_EN bit in the ERROR_EN register.

9.6.5 SPI READ/WRITE ERRORS

Along with the SCLK counter, the AD7124-8 can also check the read and write operations to ensure that valid registers are being addressed. When the SPI_READ_ERR_EN bit or the SPI_ WRITE_ERR_EN bit in the ERROR_EN register are set, the AD7124-8 checks the a ddress of the read/write operations. If the user attempts to write to or read from any register other than the user registers described in this data sheet, an error is flagged; the SPI_READ_ERR bit or the SPI_WRITE_ERR bit in the error register is set and the read/write operation is aborted.

This function, along with the SCLK counter and the CRC, makes the serial interface more robust. Invalid registers are not written to or read from. An incorrect number of SCLK pulses can cause the serial interface to go asynchronous and incorrect registers to be accessed. The AD7124 protects against these issues via the diagnostics.

9.6.6 SPI_IGNORE ERROR

At certain times, the on-chip registers are not accessible. For example, during power-up, the on-chip registers are set to their default values. The user must wait until this operation is complete before writing to registers. Also, when offset or gain calibrations are being performed, registers cannot be accessed. If the user writes to registers during these busy periods, the SPI_IGNORE_ERR flag is set, indicating that the ADC is busy, and the write operation is ignored. The SPI_IGNORE_ERR flag is cleared when the bit is read. This diagnostic is enabled by default. The function can be disabled using the SPI_IGNORE_ERR_EN bit in the ERROR_EN register.

9.6.7 CHECKSUM PROTECTION

The AD7124-8 has a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERR bit is set in the error register. However, to ensure that the register write was successful, read back the register and verify the checksum.

For CRC checksum calculations, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

The CRC_ERR_EN bit in the ERROR_EN register enables and disables the checksum.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit to 32-bit data output. Figure 49 and Figure 50 show SPI write and read transactions, respectively.

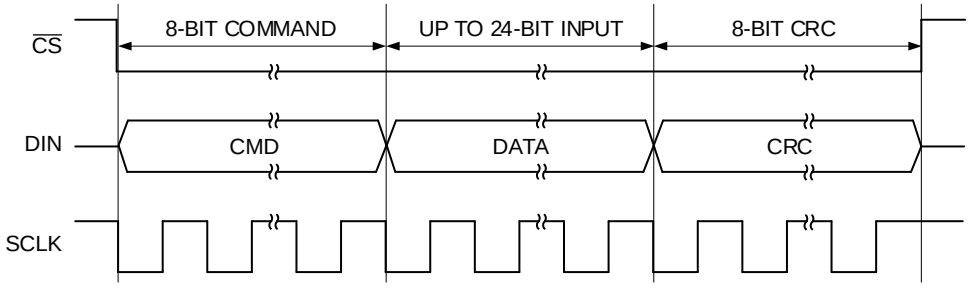


Figure 49: SPI Write Transaction with CRC

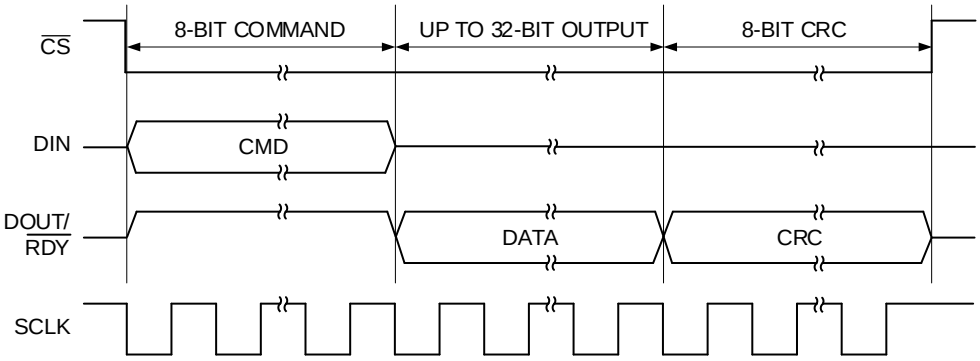


Figure 50: SPI Read Transaction with CRC

If checksum protection is enabled when continuous read mode is active, there is an implied command of 0x99 before every data transmission that must be accounted for when calculating the checksum value. This ensures a nonzero checksum value even if the ADC data equals 0x000000.

9.6.8 MEMORY MAP CHECKSUM PROTECTION

For added robustness, a CRC calculation is performed on the on-chip registers as well. The status register, data register, error register, MCLK counter register, offset registers, and gain registers are not included in this check because their contents change continuously. The CRC is performed at a rate of 1/2400 seconds. Each time that the memory map is accessed, the CRC is recalculated. Events that cause the CRC to be recalculated are:

- A user write
- An offset/full-scale calibration

- When the device is operated in single conversion mode and the ADC goes into standby mode following the completion of the conversion
- When exiting continuous read mode (the CONT_READ bit in the ADC_CONTROL register is set to 0)

The memory map CRC function is enabled by setting the MM_ CRC_ERR_EN bit in the ERROR_EN register to 1. If an error occurs, the MM_CRC_ERR bit in the error register is set to 1.

9.6.9 CRC Calculation

The checksum, which is 8 bits wide, is generated using the polynomial:

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

Initial value	011001010100001100100001	Initial value = 0x654321
	011001010100001100100001**00000000**	left shifted eight bits
$x^8 + x^2 + x + 1 = 100000111$	100000111	polynomial
	001001000001100100001**00000000**	XOR result
	100000111	polynomial
	000110001100100001**00000000**	XOR result
	100000111	polynomial
	111111100100001**00000000**	XOR result
	100000111	polynomial
	111110111000010**0000000**	XOR result
	100000111	polynomial
	111100000000100**0000000**	XOR result
	100000111	polynomial
	111001110001000**0000000**	XOR result
	100000111	polynomial
	110010010010000**0000000**	XOR result
	100000111	polynomial
	100101010100000**0000000**	XOR result
	100000111	polynomial
	101101100000**0000000**	XOR result
	100000111	polynomial
	1101011000**0000000**	XOR result
	100000111	polynomial
	101010110**0000000**	XOR result
	100000111	polynomial
	101000100**0000000**	XOR result
	100000111	polynomial
	10000110**0000000**	checksum = 0x86

9.6.10 BURNOUT CURRENTS

The AD7124-8 contains two constant current generators that can be programmed to 0.5 µA, 2 µA, or 4 µA. One generator sources current from AVDD to AINP, and one sinks current from AINM to AVSS. These currents enable open wire detection.

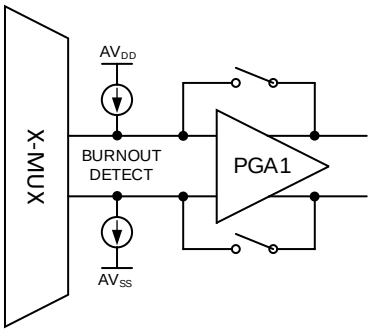


Figure 51: Burnout Currents

The currents are switched to the selected analog input pair. Both currents are either on or off. The burnout bits in the configuration register enable/disable the burnout currents along with setting the amplitude. Use these currents to verify that an external transducer is still operational before attempting to take measurements on that channel. After the burnout currents are turned on, they flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resulting voltage measured is near full scale, the user must verify why this is the case. A near full-scale reading can mean that the front-end sensor is open circuit. It can also mean that the front-end sensor is overloaded and is justified in outputting full scale, or that the reference may be absent, thus clamping the data to all 1s.

When a conversion is close to full scale, the user must check these three cases before making a judgment. If the voltage measured is 0 V, it may indicate that the transducer has short circuited. For normal operation, these burnout currents are turned off by setting the burnout bits to zero. The current sources work over the normal absolute input voltage range specifications with buffers on.

9.6.11 TEMPERATURE SENSOR

Embedded in the AD7124 is a temperature sensor that is useful to monitor the die temperature. This is selected using the AINP[4:0] and AINM[4:0] bits in the channel register.

The sensitivity is 13,584 codes/°C, approximately. The equation for the temperature sensor is:

$$T(℃) = \big((Conversion - 0x800000)/13{,}584\big) - 272.5$$

The temperature sensor has an accuracy of ±1.0°C typically.

10 Detailed Description

10.1 Register Map

10.1.1 AD7124-8 Register Map

Addr.	Name	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	COMMS	W	0x00	$\overline{WEN}$	R/$\overline{W}$	RS[5:0]					
0x00	STATUS	R	0x80	$\overline{RDY}$	ERROR_FLAG	0	POR_FLAG	CH_ACTIVE			
0x01	ADC_ CONTROL	R/W	0x0000	0			DOUT_$\overline{RDY}$_DEL	CONT_READ	DATA_STATUS	$\overline{CS}$_EN	REF_EN
				POWER_MODE		MODE				CLK_SEL	
0x02	Data	R	0x000000	DATA[23:0]							
0x03	IO_ CONTROL_1	R/W	0x000000	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1
				PDSW	0	IOUT1			IOUT0		
				IOUT1_CH				IOUT0_CH			
0x04	IO_ CONTROL_2	R/W	0x0000	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8
				VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0

0x05	ID	R	0x14	DEVICE_ID					SILICON_REVISION			
0x06	ERROR	R	0x000000	0				0	ADC_CAL_ERR	ADC_CONV_ERR	ADC_SAT_ERR	
				0	0	0	0	0	0	0	0	
				0	SPI_IGNORE_ERR	SPI_SCLK_CNT_ERR	SPI_READ_ERR	SPI_WRITE_ERR	SPI_CRC_ERR	MM_CRC_ERR	0	
0x07	ERROR_EN	R/W	0x000040	0	MCLK_CNT_EN	0	0		ADC_CAL_ERR_EN	ADC_CONV_ERR_EN	ADC_SAT_ERR_EN	
				0	0	0	0	0	0	0	0	
				0	SPI_IGNORE_ERR_EN	SPI_SCLK_CNT_ERR_EN	SPI_READ_ERR_EN	SPI_WRITE_ERR_EN	SPI_CRC_ERR_EN	MM_CRC_ERR_EN	0	
0x08	MCLK_COUNT	R	0x00	MCLK_COUNT								
0x09 ~ 0x18	CHANNEL0~15	R/W	0x8001 0x0001	ENABLE	SETUP			0		AINP[4:3]		
				AINP[2:0]			AINM[4:0]					
0x19 ~ 0x20	CONFIG0~7	R/W	0x0860	0				BIPOLAR	BURNOUT		REF_BUFP	
				REF_BUFM	PGA_CONTROL		REF_SEL		PGA			
0x21 ~ 0x28	FILTER0~7	R/W	0x060180	Filter			REJ60	POST_FILTER			SINGLE_CYCLE	
				0					FS[10:8]			
				FS[7:0]								
0x29 ~ 0x30	OFFSET0~7	R/W	0x800000	Offset[23:16]								
				Offset[15:8]								
				Offset[7:0]								
0x31 ~ 0x38	GAIN0~7	R/W	0x500000	Gain[23:16]								
				Gain[15:8]								
				Gain[7:0]								

CHANNEL_0 is reset to 0x8001. All other channels are reset to 0x0001.

10.1.2 AD7124-8 Detailed Register Definitions

10.1.2.1 *COMMS—COMMUNICATIONS REGISTER (Addr = 00h) [reset = 00h]*

The communications register is an 8-bit, write only register. All communications to the device must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place, the RS[5:0] bits selecting the register to be accessed.
For read or write operations, after the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset,the ADC is in this default state waiting for a write aperation to the communications tegister.
In situations where the interface sequence is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire device. Below Table outlines the bit designations for the communications register. Bit 7 denotes the first bit of the data stream.

Addr	Bit	Default	Field	Type	Description
00h	7	0	$\overline{WEN}$	W	Write enable bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the device does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. As soon as a 0 is written to the $\overline{WEN}$ bit, the next seven bits are loaded to the communications register.
	6	0	R/$\overline{W}$	W	A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
	5:0	000000	RS[5:0]	W	Register address bits. These address bits select which registers of the ADC are being selected during this serial interface communication.

10.1.2.2 *STATUS—STATUS REGISTER (Addr = 01h) [reset = 80h]*

The status register is an 8-bit, read only register. To access the ADC status register, the user must write to the communications register, select the next operation to be read, and set the register address bits RS[5:0] to 0.
Below Table outlines the bit designations for the status register. Bit 7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
00h	7	1	$\overline{\text{RDY}}$	R	Ready bit for the ADC. This bit is cleared when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register is read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the device is placed in power-down or standby mode. The end of a conversion is also indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
	6	0	ERROR_FLAG	R	ADC error bit. This bit indicates if one of the error bits has been asserted in the error register. This bit is high if one or more of the error bits in the error register has been set. This bit is cleared by a read of the error register.
	5	0		R	This bit is set to 0.
	4	0	POR_FLAG	R	Power-on reset flag. This bit indicates that a power-on reset has occurred. A power-on reset occurs on power-up, when the power supply voltage goes below a threshold voltage, when a reset is performed, and when coming out of power-down mode. The status register must be read to clear the bit.
	3:0	0000	CH_ACTIVE	R	These bits indicate which channel is being converted by the ADC. 0000 = Channel 0. 0001 = Channel 1. 0010 = Channel 2. 0011 = Channel 3. 0100 = Channel 4. 0101 = Channel 5. 0110 = Channel 6. 0111 = Channel 7. 1000 = Channel 8. 1001 = Channel 9. 1010 = Channel 10. 1011 = Channel 11. 1100 = Channel 12. 1101 = Channel 13. 1110 = Channel 14. 1111 = Channel 15.

10.1.2.3 *ADC_CONTROL REGISTER (Addr = 01h) [reset = 0000h]*

Below Table outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
01h	15:13	00		R	These bits must be programmed with a Logic 0 for correct operation.
	12	0	DOUT_$\overline{\text{RDY}}$ _DEL	R/W	Controls the SCLK inactive edge to DOUT/$\overline{\text{RDY}}$ high time. When DOUT_$\overline{\text{RDY}}$_DEL is cleared, the delay is 10 ns minimum. When DOUT_$\overline{\text{RDY}}$_DEL is set, the delay is increased to 100 ns minimum. This function is useful when $\overline{\text{CS}}$ is tied low (the $\overline{\text{CS}}$_EN bit is set to 0).
	11	0	CONT_READ	R/W	Continuous read of the data register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read; that is, the contents of the data register are automatically placed on the DOUT pin when the SCLK pulses are applied after the $\overline{\text{RDY}}$ pin goes low to indicate

					that a conversion is complete. The communications register does not have to be written to for subsequent data reads. To enable continuous read, the CONT_READ bit is set. To disable continuous read, write a read data command while the DOUT/ $\overline{RDY}$ pin is low. While continuous read is enabled, the ADC monitors activity on the DIN line so that it can receive the instruction to disable continuous read. Additionally, a reset occurs if 64 consecutive 1s occur on DIN; therefore, hold DIN low until an instruction is written to the device.
	10	0	DATA_STATUS	R/W	This bit enables the transmission of the status register contents after each data register read. When DATA_STATUS is set, the contents of the status register are transmitted along with each data register read. This function is useful when several channels are selected because the status register identifies the channel to which the data register value corresponds.
	9	0	$\overline{CS}$_EN	R/W	This bit controls the operation of the DOUT/$\overline{RDY}$ pin during read operations. When $\overline{CS}$_EN is cleared, the DOUT pin returns to being a $\overline{RDY}$ pin within nanoseconds of the SCLK inactive edge (the delay is determined by the DOUT_$\overline{RDY}$_DEL bit). When set, the DOUT/$\overline{RDY}$ pin continues to output the LSB of the register being read until $\overline{CS}$ is taken high. $\overline{CS}$ must frame all read operations when $\overline{CS}$_EN is set. $\overline{CS}$_EN must be set to use the diagnostic functions SPI_WRITE_ERR, SPI_READ_ERR, and SPI_SCLK_CNT_ERR.
	8	0	REF_EN	R/W	Internal reference voltage enable. When this bit is set, the internal reference is enabled and available at the REFOUT pin. When this bit is cleared, the internal reference is disabled.
	7:6	00	POWER_MODE	R/W	Power Mode Select. These bits select the power mode. The current consumption and output data rate ranges are dependent on the power mode. 00 = low power. 01 = mid power. 10 = full power. 11 = full power.
	5:2	0000	MODE	R/W	These bits control the mode of operation for ADC. See Operating Modes Table below.
	1:0	00	CLK_SEL	R/W	These bits select the clock source for the ADC. Either the on-chip 614.4 kHz clock can be used or an external clock can be used. The ability to use an external clock allows several AD7124 devices to be synchronized. Also, 50 Hz and 60 Hz rejection is improved when an accurate external clock drives the ADC. 00 = internal 614.4 kHz clock. The internal clock is not available at the CLK pin. 01 = internal 614.4 kHz clock. This clock is available at the CLK pin. 10 = external 614.4 kHz clock. 11 = external clock. The external clock is divided by 4 within the AD7124

Operating Modes

Mode Value	Description
0000	Continuous conversion mode (default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{RDY}$ goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, a reset, or a reconfiguration of the ADC, the complete settling time of the filter is required to generate the first valid conversion. Subsequent conversions are available at the selected output data rate, which is dependent on filter choice.

0001	Single conversion mode. When single conversion mode is selected, the ADC powers up and performs a single conversion on the selected channel. The conversion requires the complete settling time of the filter. The conversion result is placed in the data register, $\overline{RDY}$ goes low, and the ADC returns to standby mode. The conversion remains in the data register and $\overline{RDY}$ remains active (low) until the data is read or another conversion is performed.
0010	Standby mode. In standby mode, all sections of the AD7124 can be powered down except the LDOs. The internal reference, on-chip oscillator, low-side power switch, and bias voltage generator can be enabled or disabled while in standby mode. The on-chip registers retain their contents in standby mode. Any enabled diagnostics remain active when the ADC is in standby mode. The diagnostics can be enabled/disabled while in standby mode. However, any diagnostics that require the master clock (reference detect, undervoltage/overvoltage detection, LDO trip tests, memory map CRC, and MCLK counter) must be enabled when the ADC is in continuous conversion mode or idle mode; these diagnostics do not function if enabled in standby mode.
0011	Power-down mode. In power-down mode, all the AD7124 circuitry is powered down, including the current sources, power switch, burnout currents, bias voltage generator, and clock circuitry. The LDOs are also powered down. In power-down mode, the on-chip registers do not retain their contents. Therefore, coming out of power-down mode, all registers must be reprogrammed.
0100	Idle mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks continue to be provided.
0101	Internal zero-scale (offset) calibration. An internal short is automatically connected to the input. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. Select only one channel when zero-scale calibration is being performed. An internal zero-scale calibration takes a time of one settling period to be performed.
0110	Reserved, The AD7124 is factory calibrated for all gains.
0111	System zero-scale (offset) calibration. Connect the system zero-scale input to the channel input pins of the selected channel. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. A system zero-scale calibration is required each time the gain of a channel is changed. Select only one channel when full-scale calibration is being performed. A system zero-scale calibration takes a time of one settling period to be performed.
1000	System full-scale (gain) calibration. Connect the system full-scale input to the channel input pins of the selected channel. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the gain register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed. Select only one channel when full-scale calibration is being performed. A system full-scale calibration takes a time of one settling period to be performed.
1001 to 1111	Reserved

10.1.2.4 *DATA REGISTER (Addr = 02h) [reset = 000000h]*

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.

10.1.2.5 *IO_CONTROL_1 REGISTER (Addr = 03h) [reset = 000000h]*

Below Table outlines the bit designations for the register. Bit 23 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
03h	23	0	GPIO_DAT4	R/W	Digital Output P4. When GPIO_CTRL4 is set, the GPIO_DAT4 bit sets the value of the P4 general-purpose output pin. When GPIO_DAT4 is high, the P4 output pin is high. When GPIO_DAT4 is low, the P4 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT4 bit reflects the status of the P4 pin if GPIO_CTRL4 is set.
	22	0	GPIO_DAT3	R/W	Digital Output P3. When GPIO_CTRL3 is set, the GPIO_DAT3 bit sets the value of the P3 general-purpose output pin. When GPIO_DAT3 is high, the P3 output pin is high. When GPIO_DAT3 is low, the P3 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT3 bit reflects the status of the P3 pin if GPIO_CTRL3 is set.

	21	0	GPIO_DAT2	R/W	Digital Output P2. When GPIO_CTRL2 is set, the GPIO_DAT2 bit sets the value of the P2 general-purpose output pin. When GPIO_DAT2 is high, the P2 output pin is high. When GPIO_DAT2 is low, the P2 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT2 bit reflects the status of the P2 pin if GPIO_CTRL2 is set.
	20	0	GPIO_DAT1	R/W	Digital Output P1. When GPIO_CTRL1 is set, the GPIO_DAT1 bit sets the value of the P1 general-purpose output pin. When GPIO_DAT1 is high, the P1 output pin is high. When GPIO_DAT1 is low, the P1 output pin is low. When the IO_CONTROL_1 register is read, the GPIO_DAT1 bit reflects the status of the P1 pin if GPIO_CTRL1 is set.
	19	0	GPIO_CTRL4	R/W	Digital Output P4 enable. When GPIO_CTRL4 is set, the digital output P4 is active. When GPIO_CTRL4 is cleared, the pin functions as analog input pin AIN5.
	18	0	GPIO_CTRL3	R/W	Digital Output P3 enable. When GPIO_CTRL3 is set, the digital output P3 is active. When GPIO_CTRL3 is cleared, the pin functions as analog input pin AIN4.
	17	0	GPIO_CTRL2	R/W	Digital Output P2 enable. When GPIO_CTRL2 is set, the digital output P2 is active. When GPIO_CTRL2 is cleared, the pin functions as analog input pin AIN3.
	16	0	GPIO_CTRL1	R/W	Digital Output P1 enable. When GPIO_CTRL1 is set, the digital output P1 is active. When GPIO_CTRL1 is cleared, the pin functions as analog input pin AIN2.
	15	0	PDSW	R/W	Bridge power-down switch control bit. Set this bit to close the bridge power-down switch PDSW to AGND. The switch can sink up to 30 mA. Clear this bit to open the bridge power-down switch. When the ADC is placed in standby mode, the bridge power-down switch remains active.
	14	0		R/W	This bit must be programmed with a Logic 0 for correct operation.
	13:11	000	IOUT1	R/W	These bits set the value of the excitation current for IOUT1. 000 = off. 001 = 50 µA. 010 = 100 µA 011 = 250 µA. 100 = 500 µA. 101 = 750 µA. 110 = 1000 µA. 111 = 10 µA.
	10:8	000	IOUT0	R/W	These bits set the value of the excitation current for IOUT0. 000 = off. 001 = 50 µA. 010 = 100 µA 011 = 250 µA. 100 = 500 µA. 101 = 750 µA. 110 = 1000 µA. 111 = 10 µA.
	7:4	0000	IOUT1_CH	R/W	Channel select bits for the excitation current for IOUT1. 0000 = IOUT1 is available on the AIN0 pin. 0001 = IOUT1 is available on the AIN1 pin. 0010 = IOUT1 is available on the AIN2 pin. 0011 = IOUT1 is available on the AIN3 pin. 0100 = IOUT1 is available on the AIN4 pin. 0101 = IOUT1 is available on the AIN5 pin. 0110 = IOUT1 is available on the AIN6 pin. 0111 = IOUT1 is available on the AIN7 pin. 1000 = IOUT1 is available on the AIN8 pin. 1001 = IOUT1 is available on the AIN9 pin. 1010 = IOUT1 is available on the AIN10 pin. 1011 = IOUT1 is available on the AIN11 pin. 1100 = IOUT1 is available on the AIN12 pin. 1101 = IOUT1 is available on the AIN13 pin. 1110 = IOUT1 is available on the AIN14 pin. 1111 = IOUT1 is available on the AIN15 pin.

	3:0	0000	IOUT0_CH	R/W	Channel select bits for the excitation current for IOUT0. 0000 = IOUT0 is available on the AIN0 pin. 0001 = IOUT0 is available on the AIN1 pin. 0010 = IOUT0 is available on the AIN2 pin. 0011 = IOUT0 is available on the AIN3 pin. 0100 = IOUT0 is available on the AIN4 pin. 0101 = IOUT0 is available on the AIN5 pin. 0110 = IOUT0 is available on the AIN6 pin. 0111 = IOUT0 is available on the AIN7 pin. 1000 = IOUT0 is available on the AIN8 pin. 1001 = IOUT0 is available on the AIN9 pin. 1010 = IOUT0 is available on the AIN10 pin. 1011 = IOUT0 is available on the AIN11 pin. 1100 = IOUT0 is available on the AIN12 pin. 1101 = IOUT0 is available on the AIN13 pin. 1110 = IOUT0 is available on the AIN14 pin. 1111 = IOUT0 is available on the AIN15 pin.

10.1.2.6 *IO_CONTROL_2 Register (Addr = 04h) [reset = 0000h]*

Below Table outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. The internal bias voltage can be enabled on multiple channels.

Addr	Bit	Default	Field	Type	Description
04h	15	0	VBIAS15	R/W	Enable the bias voltage on the AIN15 channel. When set, the internal bias voltage is available on AIN15.
	14	0	VBIAS14	R/W	Enable the bias voltage on the AIN14 channel. When set, the internal bias voltage is available on AIN14.
	13	0	VBIAS13	R/W	Enable the bias voltage on the AIN13 channel. When set, the internal bias voltage is available on AIN13.
	12	0	VBIAS12	R/W	Enable the bias voltage on the AIN12 channel. When set, the internal bias voltage is available on AIN12.
	11	0	VBIAS11	R/W	Enable the bias voltage on the AIN11 channel. When set, the internal bias voltage is available on AIN11.
	10	0	VBIAS10	R/W	Enable the bias voltage on the AIN10 channel. When set, the internal bias voltage is available on AIN10.
	9	0	VBIAS9	R/W	Enable the bias voltage on the AIN9 channel. When set, the internal bias voltage is available on AIN9.
	8	0	VBIAS8	R/W	Enable the bias voltage on the AIN8 channel. When set, the internal bias voltage is available on AIN8.
	7	0	VBIAS7	R/W	Enable the bias voltage on the AIN7 channel. When set, the internal bias voltage is available on AIN7.
	6	0	VBIAS6	R/W	Enable the bias voltage on the AIN6 channel. When set, the internal bias voltage is available on AIN6.
	5	0	VBIAS5	R/W	Enable the bias voltage on the AIN5 channel. When set, the internal bias voltage is available on AIN5.
	4	0	VBIAS4	R/W	Enable the bias voltage on the AIN4 channel. When set, the internal bias voltage is available on AIN4.
	3	0	VBIAS3	R/W	Enable the bias voltage on the AIN3 channel. When set, the internal bias voltage is available on AIN3.
	2	0	VBIAS2	R/W	Enable the bias voltage on the AIN2 channel. When set, the internal bias voltage is available on AIN2.
	1	0	VBIAS1	R/W	Enable the bias voltage on the AIN1 channel. When set, the internal bias voltage is available on AIN1.
	0	0	VBIAS0	R/W	Enable the bias voltage on the AIN0 channel. When set, the internal bias voltage is available on AIN0.

10.1.2.7 *ID Register (Addr = 05h) [reset = 14h]*

The identification number for the AD7124 is stored in the ID register. This is a read only register.

10.1.2.8 *ERROR Register (Addr = 06h) [reset = 000000h]*

Diagnostics, such as checking checking the SPI interface, are included on the AD7124 . The error register contains the flags for the different diagnostic functions. The functions are enabled and disabled using the ERROR_EN register.
Below Table outlines the bit designations for the register. Bit 23 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
06h	23:20	0000	RESERVED	R	These bits must be programmed with a Logic 0 for correct operation.
	19	0	RESERVED	R	These bits must be programmed with a Logic 0 for correct operation.
	18	0	ADC_CAL_ERR	R	Calibration check. If a calibration is initiated but not completed, this flag is set to indicate that an error occurred during the calibration. The associated calibration register is updated anyway.
	17	0	ADC_CONV_ERR	R	This bit indicates whether a conversion is valid. This flag is set if an error occurs during a conversion.
	16	0	ADC_SAT_ERR	R	ADC saturation flag. This flag is set if the modulator is saturated during a conversion.
	15	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	14	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	13	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	12	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	11	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	10	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	9	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	8	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	7	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	6	0	SPI_IGNORE_ERR	R	During power-on reset and calibrations, the on-chip registers cannot be written to. User write instructions are ignored by the ADC. This bit is set, indicating that the ADC is busy and the write instruction has been ignored. The SPI_IGNORE_ERR bit is cleared when read.
	5	0	SPI_SCLK_CNT_ERR	R	All serial communications are some multiple of eight bits. This bit is set when the number of SCLK cycles is not a multiple of eight.
	4	0	SPI_READ_ERR	R	This bit is set when an error occurs during an SPI read operation.
	3	0	SPI_WRITE_ERR	R	This bit is set when an error occurs during an SPI write operation.
	2	0	SPI_CRC_ERR	R	This bit is set if an error occurs in the CRC check of the serial communications.
	1	0	MM_CRC_ERR	R	Memory map error. A CRC calculation is performed on the memory map each time that the registers are written to. Following this, periodic CRC checks are performed on the on-chip registers. If the register contents have changed, the MM_CRC_ERR bit is set.
	0	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.

10.1.2.9 *ERROR_EN Register (Addr = 07h) [reset = 000040h]*

All the diagnostic functions can be enabled or disabled by setting the appropriate bits in this register.

Below Table outlines the bit designations for the register. Bit 23 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
07h	23	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	22	0	MCLK_CNT_EN	R/W	Master clock counter. When this bit is set, the master clock counter is enabled and the result is reported via the MCLK_COUNT register. The counter monitors the master clock being used by the ADC. If an external clock is the clock source, the MCLK counter monitors this external clock. Similarly, if the on-chip oscillator is selected as the clock source to the ADC, the MCLK counter monitors the on-chip oscillator.
	21	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	20:19	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	18	0	ADC_CAL_ERR_EN	R/W	When this bit is set, the calibration fail check is enabled.
	17	0	ADC_CONV_ERR_EN	R/W	When this bit is set, the conversions are monitored and the ADC_CONV_ERR bit is set when a conversion fails.
	16	0	ADC_SAT_ERR_EN	R/W	When this bit is set, the ADC modulator saturation check is enabled.
	15	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	14	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	13	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	12	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	11	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	10	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	9	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	8	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	7	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.
	6	0	SPI_IGNORE_ERR_EN	R/W	During power-on reset and calibrations, the on-chip registers cannot be written to. User write instructions are ignored by the ADC. Set this bit so that the SPI_IGNORE_ERR bit in the error register informs the user when write operations are ignored.
	5	0	SPI_SCLK_CNT_ERR_EN	R/W	When this bit is set, the SCLK counter is enabled. All read and write operations to the ADC are multiples of eight bits. For every serial communication, the SCLK counter counts the number of SCLK pulses. $\overline{CS}$ must be used to frame each read and write operation. If the number of SCLK pulses used during a communication is not a multiple of eight, the SPI_SCLK_CNT_ERR bit in the error register is set. For example, a glitch on the SCLK pin during a read or write operation can be interpreted as an SCLK pulse. In this case, the SPI_SCLK_CNT_ERR bit is set as there is an excessive number of SCLK pulses detected. $\overline{CS}$_EN in the ADC_CONTROL register

					must be set to 1 when the SCLK counter function is being used.
	4	0	SPI_READ_ERR_EN	R/W	When this bit is set, the SPI_READ_ERR bit in the error register is set when an error occurs during a read operation. An error occurs if the user attempts to read from invalid addresses. $\overline{CS}$_EN in the ADC_CONTROL register must be set to 1 when the SPI read check function is being used.
	3	0	SPI_WRITE_ERR_EN	R/W	When this bit is set, the SPI_WRITE_ERR bit in the error register is set when an error occurs during a write operation. An error occurs if the user attempts to write to invalid addresses or write to read-only registers. $\overline{CS}$ _EN in the ADC_CONTROL register must be set to 1 when the SPI write check function is being used.
	2	0	SPI_CRC_ERR_EN	R/W	This bit enables a CRC check of all read and write operations. The SPI_CRC_ERR bit in the error register is set if the CRC check fails. In addition, an 8-bit CRC word is appended to all data read from the AD7124
	1	0	MM_CRC_ERR_EN	R/W	When this bit is set, a CRC calculation is performed on the memory map each time that the registers are written to. Following this, periodic CRC checks are performed on the on-chip registers. If the register contents have changed, the MM_CRC_ERR bit is set.
	0	0	RESERVED	R	This bit must be programmed with a Logic 0 for correct operation.

10.1.2.10 *MCLK_COUNT Register (Addr = 08h) [reset = 00h]*

The master clock frequency can be monitored using this register.
Below Table outlines the bit designations for the register. Bit 7 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
08h	7:0	0	MCLK_COUNT	R/W	This register allows the user to determine the frequency of the internal/external oscillator. Internally, a clock counter increments every 131 pulses of the sampling clock (614.4 kHz in full power mode, 153.6 kHz in mid power mode, and 768 kHz in low power mode). The 8-bit counter wraps around on reaching its maximum value. The counter output is read back via this register. Note that the incrementation of the register is asynchronous to the register read. If a register read coincides with the register incrementation, it is possible to read an invalid value. To prevent this, read the register four times rather than once, then read the register four times again at a later point. By reading four values, it is possible to identify the correct register value at the start and at the end of the timing instants.

10.1.2.11 *CHANNEL Registers (Addr = 09h~18h) [reset = 0x8001 for CHANNEL_0; all other channel registers are set to 0x0001]*

Sixteen channel registers are included on the AD7124 , CHANNEL_0 to CHANNEL_15. The channel registers begin at Address 0x09 (CHANNEL_0) and end at Address 0x18 (CHANNEL_15). Via each register, the user can configure the channel (AINP input and AINM input), enable or disable the channel, and select the setup. The setup is selectable from eight different options defined by the user. When the ADC converts, it automatically sequences through all enabled channels. This allows the user to sample some channels multiple times in a sequence, if required. In addition, it allows the user to include diagnostic functions in a sequence also.
Below Table outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
09h ~ 18h	15	0	ENABLE	R/W	Channel enable bit. Setting this bit enables the device channel for the conversion sequence. By default, only the enable bit for Channel 0 is set. The order of conversions starts with the lowest enabled channel, then cycles through successively higher

					channel numbers, before wrapping around to the lowest channel again. When the ADC writes a result for a particular channel, the four LSBs of the status register are set to the channel number, 0 to 15. This allows the channel the data corresponds to be identified. When the DATA_STATUS bit in the ADC_CONTROL register is set, the contents of the status register are appended to each conversion when it is read. Use this function when several channels are enabled to determine to which channel the conversion value read corresponds.
	14:12	0	SETUP	R/W	Setup select. These bits identify which of the eight setups are used to configure the ADC for this channel. A setup comprises a set of four registers: analog configuration, output data rate/filter selection, offset register, and gain register. All channels can use the same setup, in which case the same 3-bit value must be written to these bits on all active channels. Alternatively, up to eight channels can be configured differently.
	11:10	0	RESERVED	R/W	These bits must be programmed with a Logic 0 for correct operation.
	9:5	00000	AINP[4:0]	R/W	Positive analog input AINP input select. These bits select which of the analog inputs is connected to the positive input for this channel. 00000 = AIN0 (default). 00001 = AIN1. 00010 = AIN2. 00011 = AIN3. 00100 = AIN4. 00101 = AIN5. 00110 = AIN6. 00111 = AIN7. 01000 = AIN8. 01001 = AIN9. 01010 = AIN10. 01011 = AIN11. 01100 = AIN12. 01101 = AIN13. 01110 = AIN14. 01111 = AIN15. 10000 = temperature sensor. 10001 = AVSS. 10010 = internal reference. 10011 = DGND. 10100 = (AVDD − AVSS)/6+. Use in conjunction with (AVDD − AVSS)/6− to monitor supply AVDD − AVSS. 10101 = (AVDD − AVSS)/6−. Use in conjunction with (AVDD − AVSS)/6+ to monitor supply AVDD − AVSS. 10110 = (IOVDD − DGND)/6+. Use in conjunction with (IOVDD − DGND)/6− to monitor IOVDD − DGND. 10111 = (IOVDD − DGND)/6−. Use in conjunction with (IOVDD − DGND)/6+ to monitor IOVDD − DGND. 11000 = Reserved. 11001 = Reserved. 11010 = Reserved. 11011 = Reserved. 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20 mV p-p signal to the ADC. 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20 mV p-p signal to the ADC. 11110 = Reserved. 11111 = Reserved.
	4:0	00001	AINM[4:0]	R/W	Negative analog input AINM input select. These bits select which of the analog inputs is connected to the negative input for this channel. 00000 = AIN0.

					00001 = AIN1 (default). 00010 = AIN2. 00011 = AIN3. 00100 = AIN4. 00101 = AIN5. 00110 = AIN6. 00111 = AIN7. 01000 = AIN8. 01001 = AIN9. 01010 = AIN10. 01011 = AIN11. 01100 = AIN12. 01101 = AIN13. 01110 = AIN14. 01111 = AIN15. 10000 = temperature sensor. 10001 = AVSS. 10010 = internal reference. 10011 = DGND. 10100 = (AVDD − AVSS)/6+. Use in conjunction with (AVDD − AVSS)/6− to monitor supply AVDD − AVSS. 10101 = (AVDD − AVSS)/6−. Use in conjunction with (AVDD − AVSS)/6+ to monitor supply AVDD − AVSS. 10110 = (IOVDD − DGND)/6+. Use in conjunction with (IOVDD − DGND)/6− to monitor IOVDD − DGND. 10111 = (IOVDD − DGND)/6−. Use in conjunction with (IOVDD − DGND)/6+ to monitor IOVDD − DGND. 11000 = Reserved. 11001 = Reserved. 11010 = Reserved. 11011 = Reserved. 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20 mV p-p signal to the ADC. 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20 mV p-p signal to the ADC. 11110 = Reserved. 11111 = Reserved.

10.1.2.12 *CONFIGURATION Registers (Addr = 19h~20h) [reset = 0x0860]*

The AD7124 has eight configuration registers, CONFIG_0 to CONFIG_7. Each configuration register is associated with a setup; CONFIG_x is associated with Setup x. In the configuration register, the reference source, polarity, reference buffers are configured. Below Table outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/ reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
19h ~ 20h	15:12	0000	RESERVED	R/W	These bits must be programmed with a Logic 0 for correct operation.
	11	0	Bipolar	R/W	Polarity select bit. When this bit is set, bipolar operation is selected. When this bit is cleared, unipolar operation is selected.
	10:9	00	Burnout	R/W	These bits select the magnitude of the sensor burnout detect current source. 00 = burnout current source off (default). 01 = burnout current source on, 0.5 µA. 10 = burnout current source on, 2 µA. 11 = burnout current source on, 4 µA.
	8	0	REF_BUFP	R/W	Buffer enable on REFINx(+). When this bit is set, the positive reference input (internal or external) is buffered. When this bit is cleared, the positive reference input (internal or external) is unbuffered.
	7	0	REF_BUFM	R/W	Buffer enable on REFINx(−). When this bit is set, the negative reference input (internal or external) is buffered. When this bit is

					cleared, the negative reference input (internal or external) is unbuffered.
	6:5	00	PGA _CONTROL	R/W	PGA enable bits. 00 = PGA bypass. 01 = PGA bypass. 10 = PGA bypass. 11 = PGA enable. Note: In PGA bypass mode, PGA will automatically enabled when the gain exceeds 1.
	4:3	010	REF_SEL	R/W	Reference source select bits. These bits select the reference source to use when converting on any channels using this configuration register. 00 = REFIN1(+)/REFIN1(−). 01 = REFIN2(+)/REFIN2(−). 10 = internal reference. 11 = AVDD.
	2:0	000	PGA	R/W	Gain select bits. These bits select the gain to use when converting on any channels using this configuration register. 000: Gain = 1 001: Gain = 2 010: Gain = 4 011: Gain = 8 100: Gain = 16 101: Gain = 32 110: Gain = 64 111: Gain = 128

10.1.2.13 *FILTER Registers (Addr = 21h~28h) [reset = 0x060180]*

The AD7124 has eight filter registers, FILTER_0 to FILTER_7. Each filter register is associated with a setup; FILTER_x is associated with Setup x. In the filter register, the filter type and output word rate are set.
Below Table outlines the bit designations for the register. Bit 15 is the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

Addr	Bit	Default	Field	Type	Description
21h ~ 28h	23:21	0000	Filter	R/W	Filter type select bits. These bits select the filter type. 000 = sinc4 filter (default). 001 = reserved. 010 = sinc3 filter. 011 = reserved. 100 = fast settling filter using the sinc4 filter. The sinc4 filter is followed by an averaging block, which results in a settling time equal to the conversion time. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode. 101 = fast settling filter using the sinc3 filter. The sinc3 filter is followed by an averaging block, which results in a settling time equal to the conversion time. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode. 110 = reserved. 111 = post filter enabled. The AD7124 includes several post filters, selectable using the POST_FILTER bits. The post filters have single cycle settling, the settling time being considerably better than a simple sinc3/sinc4 filter. These filters offer excellent 50 Hz and 60 Hz rejection.
	20	0	REJ60	R/W	When this bit is set, a first order notch is placed at 60 Hz when the first notch of the sinc filter is at 50 Hz. This allows simultaneous 50 Hz and 60 Hz rejection. Note this bit is only worked when data rate is 50SPS or 25SPS.
	19:17	000	POST_FILTER	R/W	Post filter type select bits. When the filter bits are set to 1, the sinc3 filter is followed by a post filter that offers good 50 Hz and 60

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td>Hz rejection at output data rates that have zero latency approximately.
<table>
<tr><th>POST_FILTER</th><th>Output Data Rate (SPS)</th><th>Rejection at 50 Hz and 60 Hz ± 1 Hz (dB)</th></tr>
<tr><td>000</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>010</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>010</td><td>27.27</td><td>48</td></tr>
<tr><td>011</td><td>25</td><td>63</td></tr>
<tr><td>100</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>101</td><td>20</td><td>88</td></tr>
<tr><td>110</td><td>16.7</td><td>93</td></tr>
<tr><td>111</td><td>Reserved</td><td>Not applicable</td></tr>
</table></td></tr>
<tr><td></td><td>16</td><td>0</td><td>SINGLE_CYCLE</td><td>R/W</td><td>Single cycle conversion enable bit. When this bit is set, the AD7124 settles in one conversion cycle so that it functions as a zero latency ADC. This bit has no effect when multiple analog input channels are enabled or when the single conversion mode is selected. When the fast filters are used, this bit has no effect.</td></tr>
<tr><td></td><td>15:11</td><td>0</td><td>RESERVED</td><td>R/W</td><td>These bits must be programmed with a Logic 0 for correct operation.</td></tr>
<tr><td></td><td>10:0</td><td>0</td><td>FS[10:0]</td><td>R/W</td><td>Filter output data rate select bits. These bits set the output data rate of the sinc3 filter, sinc4 filter, and fast settling filters. In addition, they affect the position of the first notch of the sinc filter and the cutoff frequency. In association with the gain selection, they also determine the output noise and, therefore, the effective resolution of the device (see noise tables). FS can have a value from 1 to 2047.</td></tr>
</table>

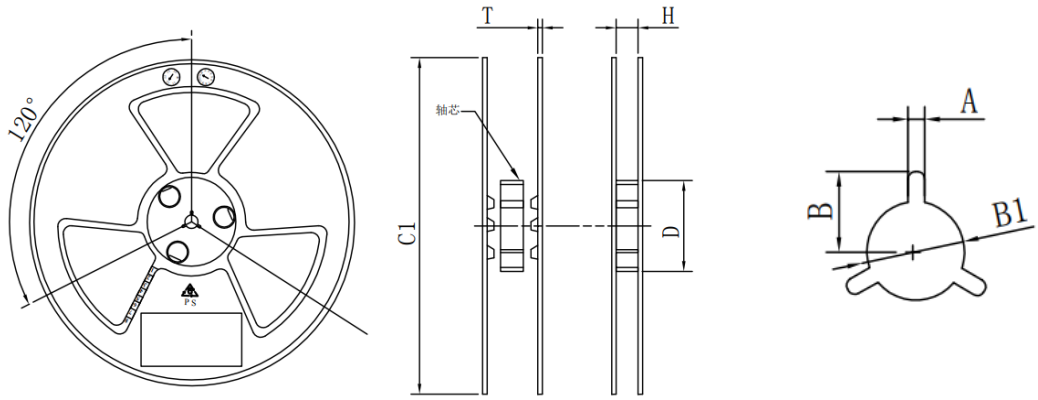
10.1.2.14 *OFFSET Registers (Addr = 29h~30h) [reset = 0x800000]*

The AD124 has eight offset registers, OFFSET_0 to OFFSET_7. Each offset register is associated with a setup; OFFSET_x is associated with Setup x. The offset registers are 24-bit registers and hold the offset calibration coefficient for the ADC and its power-on reset value is 0x800000. Each of these registers is a read/write register. These registers are used in conjunction with the associated gain register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The ADC must be placed in standby mode or idle mode when writing to the offset registers.

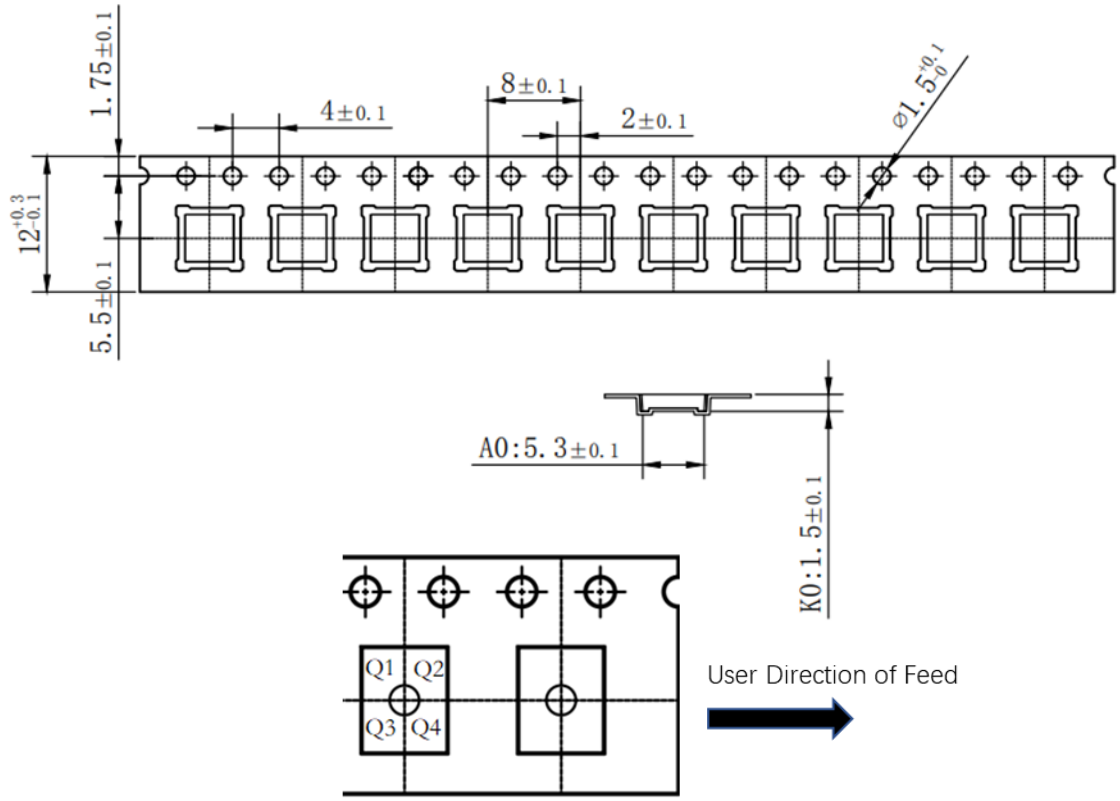
10.1.2.15 *GAIN Registers (Addr = 31h~38h) [reset = 0x500000]*

The AD7124 has eight gain registers, GAIN_0 to GAIN_7, they are designed for system full-scall calibration only(The AD7124 is factory calibrated for all gains, the factory gain calibrated coefficients are not open to user.). Each gain register is associated with a setup; GAIN_x is associated with Setup x. The gain registers are 24-bit registers and hold the full-scale calibration coefficient for the ADC. The gain registers are read/write registers. However, when writing to the registers, the ADC must be placed in standby mode or idle mode. The default value is automatically overwritten if an system full-scale calibration is initiated by the user or the full-scale registers are written to.

10.2 Tape and Reel Information



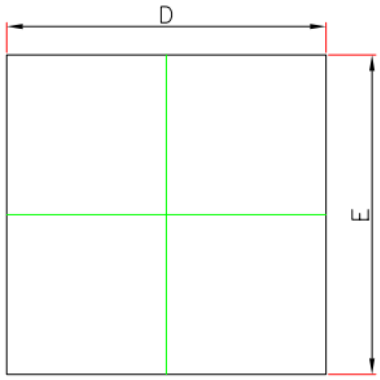
C1	330±3	178±3
H	12.5±0.5	12.8±0.5
A	2.3±0.3	2.6±0.3
B	10.75±0.3	22.5±0.3
B1	∅13.0 +0.5/–0.2	∅13.5±0.3
T	2±0.2	1.2±0.2
D	∅100±1	∅60±0.5
SPQ	2000	300



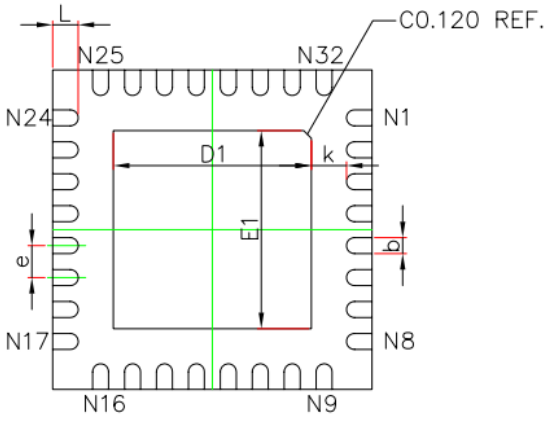
Note: Q1~Q4 is Pocket Quadrants

10.3 Package Information

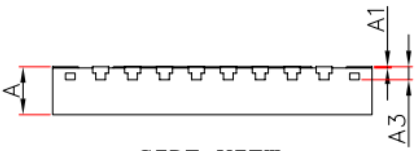
QFNWB5×5-32L-K(P0.50T0.75) PACKAGE OUTLINE DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D1	3.000	3.200	0.118	0.126
E1	3.000	3.200	0.118	0.126
k	0.550REF.		0.022REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.300	0.500	0.012	0.020