

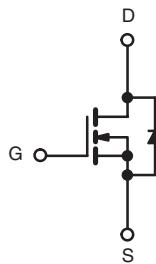
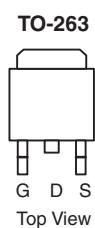
NP82N10PUF-VB Datasheet

N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
100	0.010 at $V_{GS} = 10$ V	100
	0.023 at $V_{GS} = 4.5$ V	85

FEATURES

- Trench Power MOSFET
- 175 °C Maximum Junction Temperature
- Compliant to RoHS Directive 2002/95/EC



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	100	A
		75 ^a	
Pulsed Drain Current	I_{DM}	300	A
Avalanche Current	I_{AS}	75	
Single Pulse Avalanche Energy ^b	E_{AS}	280	mJ
Maximum Power Dissipation ^b	P_D	250 ^c	W
		3.75	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
		62.5	
Junction-to-Case	R_{thJC}	0.6	

Notes:

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

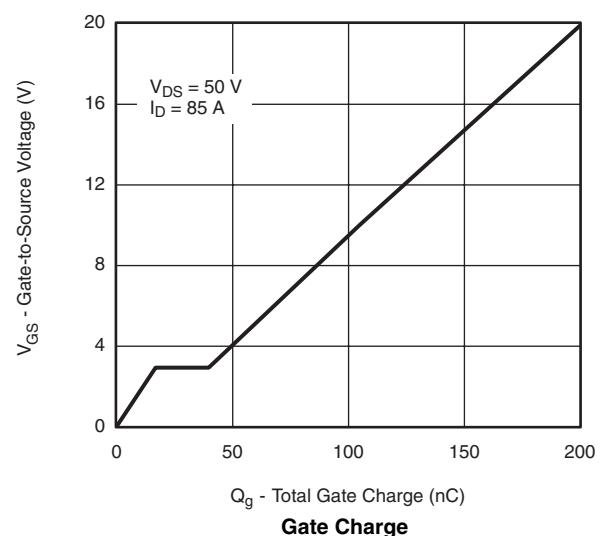
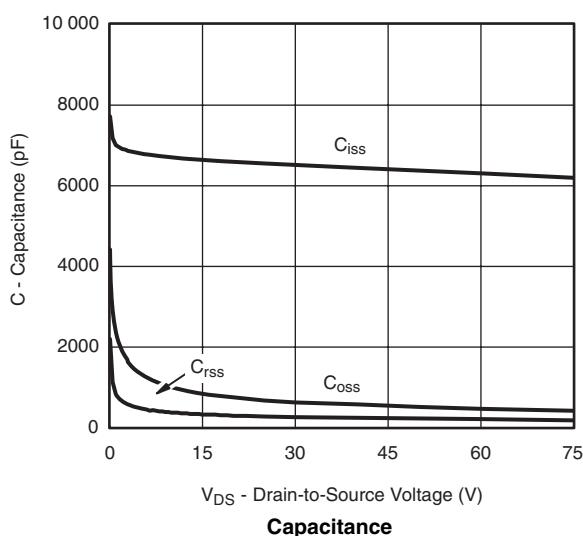
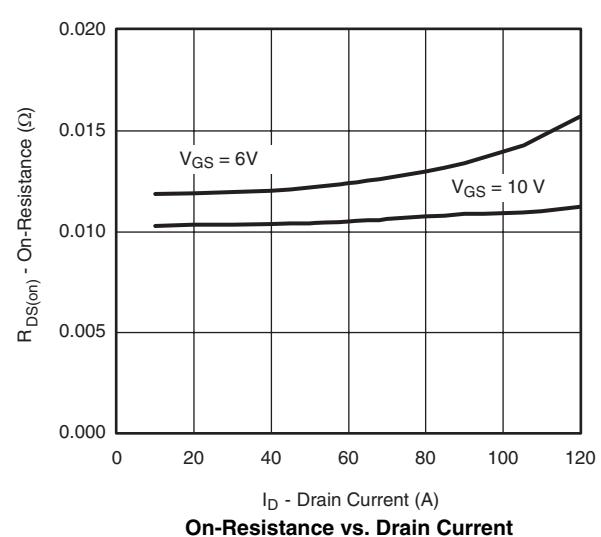
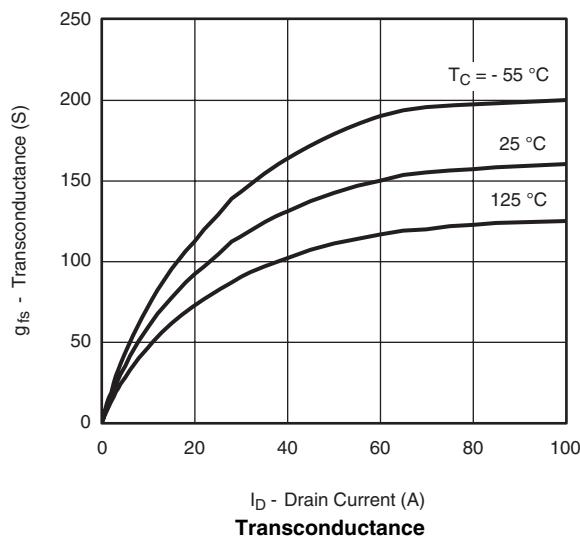
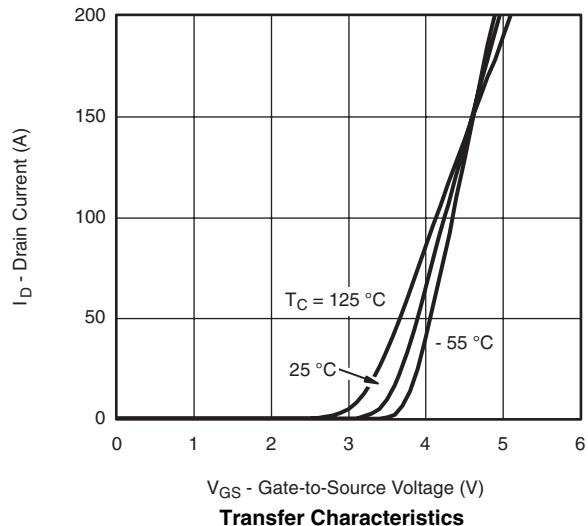
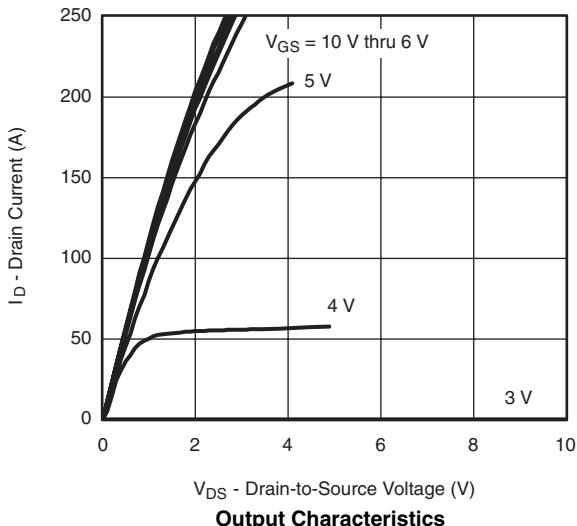
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

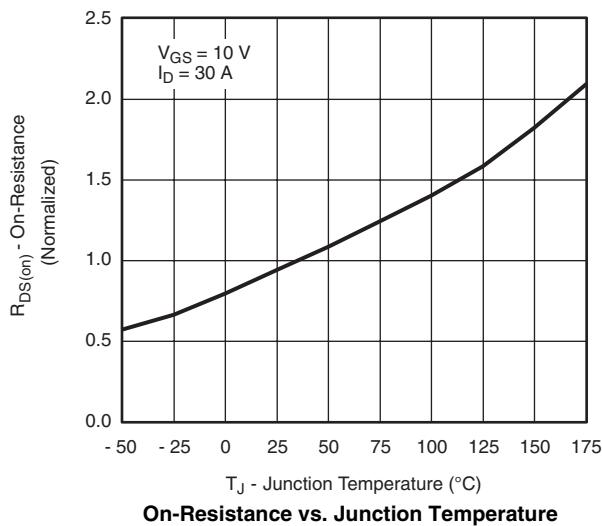
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2		4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$			50	
		$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 175^\circ\text{C}$			250	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} = \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	120			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$		0.010		Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 20 \text{ A}$		0.023		
		$V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$, $T_J = 125^\circ\text{C}$		0.020		
		$V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$, $T_J = 175^\circ\text{C}$		0.030		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 30 \text{ A}$	25			S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$		6550		pF
Output Capacitance	C_{oss}			665		
Reverse Transfer Capacitance	C_{rss}			265		
Total Gate Charge ^c	Q_g	$V_{DS} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 85 \text{ A}$		105	160	nC
Gate-Source Charge ^c	Q_{gs}			17		
Gate-Drain Charge ^c	Q_{gd}			23		
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$, $R_L = 0.6 \Omega$ $I_D \geq 85 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 2.5 \Omega$		12	25	ns
Rise Time ^c	t_r			90	135	
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			55	85	
Fall Time ^c	t_f			130	195	
Source-Drain Diode Ratings and Characteristics $T_C = 25^\circ\text{C}^b$						
Continuous Current	I_S				85	A
Pulsed Current	I_{SM}				240	
Forward Voltage ^a	V_{SD}	$I_F = 85 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 50 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$		85	140	ns
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			4.5	7	A
Reverse Recovery Charge	Q_{rr}			0.17	0.35	μC

Notes:

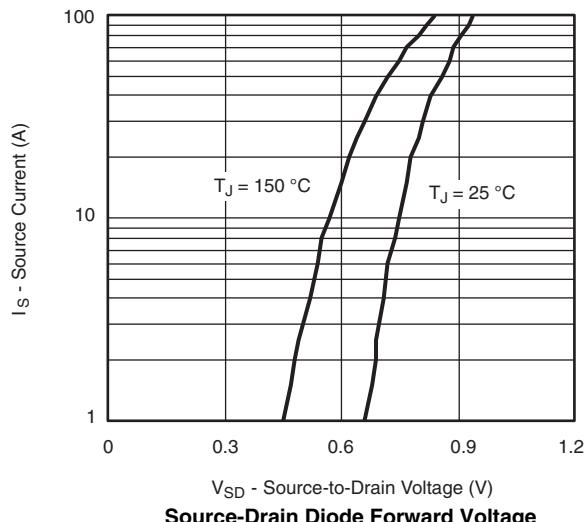
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

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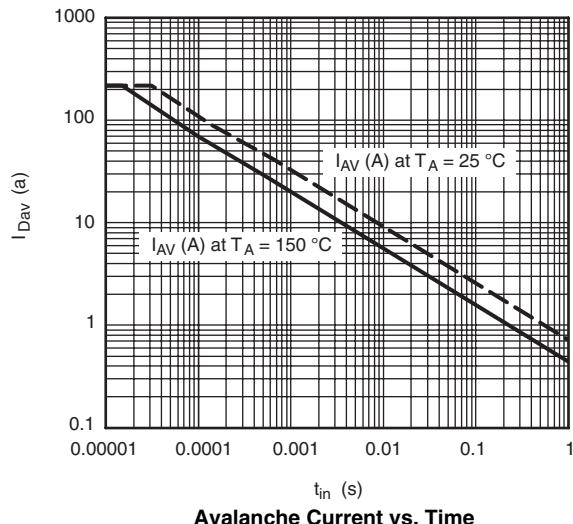
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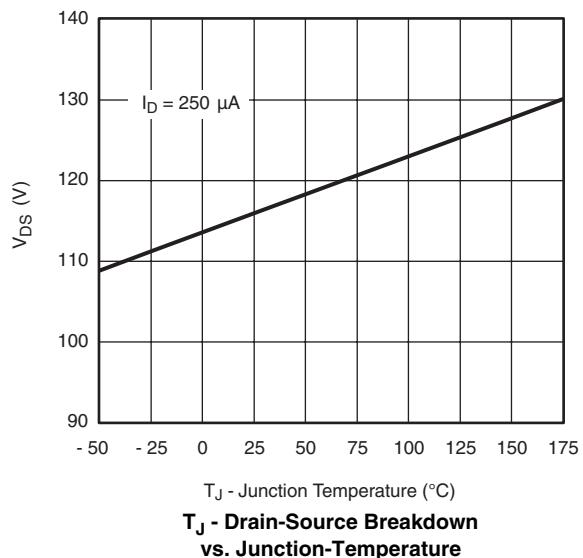
On-Resistance vs. Junction Temperature



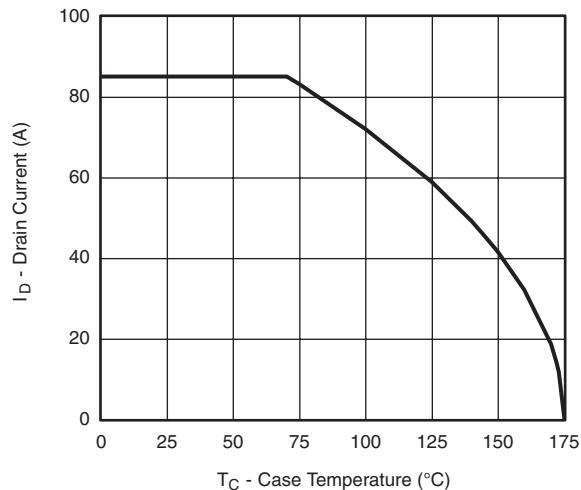
Source-Drain Diode Forward Voltage



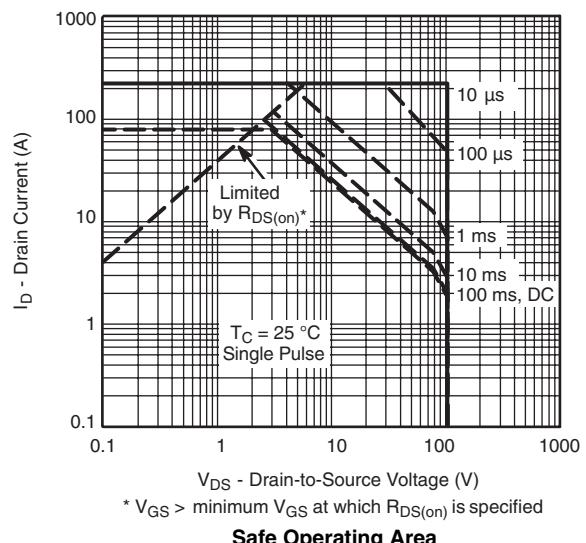
Avalanche Current vs. Time

 T_J - Drain-Source Breakdown vs. Junction-Temperature

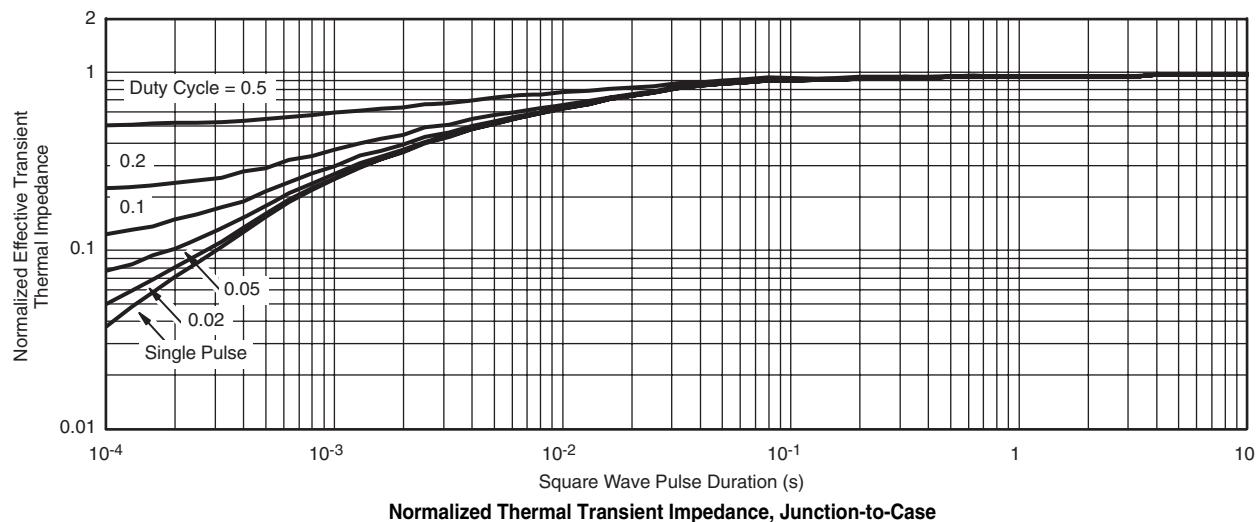
THERMAL RATINGS



**Maximum Avalanche and Drain Current
vs. Case Temperature**

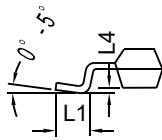
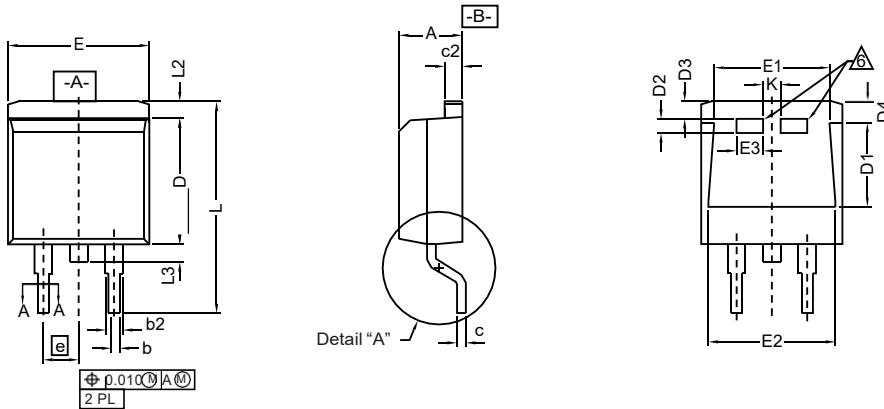


Safe Operating Area

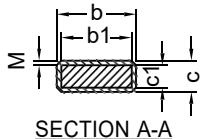


Normalized Thermal Transient Impedance, Junction-to-Case

TO-263 (D²PAK): 3-LEAD



DETAIL A (ROTATED 90°)



SECTION A-A

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6.  This feature is for thick lead.

DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

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