Power Management IC for X5 SoC

Features

- 2.7-V to 5.5-V input voltage range
- 0.6V to 3.6V output voltage range with DVS
- Five synchronous buck converters
  - Buck 1, buck 2, buck 3 and buck 4 up to 4 A
  - Buck 5 up to 3 A
- Three 300mA LDOs
- ±2% output voltage accuracy
- Programmable output current limit
- Auto PFM and forced PWM operations
- Configurable dual phase operating
- Pre-set start-up and shutdown sequencing
- Programmable enable control for power rails
- I²C interface supporting standard, fast and fast plus speed modes
- Open-drain power on reset output
- Power key input
- Reset input
- Real time clock with alarm
- Over temperature protection
- Operating T_J temperature range from −40°C ~ +125°C
- Available in 6mm×6mm 48-pin QFN package

Applications

- Power supply for AI, video processors
- Smartphone, tablet, AR/VR, drone
- Optical module
- SSD, NAS

Description

The HPU3501 is a highly integrated power management IC for applications that require multi-channel buck converters and LDOs. The device contains five buck converters. The buck 1, the buck 2, the buck 3, and the buck 4 provide programmable output voltage from 0.6 V to 1.275 V. They have up to 4-A output current capability. The buck 5 has up to 3-A output current capability. The buck 1 and the buck 2, or the buck 3 and the buck 4 can be configured to be a dual-phase buck converter. In addition, the device integrates three programmable LDOs and one real time clock.

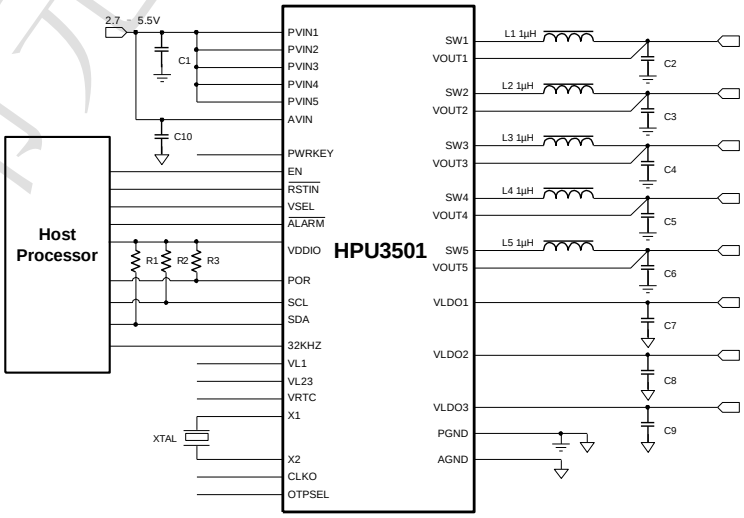
The buck converters of the HPU3501 run at 1.2MHz with small size external components. They also support auto PFM mode to maximize efficiency in light load condition.

The HPU3501 supports programmable start-up slew rate, power-up and power-down sequencing to meet the requirements by processors. The device has a power-on reset output with more than 20ms delay time for processors.

The HPU3501 has output current limit protection, output short-circuit and over-load protection. The over-temperature thermal shutdown protects the device from damage due to high temperature.

The HPU3501 is available in 48-pin 6mmx6mm QFN package with exposed pad for better thermal performance.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2023-04-05	Rev.1.0	Initial release
2024-07-02	Rev.1.1	Updated the Product Family Table
2024-11-14	Rev.1.2	● Added three new part numbers, HPU3501A10CQNXMB, HPU3501A13CQNXMA and HPU3501A13CQNXMB. ● Added the default output voltage and power on/off sequence setting for new added three parts. ● Corrected editorial typos.

Product Family Table

Part Number	Power ON/OFF Key Input	I²C address when OTPSEL=0	I²C address when OTPSEL=1	Power Up/Down Sequence Interval Time	Chip ID
HPU3501A10CQNXMA	Disabled	0x1C	0x3C	1.9ms	00000110
HPU3501A10CQNXMB	Disabled	0x1C	0x3C	1.9ms	00000111
HPU3501A13CQNXMA	Disabled	0x1C	0x3C	1.9ms	00001100
HPU3501A13CQNXMB	Disabled	0x1C	0x3C	1.9ms	00001101

Default Output Voltage and Power Up/Down Sequence Setting

HPU3501A10CQNXMA and HPU3501A10CQNXMB

	Master (OTPSEL=0)		
Power Rail	Output Voltage	Power-up Sequence	Power-down Sequence
Buck 1	0.8V	Group 3	Group 3
Buck 2	0.8V	Group 5	Group 1
Buck 3	0.8V	Group 3	Group 3
Buck 4	1.1V	Group 4	Group 2
Buck 5	1.8V	Group 3	Group 3
LDO 1	0.8V	Group 5	Group 1
LDO 2 (VSEL=0)	3.3V	Group 4	Group 2
LDO 2 (VSEL=1)	1.8V	Group 4	Group 2
LDO3	1.8V	Group 5	Group 1

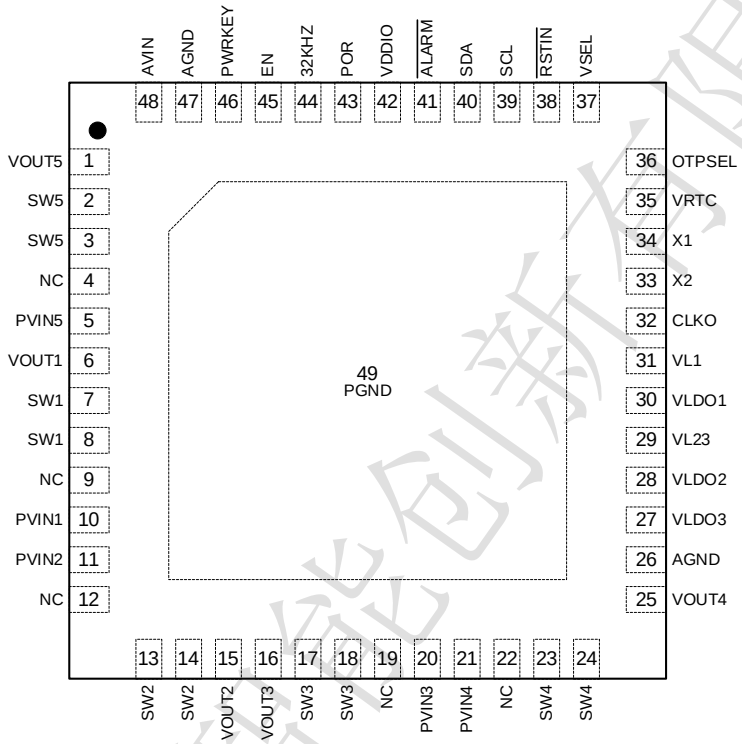
HPU3501A13CQNXMA and HPU3501A13CQNXMB

	Master (OTPSEL=0)		
Power Rail	Output Voltage	Power-up Sequence	Power-down Sequence
Buck 1	0.8V	Group 3	Group 3
Buck 2	0.8V	Group 5	Group 1
Buck 3	0.8V	Group 3	Group 3
Buck 4	1.1V	Group 4	Group 2
Buck 5	1.8V	Group 3	Group 3
LDO 1	0.8V	Group 5	Group 1
LDO 2 (VSEL=0)	1.8V	Group 5	Group 1
LDO 2 (VSEL=1)	3.3V	Group 5	Group 1
LDO3	3.3V	Group 4	Group 2

Pin Configuration and Functions

6x6 QFN Package

Top View



Pin Functions

Pin		I/O/P	Description
No.	Name		
1	VOUT5	I	Output voltage feedback for the buck converter 5
2, 3	SW5	P	The switch node of the buck converter 5. SW5 is internally connected to the drain of the low side power NMOS FET and the source of the high side PMOS FET. Connect SW5 to the inductor.
4, 9, 12, 19, 22	NC	-	No internal connection. These five NC pins could be connected to the adjacent PVINx pins or the PGND pin at the bottom of the package.
5	PVIN5	P	The input power supply for the buck converter 5. A decoupling ceramic cap must be connected close to the PVIN5 pin and PGND pins.
6	VOUT1	I	Output voltage feedback for the buck converter 1
7, 8	SW1	P	The switch node of the buck converter 1. SW1 is internally connected to the drain of the low side power NMOS FET and the source of the high side PMOS FET. Connect SW1 to the inductor.
10	PVIN1	P	The input power supply for the buck converter 1. A decoupling ceramic cap must be connected close to the PVIN1 pin and PGND pins.

11	PVIN2	P	The input power supply for the buck converter 2. A decoupling ceramic cap must be connected close to the PVIN2 pin and PGND pins.
13, 14	SW2	P	The switch node of the buck converter 2. SW2 is internally connected to the drain of the low side power NMOS FET and the source of the high side PMOS FET. Connect SW2 to the inductor.
15	VOUT2	I	Output voltage feedback for the buck converter 2
16	VOUT3	I	Output voltage feedback for the buck converter 3
17, 18	SW3	IP	The switch node of the buck converter 3. SW3 is internally connected to the drain of the low side power NMOS FET and the source of the high side PMOS FET. Connect SW3 to the inductor.
20	PVIN3	P	The input power supply for the buck converter 3. A decoupling ceramic cap must be connected close to the PVIN3 pin and PGND pins.
21	PVIN4	P	The input power supply for the buck converter 4. A decoupling ceramic cap must be connected close to the PVIN4 pin and PGND pins.
23, 24	SW4	P	The switch node of the buck converter 4. SW4 is internally connected to the drain of the low side power NMOS FET and the source of the high side PMOS FET. Connect SW4 to the inductor.
25	VOUT4	I	Output voltage feedback for the buck converter 4
26, 47	AGND	GND	Ground of the control circuit and LDO.
27	VLDO3	O	Output of the LDO 3
28	VLDO2	O	Output of the LDO 2
29	VL23	I	Input power for the LDO 2 and LDO 3
30	VLDO1	O	Output of the LDO 1
31	VL1	I	Input power for the LDO 1
32	CLKO	I/O	32.768kHz clock output when set as the master PMIC (OTPSEL=0). 32.768kHz clock input when set as the slave PMIC (OTPSEL=1).
33	X2	O	Real time clock pin. Connect to an external 32.768kHz crystal.
34	X1	I	Real time clock pin. Connect to an external 32.768kHz crystal.
35	VRTC	P	Backup power supply for the real time clock (RTC)
36	OTPSEL	I	Select one of the two default internal OTP setting banks. When OTPSEL is connected to ground, the device is set as the master PMIC. When OTPSEL is connected to VRTC, the device is set as the slave PMIC.
37	VSEL	I	LDO 2 output selection pin. Logic low input selects the output voltage set in the LDO2_VOUT_CFG1R register. Logic high input selects the output voltage set in the LDO2_ CFG2R register.
38	RSTIN_N	I	Power-down acknowledgement input. Pulling down the RSTIN_N to power down the PMIC when PWRKEY is at logic low level. The RSTIN_N is only valid for the devices with power ON/OFF key input function. The HPU3501A10CQNXMA, HPU3501A10CQNXMB, HPU3501A13CQNXMA and HPU3501A13CQNXMB don't have this function.
39	SCL	I	I^2C clock input pin

40	SDA	I/O	I^2C data line
41	ALARM_N	O	Push-pull output of the RTC alarm, active low
42	VDDIO	P	Power supply for digital IO
43	POR	O	Power on reset output
44	32KHz	O	32.768kHz clock output for SoC
45	EN	I	Enable input for the selected power rail group
46	PWRKEY	I	Power-on input. When AVIN and PVINx are ready, pulling down PWRKEY to low level for more than 10ms enables the device. After the device completes power-up, pulling down PWRKEY to low level for more than 10ms shuts down the device. The HPU3501A10CQNXMA, HPU3501A10CQNXMB, HPU3501A13CQNXMA and HPU3501A13CQNXMB don't have this function.
48	AVIN	P	Power supply for analog and digital control circuit
49	PGND	GND	Power ground for buck converters. It must connect to ground plane.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Voltage range at terminals	PVIN1, PVIN2, PVIN3, PVIN4, PVIN5, SW1, SW2, SW3, SW4, SW5, VOUT1, VOUT2, VOUT3, VOUT4, VOUT5, VL1, VL23, VLDO1, VLDO2, VLDO3, EN, 32KHZ, VSEL, AVIN, SCL, SDA, POR, PWRKEY, ALARM_N, RSTIN_N, VRTC, VDDIO, OTPSEL, X1, X2, CLKO	–0.3	5.5	V
T_J	Maximum Junction Temperature	–40	125	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
V_{HBM}	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001(1)	2000	V
V_{CDM}	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002(2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
PVINx	Power supply for buck converters	2.7		5.5	V
VOUTx	Feedback for buck converters	0		3.8	V
C_{OUT}	Effective capacitance for each buck converter output	20	100	1000	µF
L	Inductor for each buck converter	0.47	1.0	2.0	µH
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC(TOP)}$	Unit
QFN6X6-48	24.2	4.8	20.5	°C/W

Electrical Characteristics

V_{AVIN} = 5 V, V_{PVINx} = 5 V, T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{AVIN}	IC supply voltage range		2.7		5.5	V
I_Q	Operating quiescent current	No switching.		1.7	2.5	mA
V_{UVLO}	Under voltage lockout	V_{IN} rising	2.85	3.0	3.15	V
V_{UVLO_HYS}	UVLO hysteresis		220	290	350	mV
V_{DDIO}	Digital input and output supply voltage range		1.5		5.5	V
Buck Converter 1 & 2						
$V_{PVIN1/2}$	Supply voltage for buck converters		2.7		5.5	V
$V_{OUT1/2}$	Programmable output voltage range		0.6		1.275	V
$V_{OUT1/2\_STEP}$	Output voltage step	0.6V ≤ $V_{OUT1/2}$ < 1.275V		5		mV
$V_{OUT1/2\_ACC}$	Output voltage accuracy	PWM mode	-2%		+2%	$V_{OUT1/2}$
		PFM mode	-2%		+3%	$V_{OUT1/2}$
I_{LIM1}	Programmable output current limit of buck converter 1	BUCK1_OCP_SET=00		4		A
		BUCK1_OCP_SET=01		5		A
		BUCK1_OCP_SET=10		6		A
		BUCK1_OCP_SET=11		7		A
I_{LIM2}	Programmable output current limit of buck converter 2	BUCK2_OCP_SET=00		4		A
		BUCK2_OCP_SET=01		5		A
		BUCK2_OCP_SET=10		6		A
		BUCK2_OCP_SET=11		7		A
$R_{DSON\_HS1/2}$	On resistance of high side PMOS FET			40		mΩ
$R_{DSON\_LS1/2}$	On resistance of Low side NMOS FET			22		mΩ
Buck Converter 3 & 4						
$V_{PVIN3/4}$	Supply voltage for buck converters		2.7		5.5	V
$V_{OUT3/4}$	Programmable Output voltage range		0.6		1.275	V
$V_{OUT3/4\_STEP}$	Output voltage step	0.6V ≤ $V_{OUT3/4}$ < 1.275V		5		mV
$V_{OUT3/4\_ACC}$	Output voltage accuracy	PWM mode	-2%		+2%	$V_{OUT3/4}$
		PFM mode	-2%		+3%	$V_{OUT3/4}$
I_{LIM3}	Programmable output current limit of buck converter 3	BUCK3_OCP_SET=00		4		A
		BUCK3_OCP_SET=01		5		A
		BUCK3_OCP_SET=10		6		A

		BUCK3_OCP_SET=11		7		A
I_{LIM4}	Programmable output current limit of buck converter 4	BUCK4_OCP_SET=00		4		A
		BUCK4_OCP_SET=01		5		A
		BUCK4_OCP_SET=10		6		A
		BUCK4_OCP_SET=11		7		A
$R_{DSON\_HS3/4}$	On resistance of high side PMOS FET			40		mΩ
$R_{DSON\_LS3/4}$	On resistance of Ligh side NMOS FET			22		mΩ
Buck Converter 5						
V_{PVIN5}	Supply voltage for buck converters		2.7		5.5	V
V_{OUT5}	Programmable Output voltage range		0.6		3.825	V
V_{OUT5_STEP}	Output voltage step	$0.6V \le V_{OUT5} \le 3.825$		15		mV
V_{OUT5_ACC}	Output voltage accuracy	PWM mode	-2%		+2%	V_{OUT5}
		PFM mode	-2%		+3%	V_{OUT5}
I_{LIM5}	Programmable output current limit of buck converter 5	BUCK5_OCP_SET=00		3		A
		BUCK5_OCP_SET=01		4		A
		BUCK5_OCP_SET=10		5		A
		BUCK5_OCP_SET=11		6		A
R_{DSON_HS5}	On resistance of high side PMOS FET			50		mΩ
R_{DSON_LS5}	On resistance of Ligh side NMOS FET			31		mΩ
Switching Frequency						
f_{SW}	Switching frequency for all buck converters			1.2		MHz
LDO 1						
V_{L1}	Input power voltage for LDO 1		1.7		5.5	V
V_{LDO1}	Output voltage range		0.6		1.3	V
V_{LDO1_STEP}	Output voltage step	$0.6V \le V_{LDO1} \le 1.3V$		10		mV
V_{LDO1_ACC}	Output voltage accuracy		-2%		+2%	V_{LDO1}
V_{DO1}	Drop out voltage	300mA load current		275		mV
LDO 2 & 3						
$V_{L2/3}$	Input power voltage for LDO 2 and LDO 3		1.7		5.5	V
$V_{LDO2/3}$	Output voltage range		1.2		3.7	V
$V_{LDO2/3\_STEP}$	Output voltage step	$1.2V \le V_{LDO2/3} \le 3.7V$		20		mV
$V_{LDO2/3\_ACC}$	Output voltage accuracy		-2%		+2%	$V_{LDO2/3}$

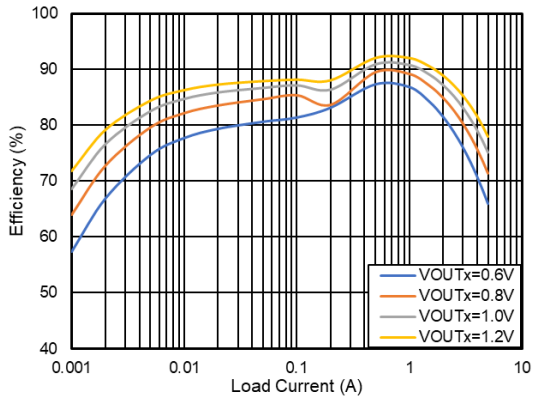
$V_{DO2/3}$	Drop out voltage	300mA load current		210		mV
V_{VSEL_H}	VSEL input high voltage threshold	V_{DDIO} = 3V			1.2	V
V_{VSEL_L}	VSEL input low voltage threshold	V_{DDIO} = 3V	0.4			V
V_{VSEL_HYS}	VSEL threshold hysteresis	V_{DDIO} = 3V		70		mV
R_{VSEL}	Internal pull-down resistance			1050		kΩ
Real Time Clock						
V_{RTC}	Backup power supply for RTC		2.0		3.3	V
I_{RTC}	Supply current for RTC powered by backup power			2.5		μA
I_{CHG}	Charge current to the VRTC pin for backup battery		0.3	0.6	0.9	mA
V_{CHG}	Charge termination voltage		2.9	3.0	3.1	V
V_{ALARM_H}	Alarm output high voltage	2mA sourcing current, V_{DDIO}=3.0V	2.5			V
V_{ALARM_L}	Alarm output low voltage	2mA sinking current, V_{DDIO}=3.0V			0.4	V
f_{RTC_CLK}	Output frequency at CLKO			32.768		kHz
V_{32KHZ_H}	32.768kHz clock output high voltage at the 32KHZ pin	2mA sourcing current, V_{DDIO}=3.0V	2.5			V
V_{32KHZ_L}	32.768kHz clock output low voltage at the 32KHZ pin	2mA sinking current, V_{DDIO}=3.0V			0.4	V
V_{CLKO_OH}	Clock output high voltage at the CLKO pin	0.2mA sourcing current	1.7			V
V_{CLKO_OL}	Clock output low voltage at the CLKO pin	0.2mA sinking current			0.4	V
V_{CLKO_IH}	Clock input high voltage threshold at the CLKO pin				1.6	V
V_{CLKO_IL}	Clock input low voltage threshold at the CLKO pin		0.5			V
Enable Control						
V_{EN_H}	EN logic high threshold (enable)	V_{DDIO} = 3V			1.2	V
V_{EN_L}	EN logic low threshold (disable)	V_{DDIO} = 3V	0.4			V
V_{EN_HYS}	EN threshold hysteresis	V_{DDIO} = 3V		70		mV
I^2C Interface						
V_{LOG_H}	Logic high threshold				1.2	V
V_{LOG_L}	Logic low threshold		0.4			V
Power-on Reset						
V_{POR}	Power-on reset threshold			92.5%		V_{OUT}

V_{POR_L}	Output low voltage	2mA sinking current			0.3	V
I_{POR_LKG}	Leakage current into POR	POR outputs high impedance. Pull up to 3.0V			1	μA
PWRKEY Input						
V_{PWRKEY_H}	PWRKEY input high threshold				1.2	V
V_{PWRKEY_L}	PWRKEY input low threshold		0.4			V
V_{PWRKEY_HYS}	PWRKEY input hysteresis			70		mV
t_{PWRKEY}	PWRKEY delay time		10		100	ms
RSTIN Input						
V_{RSTIN_H}	Reset input high threshold				1.2	V
V_{RSTIN_L}	Reset input low threshold		0.4			V
V_{RSTIN_HYS}	Reset input hysteresis			70		mV
Junction Temperature Protection						
T_{SD}	Thermal shutdown protection threshold	T_J rising		150		ºC
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		ºC

***Note:** (1). 100% tested at T_A = 25°C.

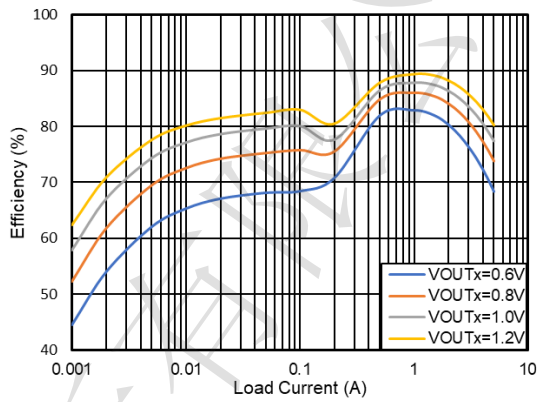
Typical Performance Characteristics

All test conditions: V_{AVIN} = V_{PVINX} = 5 V, T_A = +25°C, unless otherwise noted.



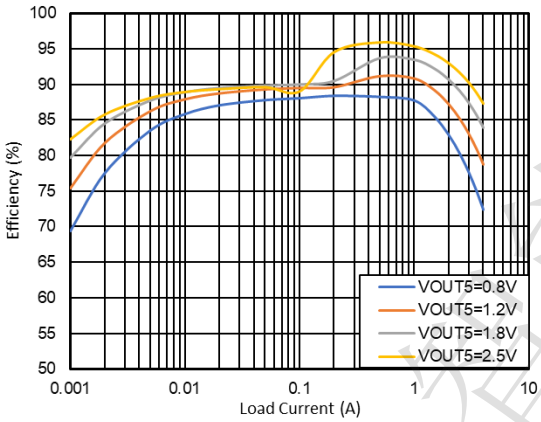
V_{PVINx} = 3.3 V, VOUTx = 0.6V, 0.8V, 1.0V, 1.2 V

Figure 1. Buck 1-4 Efficiency vs. Load Current



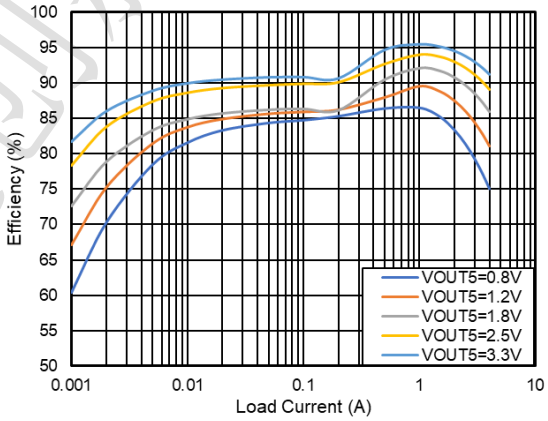
V_{PVINx} = 5 V, VOUTx = 0.6V, 0.8V, 1.0V, 1.2 V

Figure 2. Buck 1-4 Efficiency vs. Load Current



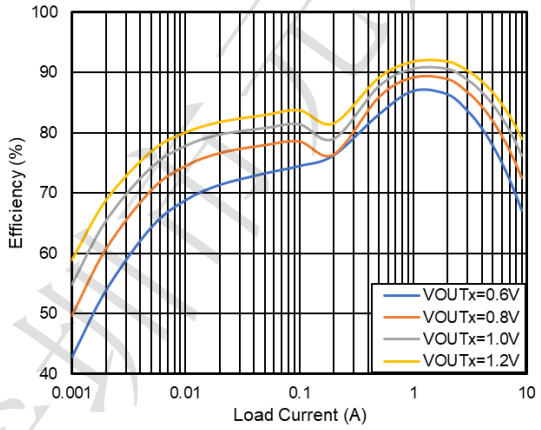
V_{PVIN5} = 3.3 V, VOUT5 = 0.8V, 1.2V, 1.8V, 2.5V

Figure 3. Buck 5 Efficiency vs. Load Current



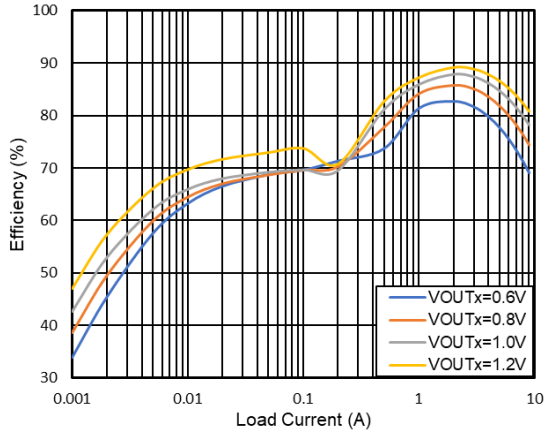
V_{PVIN5} = 5 V, VOUT5 = 0.8V, 1.2V, 1.8V, 2.5V, 3.3V

Figure 4. BUCK 5 Efficiency vs. Load Current



V_{PVINx} = 3.3V, VOUTx = 0.6V, 0.8V, 1.0V, 1.2V

Figure 5. Dual Phase Efficiency vs. Load Current

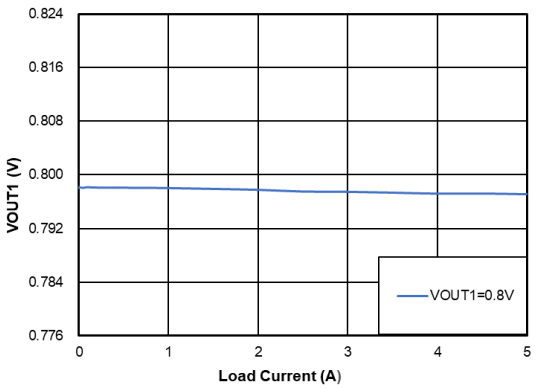


V_{PVINx} = 5 V, VOUTx = 0.6V, 0.8V, 1.0V, 1.2V

Figure 6. Dual Phase Efficiency vs. Load Current

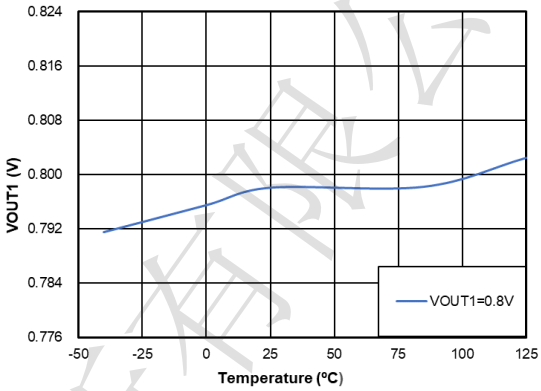
Typical Performance Characteristics (Continued)

All test condition: V_{AVIN} = V_{PVINX} = 5 V, T_A = +25°C, unless otherwise noted.



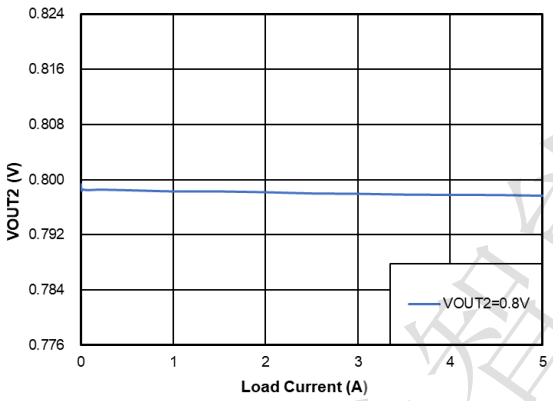
VOUT1 = 0.8V

Figure 7. Buck 1 Output Voltage vs. Load Current



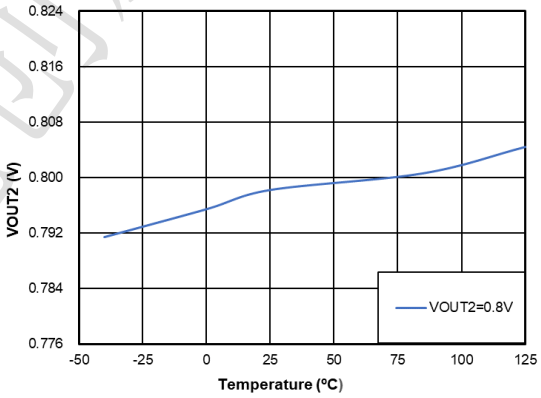
VOUT1 = 0.8V

Figure 8. Buck 1 Output Voltage vs. Temperature



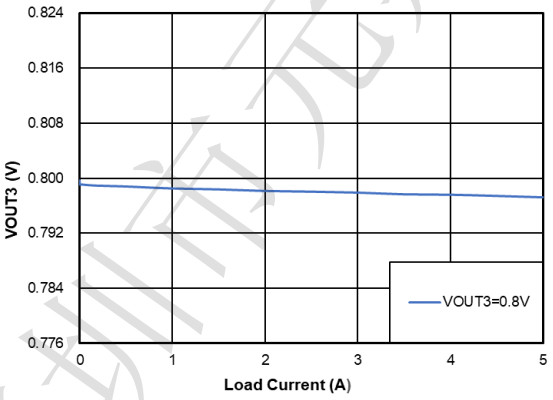
VOUT2 = 0.8V

Figure 9. Buck 2 Output Voltage vs. Load Current



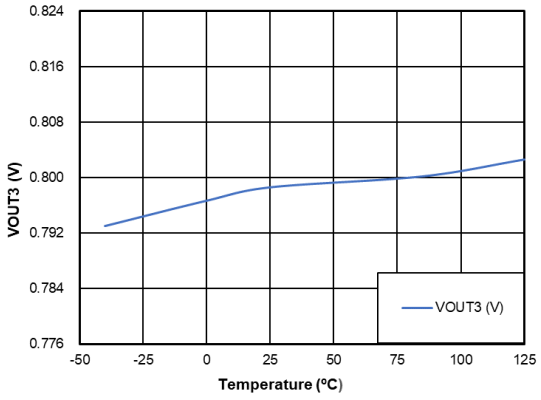
VOUT2 = 0.8V

Figure 10. Buck 2 Output Voltage vs. Temperature



VOUT3 = 0.8V

Figure 11. Buck 3 Output Voltage vs. Load Current

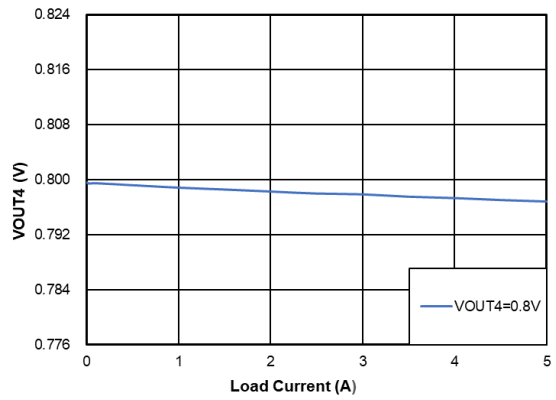


VOUT3 = 0.8V

Figure 12. Buck 3 Output Voltage vs. Temperature

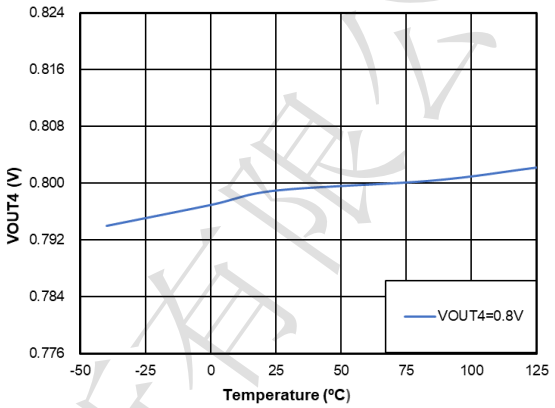
Typical Performance Characteristics (Continued)

All test condition: V_{AVIN} = V_{PVINX} = 5 V, T_A = +25°C, unless otherwise noted.



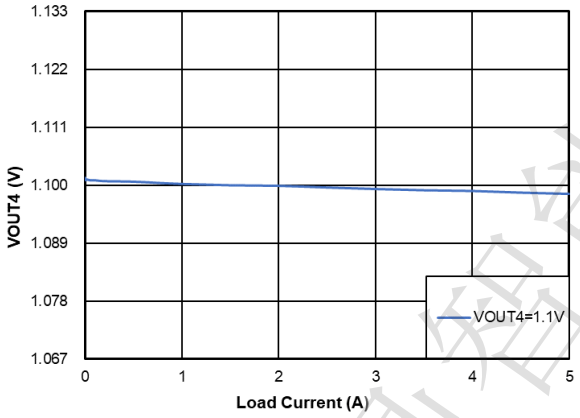
VOUT4 = 0.8V

Figure 13. Buck 4 Output Voltage vs. Load Current



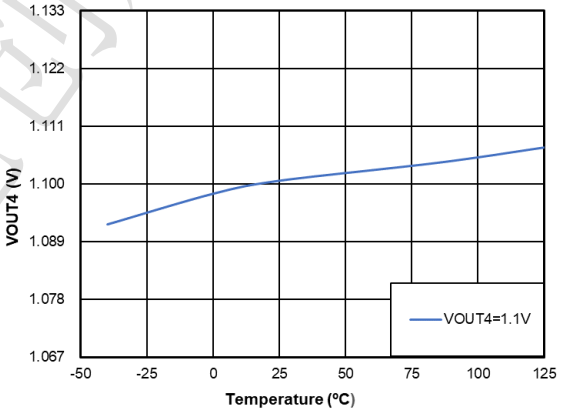
VOUT4 = 0.8V

Figure 14. Buck 4 Output Voltage vs. Temperature



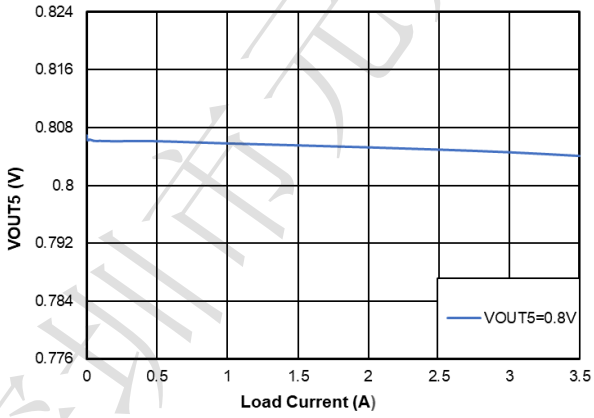
VOUT4 = 1.1V

Figure 15. Buck 4 Output Voltage vs. Load Current



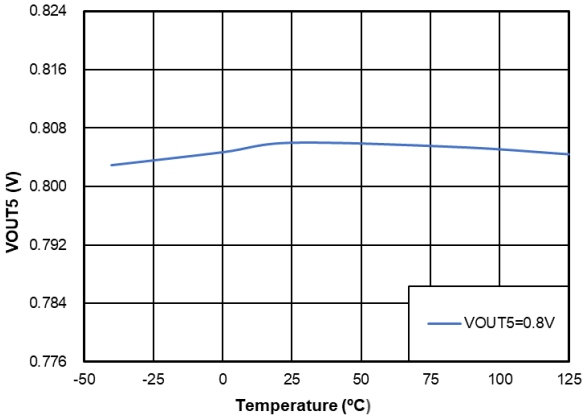
VOUT4 = 1.1V

Figure 16. Buck 4 Output Voltage vs. Temperature



VOUT5 = 0.8V

Figure 17. Buck 5 Output Voltage vs. Load Current

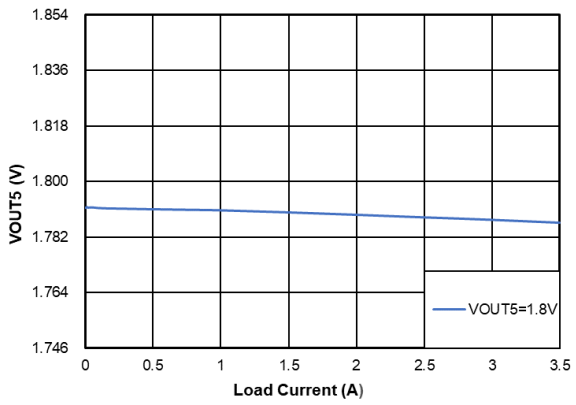


VOUT5 = 0.8V

Figure 18. Buck 5 Output Voltage vs. Temperature

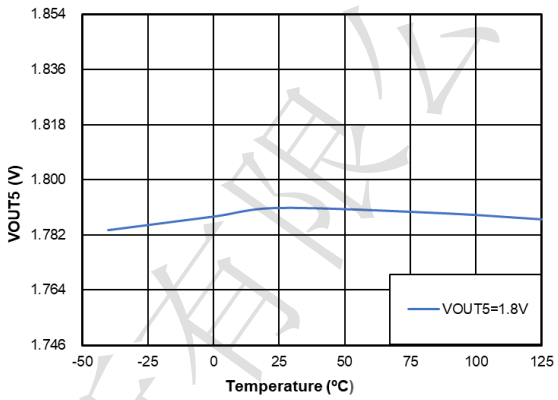
Typical Performance Characteristics (Continued)

All test condition: V_{AVIN} = V_{PVINX} = 5 V, T_A = +25°C, unless otherwise noted.



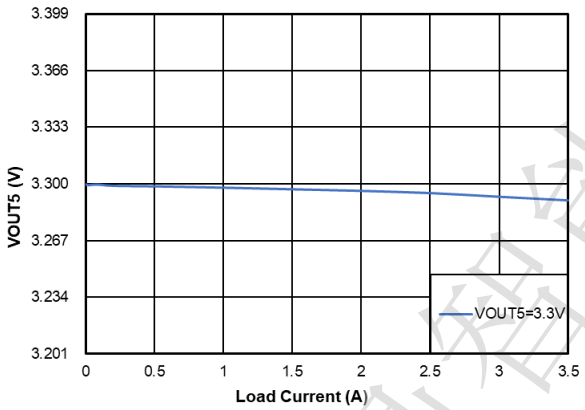
VOUT5 = 1.8V

Figure 19. Buck 5 Output Voltage vs. Load Current



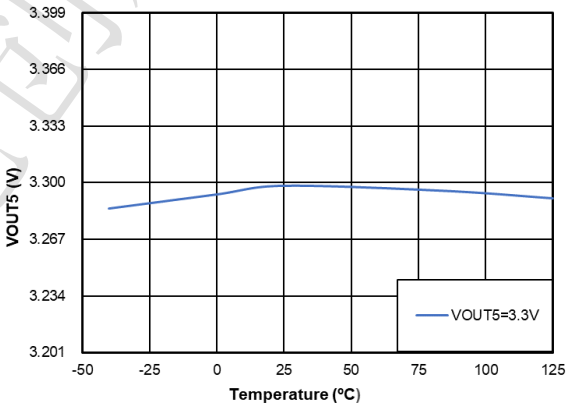
VOUT5 = 1.8V

Figure 20. Buck 5 Output Voltage vs. Temperature



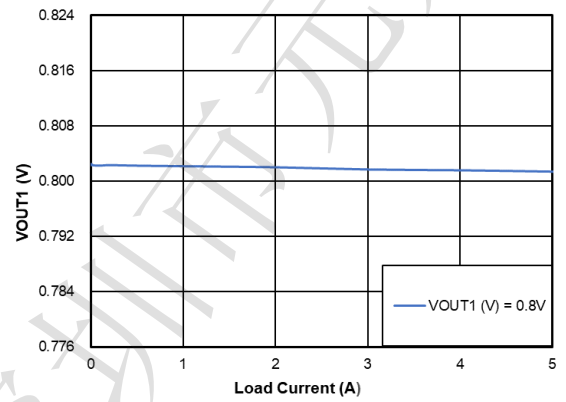
VOUT5 = 3.3V

Figure 21. Buck 5 Output Voltage vs. Load Current



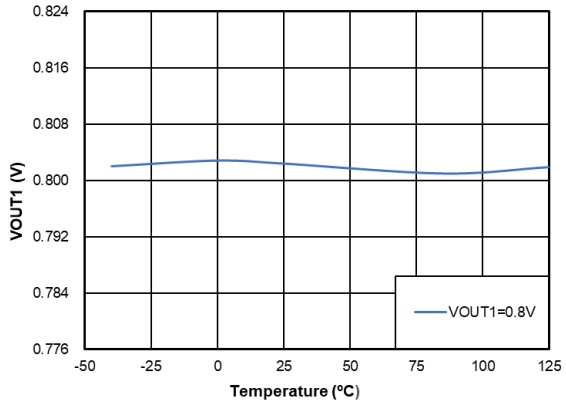
VOUT5 = 3.3V

Figure 22. Buck 5 Output Voltage vs. Temperature



VOUT1 = 0.8V

Figure 23. Dual Phase Output vs. Load Current

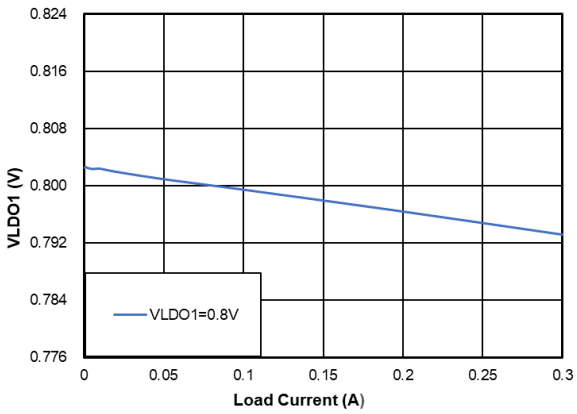


VOUT1 = 0.8V

Figure 24. Dual Phase Output vs. Temperature

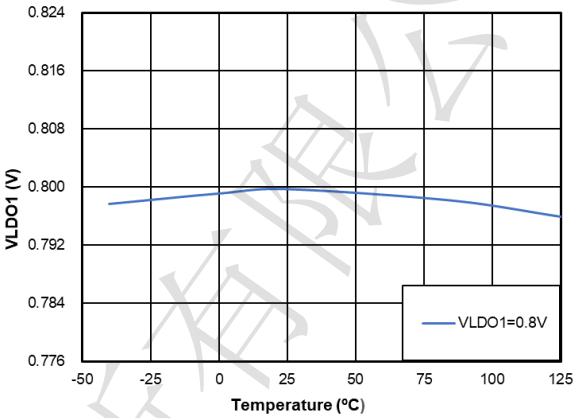
Typical Performance Characteristics (Continued)

All test condition: V_{AVIN} = V_{PVINX} = 5 V, T_A = +25°C, unless otherwise noted.



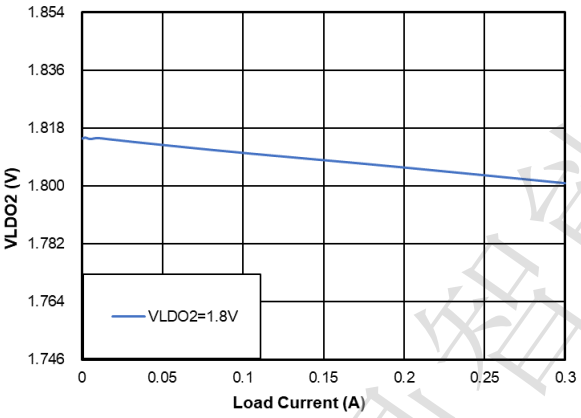
VLDO1 = 0.8V

Figure 25. LDO 1 Output Voltage vs. Load Current



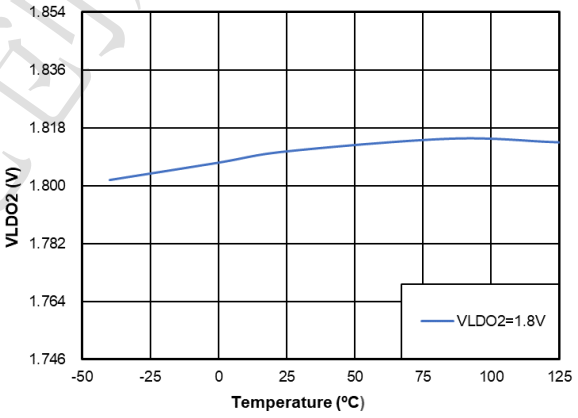
VOUT1 = 0.8V

Figure 26. LDO 1 Output Voltage vs. Temperature



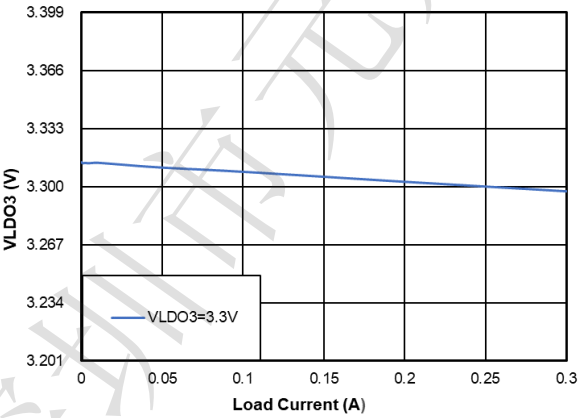
VLDO2 = 1.8V

Figure 27. LDO 2 Output Voltage vs. Load Current



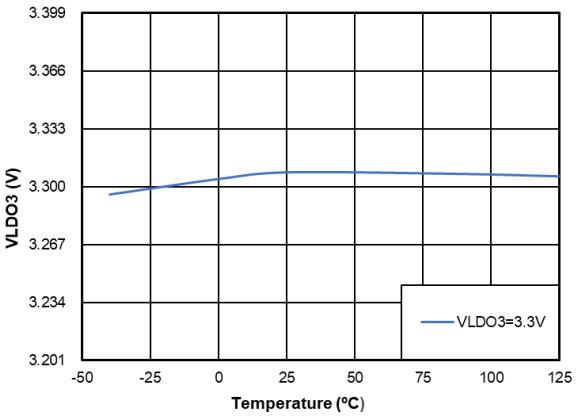
VLDO2 = 1.8V

Figure 28. LDO 2 Output Voltage vs. Temperature



VLDO3 = 3.3V

Figure 29. LDO 3 Output Voltage vs. Load Current



VLDO3 = 3.3V

Figure 30. LDO 3 Output Voltage vs. Temperature

Typical Performance Characteristics (Continued)

All test condition: V_{AVIN} = V_{PVINX} = 5 V, T_A = +25°C, unless otherwise noted.

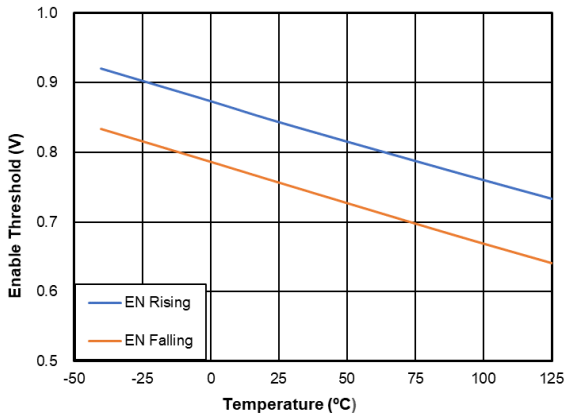


Figure 31. EN Threshold Voltage vs. Temperature

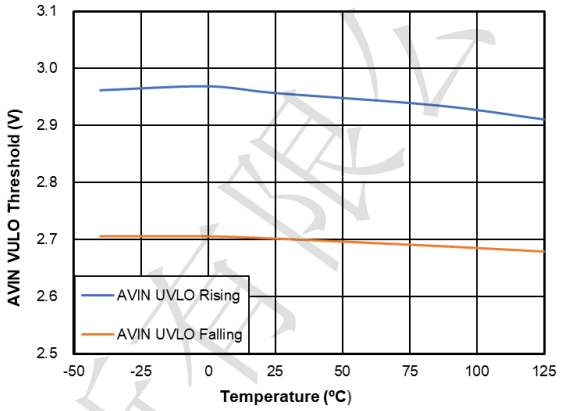
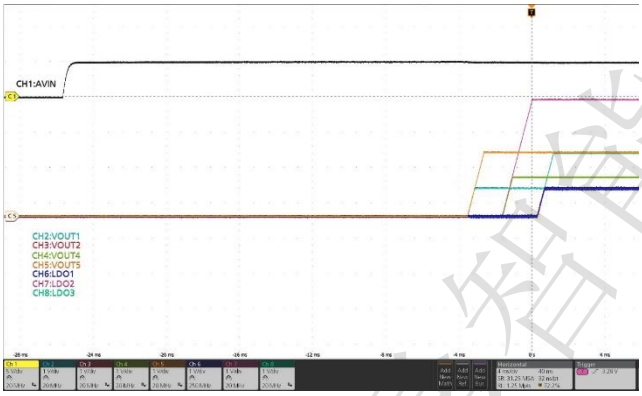
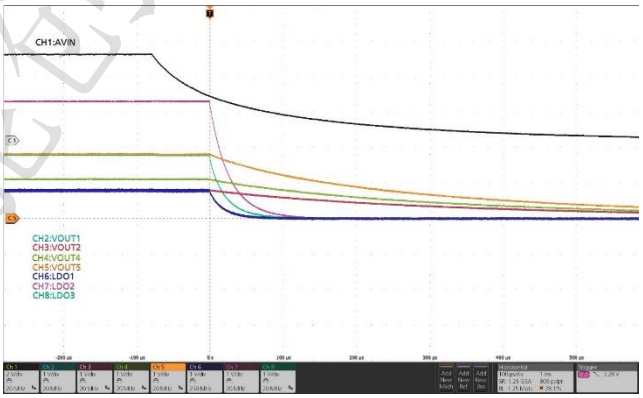


Figure 32. AVIN UVLO Voltage vs. Temperature



HPU3501A10CQNXMA and HPU3501A10CQNXMB

Figure 33. Startup Waveform by AVIN



HPU3501A10CQNXMA and HPU3501A10CQNXMB

Figure 34. Shutdown Waveform by AVIN

HPU3501A10CQNXMA and HPU3501A10CQNXMB

Figure 35. Shutdown Waveform by EN

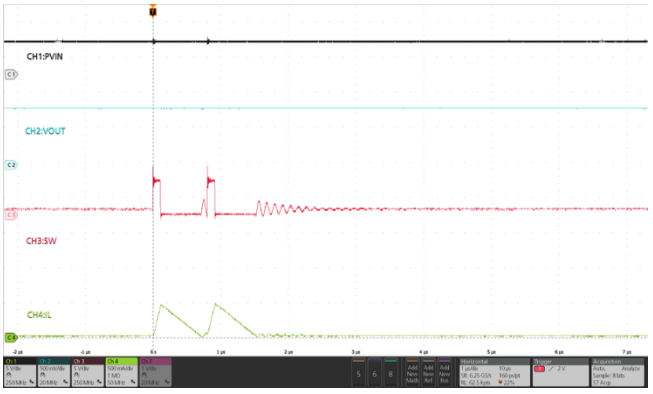


Figure 36. Switching Waveform at No Load

Typical Performance Characteristics (Continued)

All test condition: V_{AVIN} = V_{PVINX} = 5 V, T_A = +25°C, unless otherwise noted.

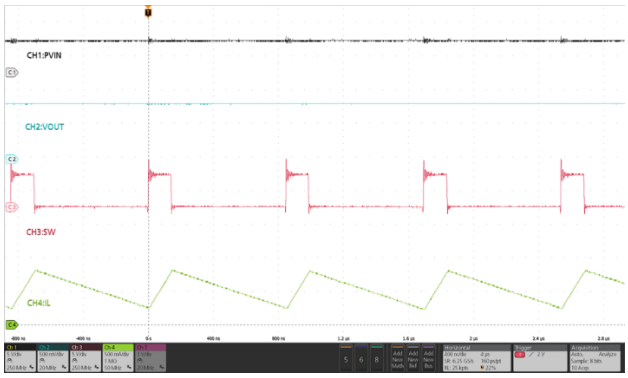


Figure 37. Switching Waveform at 0.5A Load

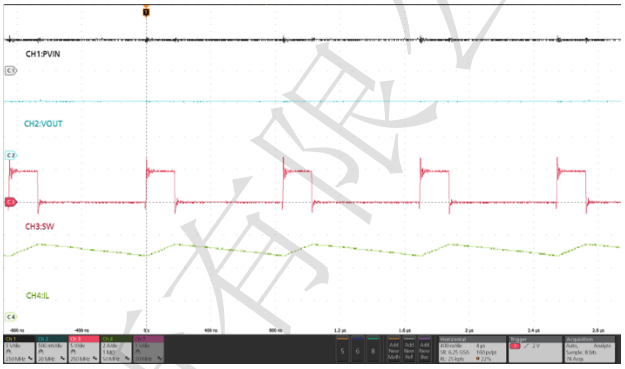
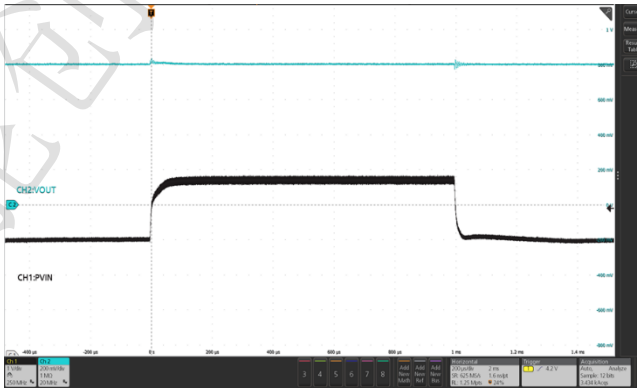


Figure 38. Switching Waveform at 4A Load

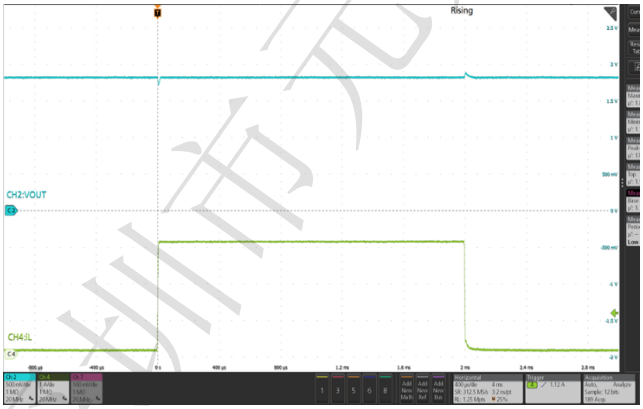
Load Current: 0A – 4A – 0A, VOUTx=0.8V

Figure 39. Buck 1-4 Load Transient



PVINx: 3.3V – 5V – 3.3V, VOUTx=0.8V

Figure 40. Buck 1-4 Line Transient



Load Current: 0A – 3A – 0A, VOUT5=1.8V

Figure 41. Buck 5 Load Transient

PVIN5: 3.3V – 5V – 3.3V, VOUT5=1.8V

Figure 42. Buck 5 Line Transient

Detailed Description

Overview

The HPU3501 is a power management unit integrating five synchronous switching buck converters, three low dropout linear regulators, and one real time clock.

The switching frequency of the five buck converters is 1.2MHz. The first buck converter and the second buck converter of the HPU3501 can be configured to work in dual phase mode. The third buck converter and the fourth buck converter of the HPU3501 also can be configured to work in dual phase mode.

The HPU3501 adopts peak current control scheme on the buck converters to provide quick response to the load current transient. Thus, it achieves excellent output voltage regulation with small output capacitance.

Functional Block Diagram

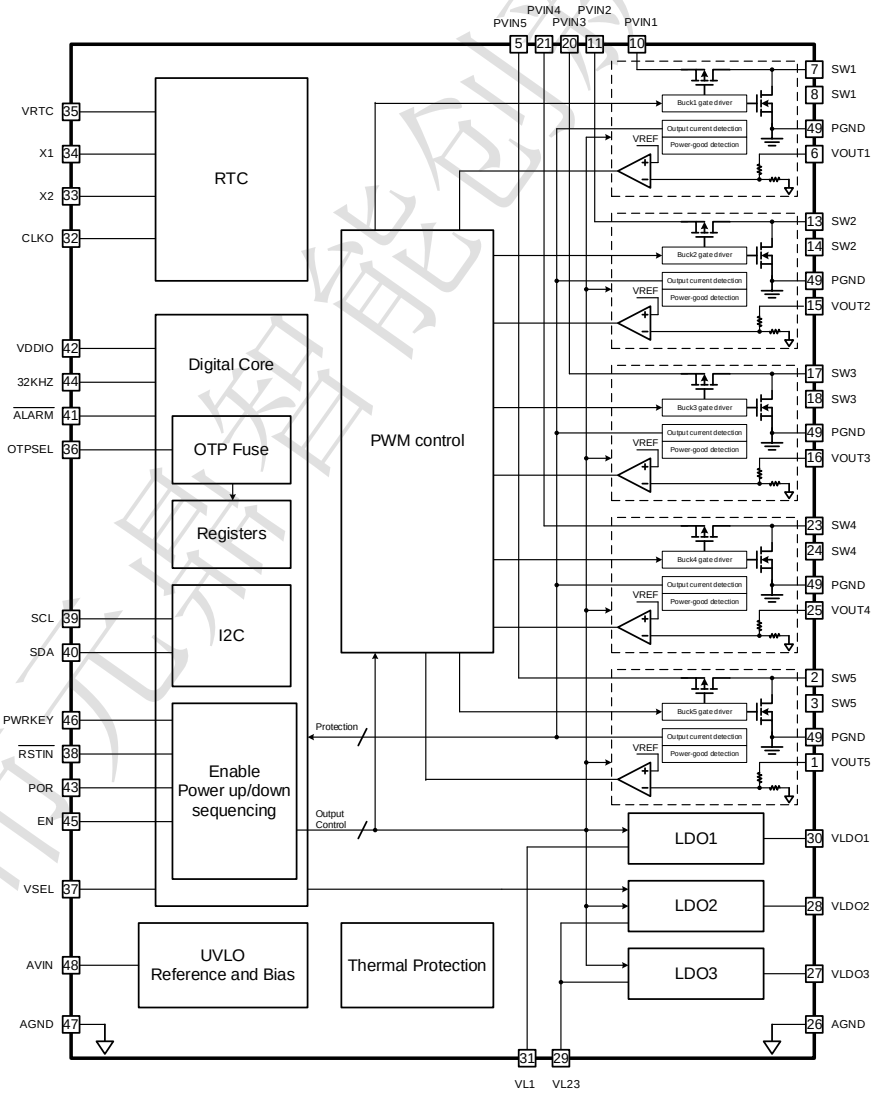


Figure 43. Functional Block Diagram

Feature Description

Power-up and Shutdown Sequence

The HPU3501 supports different features by factory one-time programmable (OTP) functions, such as the to disable or enable the power ON/OFF key input, and different I^2C slave address.

For device without power ON/OFF key input, when the input power supply is above the UVLO threshold of 3.0V, the device is enabled and starts up the power rails by a pre-defined power-on sequence in factory. For device with power ON/OFF key input, when the input power supply is above the UVLO threshold of 3.0V, the device does not start up until it detects the voltage falling edge of the PWRKEY pin and the PWRKEY pin is kept at low voltage level for more than 10ms.

When the 32.768kHz clock has appeared at the CLKO pin, the HPU3501 starts power up. The power-up sequence of each power rail and the interval delay time between two sequential power rails are pre-defined by the internal OTP registers which are set in factory.

After startup, the device without power ON/OFF key input function never goes into shutdown mode unless the input power is removed. However, the device with power ON/OFF key input function can use the power-down acknowledgement input (RSTIN_N pin) and the power ON/OFF key input (PWRKEY pin) to disable the device. When the device detects the PWRKEY pin and the RSTIN_N pin both in low level for more than 10ms, the device goes into shutdown sequence and turns off all power rails.

The power-up and shutdown timing sequence of the device with power ON/OFF key input function is shown in Figure 44.

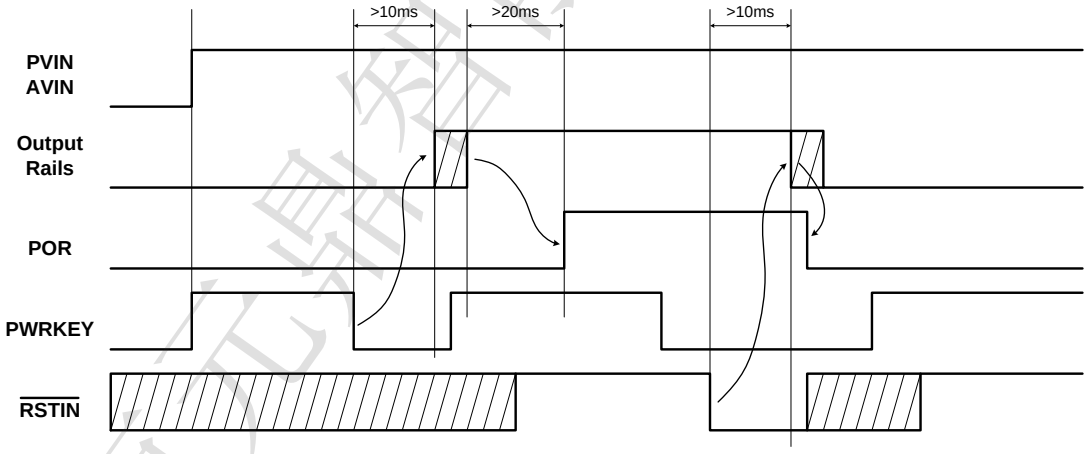


Figure 44. Power-up and shutdown sequence of the device with power ON/OFF key input

Enable and Disable

Each power rail can be enabled and disabled by a bit in the ENABLE register. In addition, the EN pin can enable and disable a group of power rails when the enable bits of the corresponding power rails are set in the EN_PIN_RMPR register by a SoC after power up.

The EN pin overrides the ENABLE register setting. When a power rail is controlled by the EN pin with the corresponding bit in the EN_PIN_RMPR register, the high level of the EN pin turns on the power rail and the

low level of the EN pin disables the power rail regardless of the corresponding ENABLE register settings.

Output Voltage Programming

The output voltages of the buck converter 1 to 4 are programmable from 0.6V to 1.275V through I^2C interface. The voltage step is 5mV. The output voltage of the buck converter 5 is programmable from 0.6V to 3.825V through I^2C interface. The voltage step is 15mV. The output voltage of the LDO 1 is programmable from 0.6V to 1.3V through I^2C interface. The voltage step is 10mV. The output voltages of the LDO 2 and the LDO 3 are programmable from 1.2V to 3.7V through I^2C interface. The voltage step is 20mV. The LDO2 has two output voltages selected by the VSEL pin. When the VSEL pin is in default low level, the LDO2 selects the voltage set in the LDO2_VOUT_CFG1R register. When the VSEL pin is pulled up to a high level, the LDO2 selects the voltage set in the LDO2_VOUT_CFG2R register.

Voltage Rising Slew Rate

During startup, the rising voltage slew rate of each power rail is adjustable by OTP setting in factory. There are eight slew rate options for buck converters and LDOs. The detailed voltage rising slew rate options are described in the Register Maps section. After startup, the slew rate settings can be read in the registers.

Dual Phase Mode

The buck converter 1 and buck converter 2 can be configured as dual phase mode with 180-degree out of phase. The buck converter 3 and buck converter 4 also can be configured as dual phase mode with 180-degree output of phase. In dual phase mode, the feedback voltages at the VOUT2 and VOUT4 pins are ignored. Dual phase operating minimizes the required input capacitance and minimizes the inductor current ripple for large load current.

Output Over Current Protection

Each buck converter of the HPU3501 has output over current protection. The over current limit is set in each buck converter's register through I^2C. The current limit for the buck converter 1 and the buck converter 2 can be set to 4A, 5A, 6A or 7A. The current limit for the buck converter 3, buck converter 4 and buck converter 5 can be set to 3A, 4A, 5A or 6A. When the output current of any buck trips the setting current limit for more than the pre-set switching cycles in the OTP registers, the HPU3501 sets the OCP flag in the register and goes into fault protection. See more detailed descriptions in the section of the Auto-Retry and Latch-off in Fault Protection.

Real Time Clock

The HPU3501 has a real time clock. The real time clock operates with an external 32.768kHz crystal. The internal RTC has registers providing year, month, day, hour, minute and second information, which can be read and written by a host processor. The HPU3501 provides alarm registers to set desired time of day, hour,

minute and second. When the alarm time is reached, the HPU3501 outputs the ALARM_N signal to inform the processor that the set time is reached. The alarm function can be disabled by the ALARM_EN bit the in the RTC configuration register. When the alarm function is disabled, the ALARM_N pin always output high level.

When a host processor initializes the RTC calendar registers, the host processor must set the INIT bit in the RTC_ISR register to stop the RTC counting the time. The calendar registers are not allowed to be changed until the INIT_F bit is changed to “1” by the HPU3501 meaning the RTC is in the initialization state. After the calendar registers are updated in the initialization state, the host processor must reset the INIT bit to “0” to start the RTC.

The Alarm registers of the RTC can be updated by the host processor only when the alarm function is disabled by resetting the ALARM_EN bit to “0” or the RTC is in initialization state.

Master and Slave Operating

The HPU3501 can operate in parallel. One is set as master PMIC and another one is set as slave PMIC. The OTPSEL pin selects the device mode. Setting the OTPSEL pin low voltage selects master PMIC mode while setting the OTPSEL pin high voltage selects slave PMIC mode. Both master and slave PMICs have their own default power-up sequencing, power-down sequencing, and output voltages settings. In addition, the RTC of the slave PMIC is disabled and the master PMIC must feed the 32.768kHz clock into the slave PMIC by connecting two CLKO pins together. Figure 45 shows the connections between the master and slave PMICs.

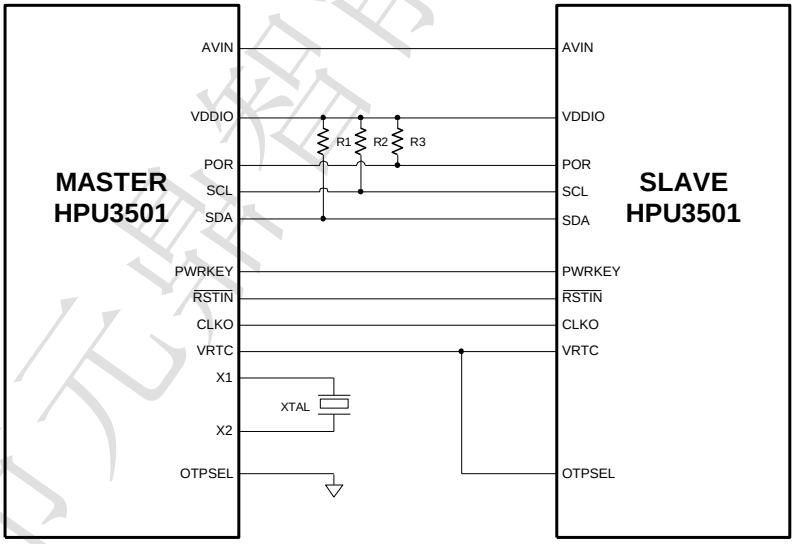


Figure 45. Connections between the master and slave PMICs

Thermal Shutdown Protection

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered, the HPU3501 turns off all power rails until the junction temperature falls below typically 125°C, then the device starts power-up again.

Auto-retry and Latch-off in Fault Protection

When OCP, OTP or OVP fault condition happens, the HPU3501 will record the fault count in the Device Status register, shut down all power rails and pull down the POR pin to low. After waiting for a pre-defined time in the FAULT_CFG register, the HPU3501 automatically re-starts up and outputs power rails again. If the fault condition disappears, the HPU3501 will go into normal operation. If the fault condition still exists, the HPU3501 increases the fault count in the register, shuts down, pulls down the POR pin and re-starts up again. The HPU3501 automatically retries the times which is set in the FAULT_CFG register. If the fault count reaches the retry times set in the FAULT_CFG register, the HPU3501 will latch off. To enable the HPU3501 after latch-off in fault protection, the power supply for the HPU3501 must be toggled.

When the latch-off of fault protection is not required, the fault count in the register must be cleared by writing “1” into the TRY_CNT_CLR bit in the FAULT_CFG register. Thus, the fault count recorded in the Device Status register never reach the preset latch-off threshold.

I²C Series Interface

The HPU3501 uses I²C interface for flexible parameter programming. I²C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). I²C devices can be considered as masters or slaves when performing data transfers. A master is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The HPU3501 operates as a slave device with addresses set by the OTPSEL pin as shown in the Product Family table. Receiving control inputs from the master device like a processor reads and writes the internal registers 00h through 1Fh. The I²C interface of the HPU3501 supports standard mode (up to 100 kHz), fast mode (up to 400 kHz) and fast mode plus (up to 1000 kHz). Both SDA and SCL must be connected to the positive supply voltage through current sources or pull-up resistors. When the bus is free, both lines are in high voltage.

Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high level or low level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

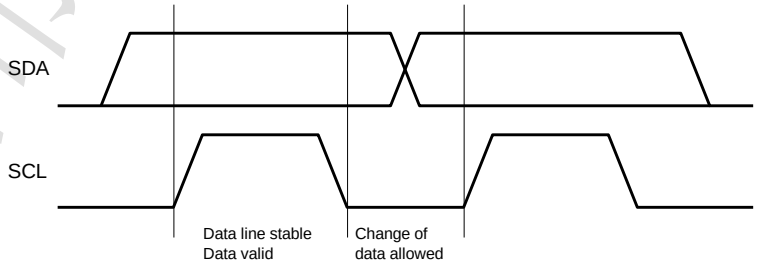


Figure 46. I²C Data Validity

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high level to low level transition on the SDA line while SCL is at high level defines a START condition. A low level to high level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

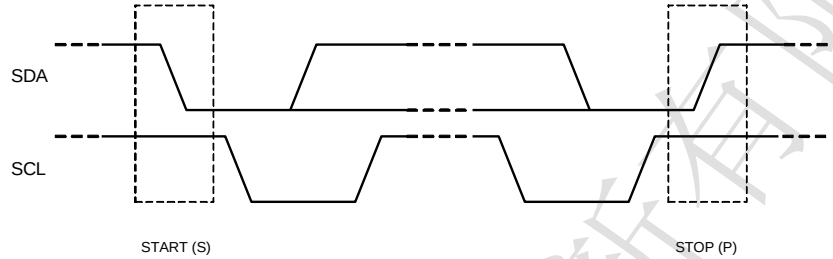


Figure 47. I²C START and STOP Conditions

Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

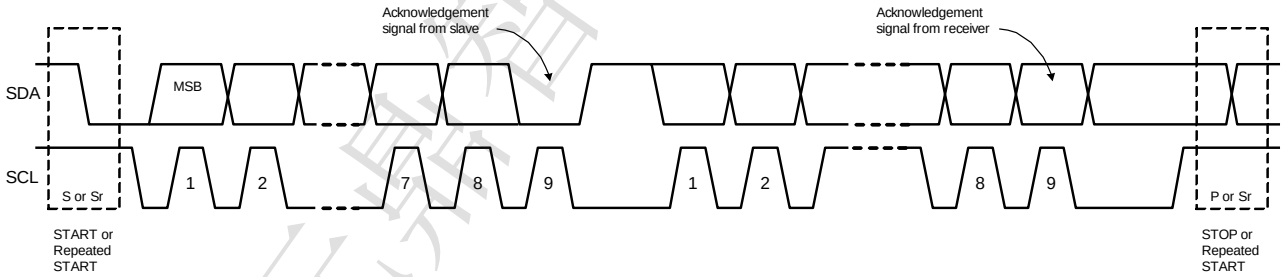


Figure 48. Byte Format

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledgment occurs after each byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received, and another byte may be sent. All clock pulses, including the acknowledgment at the 9th clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line to low level and it remains stable low level during the high level period of this clock pulse. The Not Acknowledge signal is when SDA remains high level during the 9th clock pulse. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

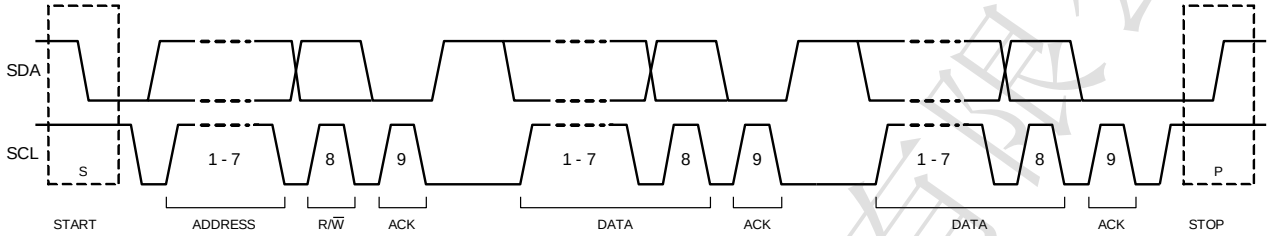


Figure 49. Slave Address and Data Direction

Single Byte Read and Write

Figure 50 and Figure 51 show the single-byte write and single-byte read format of the I²C communication.

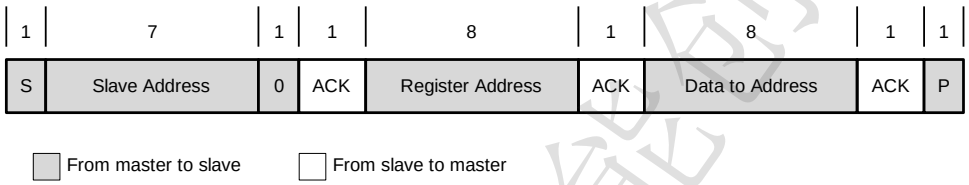


Figure 50. Single-byte Write

Figure 51. Single-byte Read

If the register address is not defined, the HPU3501 sends back NACK and goes back to the idle state.

Multi-byte Write and Multi-byte Read

The HPU3501 supports multi-byte write and multi-bye read as shown in Figure 52 and Figure 53.

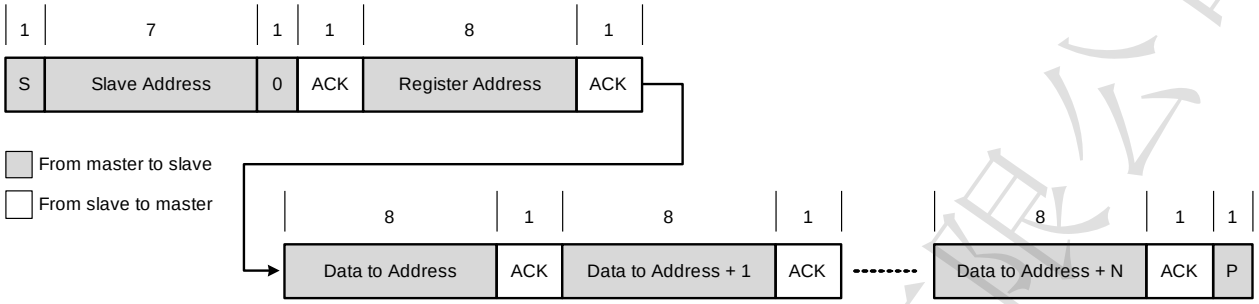


Figure 52. Multi-byte Write

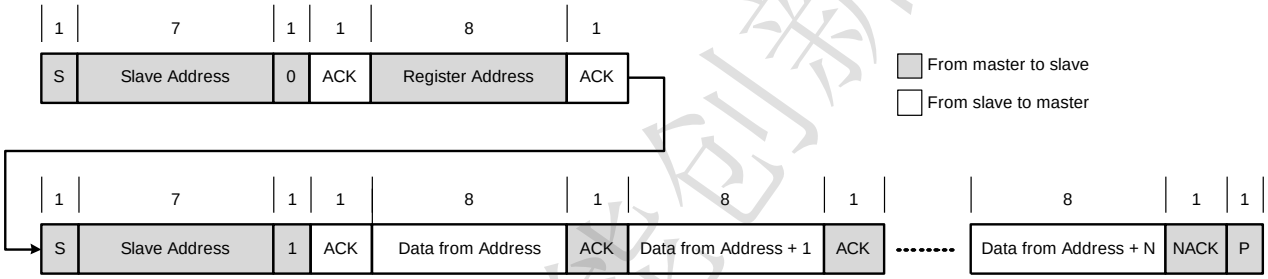


Figure 53. Multi-byte Read

Register Maps

Table 1 lists the memory-mapped registers in the HPU3501. All register addresses not listed in the Table 1 should be considered as reserved locations, and the register contents should not be modified. The reset values listed for each register are only for HPU3501A10CQNXMA as an example. Other PMIC devices may have different reset values.

Table 1. Device Registers

Address	Register Name	Description	Section
00h	CHIP_ID	Chip ID	Chip ID Register
01h-02h	Reserved	Reserved for internal use only	
03h	STS	Status of the PMIC	Device Status Register
04h	ERR_STS	Error status of the PMIC	Device Error Status Register
05h	OCP_FLAG	Over current flag for each buck converter and LDO	OCP Flag Register
06h	EN_PIN_RMPR	EN pin control mapping to buck converters and LDOs	EN Pin Mapping Register
07h	PWRKEY_CFGR	Timeout setting for RSTIN_N detection	Power Key Detection Register
08h	OCP_CFG1R	Over current threshold setting for buck converter 1, buck converter 2 and buck converter 3	OCP Configuration 1 Register

09h	OCP_CFG2R	Over current threshold setting for buck converter 4 and buck converter 5	OCP Configuration 2 Register
0Ah	FAULT_CFGR	OCP and OTP configuration	Fault Configuration Register
0Bh	PWR_SQC_STEP_CFGR	Step time setting for power-up and power-down sequence	Power Sequencing Step Configuration Register
0Ch	RTC_LDO_TRIM	RTC LDO output voltage trim	RTC LDO Trim Register
0Dh-0Fh	Reserved		
10h	ENABLE	Channel enable	Enable Register
11h	BUCK_DP_STSR	Dual phase enable	Buck Dual Phase Setting Register
12h	BUCK_SLEW_RATE1R	Slew rate setting value of buck converter 1 and buck converter 2	Buck Slew Rate Setting 1 Register
13h	BUCK_SLEW_RATE2R	Slew rate setting value of buck converter 3 and buck converter 4	Buck Slew Rate Setting 2 Register
14h	BUCK_SLEW_RATE3R	Slew rate setting value of buck converter 5 and LDO3	Buck Slew Rate Setting 3 Register
15h	LDO_SLEW_RATER	Slew rate setting value of LDO1 and LDO2	LDO Slew Rate Setting Register
16h	BUCK_FCPWM_CFGR	Forced PWM mode enable	Buck Forced PWM Mode Register
17h	BUCK1_PWR_SQC_CFGR	Power-up and power-down group setting for buck converter 1	Buck 1 Power Sequence Configuration Register
18h	BUCK1_VOUT_CFGR	Output voltage setting of the buck converter 1	Buck 1 Output Voltage Setting Register
19h	BUCK2_PWR_SQC_CFGR	Power-up and power-down group setting for buck converter 2	Buck 2 Power Sequence Configuration Register
1Ah	BUCK2_VOUT_CFGR	Output voltage setting of the buck converter 2	Buck 2 Output Voltage Setting Register
1Bh	BUCK3_PWR_SQC_CFGR	Power-up and power-down group setting for buck converter 3	Buck 3 Power Sequence Configuration Register
1Ch	BUCK3_VOUT_CFGR	Output voltage setting of the buck converter 3	Buck 3 Output Voltage Setting Register
1Dh	BUCK4_PWR_SQC_CFGR	Power-up and power-down group setting for buck converter 4	Buck 4 Power Sequence Configuration Register
1Eh	BUCK4_VOUT_CFGR	Output voltage setting of the buck converter 4	Buck 4 Output Voltage Setting Register
1Fh	BUCK5_PWR_SQC_CFGR	Power-up and power-down group setting for buck converter 5	Buck 5 Power Sequence Configuration Register
20h	BUCK5_VOUT_CFGR	Output voltage setting of the buck converter 5	Buck 5 Output Voltage Setting Register

21h	LDO1_PWR_SQC_CFGR	Power-up and power-down group setting for LDO 1	LDO 1 Power Sequence Configuration Register
22h	LDO1_VOUT_CFGR	Output voltage setting of the LDO 1	LDO 1 Output Voltage Setting Register
23h	LDO2_PWR_SQC_CFGR	Power-up and power-down group setting for LDO 2	LDO 2 Power Sequence Configuration Register
24h	LDO2_VOUT_CFG1R	Output voltage setting of the LDO 2 when the VSEL pin is at low level	LDO 2 Output Voltage Setting Register 1
25h	LDO2_VOUT_CFG2R	Output voltage setting of the LDO 2 when the VSEL pin is at high level	LDO 2 Output Voltage Setting Register 2
26h	LDO3_PWR_SQC_CFGR	Power-up and power-down group setting for LDO 3	LDO 3 Power Sequence Configuration Register
27h	LDO3_VOUT_CFGR	Output voltage setting of the LDO 3	LDO 3 Output Voltage Setting Register
28h-2Fh	Reserved		
30h	RTC_ISR	RTC initialization and status	RTC Initialization and Status Register
31h	RTC_YEAR	RTC year	RTC YEAR Register
32h	RTC_MONTH	RTC month	RTC Month Register
33h	RTC_DAY	RTC day	RTC DATE Register
34h	RTC_HOUR	RTC hour	RTC HOUR Register
35h	RTC_MIN	RTC minute	RTC Minute Register
36h	RTC_SEC	RTC second	RTC Second Register
37h	RTC_ALARM_DAY	RTC alarm day setting	RTC Alarm Date Register
38h	RTC_ALARM_HOUR	RTC alarm hour setting	RTC Alarm Hour Register
39h	RTC_ALARM_MIN	RTC alarm minute setting	RTC Alarm Minute Register
3Ah	RTC_ALARM_SEC	RTC alarm second setting	RTC Alarm Second Register

Chip ID Register (Address = 00h)

The HPU3501 has an 8-bit chip ID stored in the CHIP_ID register. Different devices or versions have different chip ID values.

7	6	5	4	3	2	1	0
CHIP_ID							
R – 00000110b							

Figure 54. CHIP_ID

Table 2. CHIP ID Register Field Description

Bit	Field	Type	Reset	Description
7-0	Chip ID	R	00000110	Different chip types or versions 00000000: Blank chip

				00000110: HPU3501A10CQNXMA 00000111: HPU3501A10CQNXMB 00001100: HPU3501A13CQNXMA 00001101: HPU3501A13CQNXMB

Device Status Register（Address=03h）

7	6	5	4	3	2	1	0
FUES_RDY	FUSE_BD	OTP_SEL	OVP_EN	LDO2_VSEL	POWER_KEY_OP	POR_CLR_TRY_CNT	
R - 11000000b							

Figure 55. STS

Table 3. Device Status Register Field Description

Bit	Field	Type	Reset	Description
7	FUSE_RDY	R	1	Fuse ready flag. Active high 0: Fuse not ready 1: Fuse ready and start to load OTP
6	FUSE_BD	R	1	Flag for fuse burn 0: not burnt 1: burnt
5	OTP_SEL	R	0	PMIC mode selection 0: Master 1: Slave
4	OVP_EN	R	0	Over-voltage enable 0: OVP disabled 1: OVP enabled
3	LDO2_VSEL	R	0	LDO2 output voltage selection 0: LDO2 output voltage 1 1: LDO2 output voltage 2
2	POWER_KEY_OP	R	0	Power key detection 0: Power key detection disabled 1: Power key detection enabled
1:0	FAULT_TRY_CNT	R	00	Times to pull down the POR pin after fault detected. 00: 0 01: 1 10: 2 11: 3

Device Error Status Register（Address=04h）

7	6	5	4	3	2	1	0
LDOX_PG_LATE	BUCK5_PG_LATE	BUCK4_PG_LATE	BUCK3_PG_LATE	BUCK2_PG_LATE	BUCK1_PG_LATE	OVP_FLAG	OTP_FLAG
R - 00000000b							

Figure 56. ERR_STS

Table 4. Device Error Status Register Field Description

Bit	Field	Type	Reset	Description
7	LDOX_PG_LATE	R/W1C	0	LDOx power-up status 0: Power up properly 1: Power up late after normal time Writing “1” into this bit clears the bit to “0”
6	BUCK5_PG_LATE	R/W1C	0	Buck5 power-up status 0: Power up properly 1: Power up late after normal time Writing “1” into this bit clears the bit to “0”
5	BUCK4_PG_LATE	R/W1C	0	Buck4 power-up status 0: Power up properly 1: Power up late after normal time Writing “1” into this bit clears the bit to “0”
4	BUCK3_PG_LATE	R/W1C	0	Buck3 power-up status 0: Power up properly 1: Power up late after normal time Writing “1” into this bit clears the bit to “0”
3	BUCK2_PG_LATE	R/W1C	0	Buck2 power-up status 0: Power up properly 1: Power up late after normal time Writing “1” into this bit clears the bit to “0”
2	BUCK1_PG_LATE	R/W1C	0	Buck1 power-up status 0: Power up properly 1: Power up late after normal time Writing “1” into this bit clears the bit to “0”
1	OVP_FLAG	R/W1C	0	Over-voltage flag 0: No over-voltage 1: Over-voltage happened Writing “1” into this bit clears the bit to “0”
0	OTP_FLAG	R/W1C	0	Over-temperature flag 0: No over-temperature 1: Over-temperature happened Writing “1” into this bit clears the bit to “0”

OCP Flag Register (Address=05h)

7	6	5	4	3	2	1	0
LDO3_OCP_FLAG	LDO2_OCP_FLAG	LDO1_OCP_FLAG	BUCK5_OCP_FLAG	BUCK4_OCP_FLAG	BUCK3_OCP_FLAG	BUCK2_OCP_FLAG	BUCK1_OCP_FLAG
R - 00000000b							

Figure 57. OCP_FLAG

Table 5. OCP Flag Register Field Description

Bit	Field	Type	Reset	Description
7	LDO3_OCP_FLAG	R/W1C	0	LDO3 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”
6	LDO2_OCP_FLAG	R/W1C	0	LDO2 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”
5	LDO1_OCP_FLAG	R/W1C	0	LDO1 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”
4	BUCK5_OCP_FLAG	R/W1C	0	BUCK5 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”
3	BUCK4_OCP_FLAG	R/W1C	0	BUCK4 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”
2	BUCK3_OCP_FLAG	R/W1C	0	BUCK3 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”
1	BUCK2_OCP_FLAG	R/W1C	0	BUCK2 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”
0	BUCK1_OCP_FLAG	R/W1C	0	BUCK1 OCP flag 0: No OCP 1: OCP happened Writing “1” into this bit clears the bit to “0”

EN Pin Mapping Register (Address=06h)

7	6	5	4	3	2	1	0
LDO3_RMP	LDO2_RMP	LDO1_RMP	BUCK5_RMP	BUCK4_RMP	BUCK3_RMP	BUCK2_RMP	BUCK1_RMP
R - 00000000b							

Figure 58. EN_PIN_RMPR

Table 6. OCP Flag Register Field Description

Bit	Field	Type	Reset	Description
7	LDO3_RMP	R/W	0	LDO3 Enable mapped to the EN pin 0: LDO3 not controlled by the EN pin 1: LDO3 controlled by the EN pin
6	LDO2_RMP	R/W	0	LDO2 Enable mapped to the EN pin 0: LDO2 not controlled by the EN pin 1: LDO2 controlled by the EN pin
5	LDO1_RMP	R/W	0	LDO1 Enable mapped to the EN pin 0: LDO1 not controlled by the EN pin 1: LDO1 controlled by the EN pin
4	BUCK5_RMP	R/W	0	BUCK5 Enable mapped to the EN pin 0: BUCK5 not controlled by the EN pin 1: BUCK5 controlled by the EN pin
3	BUCK4_RMP	R/W	0	BUCK4 Enable mapped to the EN pin 0: BUCK4 not controlled by the EN pin 1: BUCK4 controlled by the EN pin
2	BUCK3_RMP	R/W	0	BUCK3 Enable mapped to the EN pin 0: BUCK3 not controlled by the EN pin 1: BUCK3 controlled by the EN pin
1	BUCK2_RMP	R/W	0	BUCK2 Enable mapped to the EN pin 0: BUCK2 not controlled by the EN pin 1: BUCK2 controlled by the EN pin
0	BUCK1_RMP	R/W	0	BUCK1 Enable mapped to the EN pin 0: BUCK1 not controlled by the EN pin 1: BUCK1 controlled by the EN pin

Power Key Detection Register (Address=07h)

7	6	5	4	3	2	1	0
RESERVED						PDACK_DET	
R - 00000000b							

Figure 59. PWRKEY_CFG

Table 7. Power-up and Power-down Sequencing Step Configuration Register Field Description

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	000000	Reserved
1:0	PDACK_DET	R/W	00	When PWRKEY is enabled, set the detection time limit for RSTIN_N signal from SoC after PWRKEY is low for 20ms. 00: 8s 01: 6s 10: 4s 11: 2s

OCP Configuration 1 Register (Address=08h)

7	6	5	4	3	2	1	0
RESERVED		BUCK3_OCP_SET		BUCK2_OCP_SET		BUCK1_OCP_SET	
R - 00111111b							

Figure 60. OCP_CFG1R

Table 8. OCP Configuration 1 Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5:4	BUCK3_OCP_SET	R/W	11	Buck 3 OCP threshold 00: 4A 01: 5A 10: 6A 11: 7A
3:2	BUCK2_OCP_SET	R/W	11	Buck 2 OCP threshold 00: 4A 01: 5A 10: 6A 11: 7A
1:0	BUCK1_OCP_SET	R/W	11	Buck 1 OCP threshold 00: 4A 01: 5A 10: 6A 11: 7A

OCP Configuration 2 Register (Address=09h)

7	6	5	4	3	2	1	0
RESERVED		BUCK5_OCP_SET		RESERVED		BUCK4_OCP_SET	
R – 00110011b							

Figure 61. OCP_CFG2R

Table 9. OCP Configuration 2 Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5:4	BUCK5_OCP_SET	R/W	11	Buck 5 OCP threshold 00: 3A 01: 4A 10: 5A 11: 6A
3:2	RESERVED	R	00	Reserved
1:0	BUCK4_OCP_SET	R/W	11	Buck 4 OCP threshold 00: 4A 01: 5A 10: 6A 11: 7A

Fault Configuration Register （Address=0Ah）

7	6	5	4	3	2	1	0
TRY_CNT_CLR	POR_MAX_TRY_TIME		POR_INTERVAL				
R - 01100001b							

Figure 62. FAULT_CFGR

Table 10. Fault Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	TRY_CNT_CLR	R/W1C	0	Clear the POR reset count by writing 1 if the faut (OCP, OTP or OVP) flag has disappeared. 0: Not clear 1: Clear
6:5	POR_MAX_TRY_TIME	R/W	11	POR repeat times after OCP, OTP or OVP happens. 00: 0 01: 1 10: 2 11: 3
4:0	POR_INTERVAL	R/W	00001	Waiting time between power-down and next power-up when OCP, OTP or OVP happened. 00000: 100ms

				00001: 200ms …… 10011: 2000ms …… 11111: 3200ms

Power Sequencing Step Configuration Register (Address=0Bh)

7	6	5	4	3	2	1	0
RESERVED				SQC_STEP			
R - 00001101b							

Figure 63. POWER_SQC_STEP_CFGR

Table 11. Power-up and Power-down Sequencing Step Configuration Register Field Description

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0000	Reserved
3:0	SQC_STEP	R/W	1101	Power up and power down sequence interval time between 305us and 2135us. 0000: 305us 0001: 305us+122us 0010: 305us+2x122us …… 1111: 305us+15x122us;

RTC LDO Trim Register (Address=0Ch)

7	6	5	4	3	2	1	0
RESERVED				RTC_LDO_TRIM			
R - 00000000b							

Figure 64. RTC_LDO_TRIM

Table 12. RTC LDO Trim Register Field Description

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0000	Reserved

3:0	RTC_LDO_TRIM	R/W	0000	The trim for RTC LDO output. Step 2% 0000: no change 0001: +2% 0002: +4% …… 01111: +14% 1000: -16% 1001: -14% …… 1000: -2%

Enable Register (Address=10h)

7	6	5	4	3	2	1	0
LDO3_EN	LDO2_EN	LDO1_EN	BUCK5_EN	BUCK4_EN	BUCK3_EN	BUCK2_EN	BUCK1_EN
R - 11111111b							

Figure 65. ENABLE

Table 13. Enable Register Field Description

Bit	Field	Type	Reset	Description
7	LDO3_EN	R/W	1	LDO3 enable control when LDO3 is not controlled by the EN pin 0: disabled 1: enabled
6	LDO2_EN	R/W	1	LDO2 enable control when LDO2 is not controlled by the EN pin 0: disabled 1: enabled
5	LDO1_EN	R/W	1	LDO1 enable control when LDO1 is not controlled by the EN pin 0: disabled 1: enabled
4	BUCK5_EN	R/W	1	Buck5 enable control when Buck5 is not controlled by the EN pin 0: disabled 1: enabled
3	BUCK4_EN	R/W	1	Buck4 enable control when Buck4 is not controlled by the EN pin 0: disabled

				1: enabled
2	BUCK3_EN	R/W	1	Buck3 enable control when Buck3 is not controlled by the EN pin 0: disabled 1: enabled
1	BUCK2_EN	R/W	1	Buck2 enable control when Buck2 is not controlled by the EN pin 0: disabled 1: enabled
0	BUCK1_EN	R/W	1	Buck1 enable control when Buck1 is not controlled by the EN pin 0: disabled 1: enabled

Buck Dual Phase Setting Register (Address=11h)

7	6	5	4	3	2	1	0
RESERVED			BUCK3/4_DP	RESERVED			BUCK1/2_DP
R - 00000001b							

Figure 66. BUCK_DP_STSR

Table 14. Dual Phase Setting Register Field Description

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000	Reserved
4	BUCK3/4_DP	R	0	Dual phase setting for Buck 3 and Buck 4 0: Dual phase disabled. Work independently 1: Dual phase enabled
3:1	RESERVED	R	000	Reserved
0	BUCK1/2_DP	R	1	Dual phase setting for Buck 1 and Buck 2 0: Dual phase disabled. Work independently 1: Dual phase enabled

Buck Slew Rate Setting 1 Register (Address=12h)

7	6	5	4	3	2	1	0
RESERVED		BUCK2_SLEW_RATE			BUCK1_SLEW_RATE		
R - 00000000b							

Figure 67. BUCK_SLEW_RATE1R

Table 15. BUCK Slew Rate 1 Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved

5:3	BUCK2_SLEW_RATE	R	000	Buck2 slew rate 000: 2 mV/μs 001: 12 mV/μs 010: 24 mV/μs 011: 36 mV/μs 100: 42 mV/μs 101: 54 mV/μs 110: 60 mV/μs 111: 72 mV/μs
2:0	BUCK1_SLEW_RATE	R	000	Buck1 slew rate 000: 2 mV/μs 001: 12 mV/μs 010: 24 mV/μs 011: 36 mV/μs 100: 42 mV/μs 101: 54 mV/μs 110: 60 mV/μs 111: 72 mV/μs

Buck Slew Rate Setting 2 Register (Address=13h)

7	6	5	4	3	2	1	0
RESERVED		BUCK4_SLEW_RATE			BUCK3_SLEW_RATE		
R - 00000000b							

Figure 68. BUCK_SLEW_RATE2R

Table 16. BUCK Slew Rate 2 Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5:3	BUCK4_SLEW_RATE	R	000	Buck4 slew rate 000: 2 mV/μs 001: 12 mV/μs 010: 24 mV/μs 011: 36 mV/μs 100: 42 mV/μs 101: 54 mV/μs 110: 60 mV/μs 111: 72 mV/μs
2:0	BUCK3_SLEW_RATE	R	000	Buck3 slew rate 000: 2 mV/μs 001: 12 mV/μs 010: 24 mV/μs

				011: 36 mV/μs 100: 42 mV/μs 101: 54 mV/μs 110: 60 mV/μs 111: 72 mV/μs

Buck Slew Rate Setting 3 Register (Address=14h)

7	6	5	4	3	2	1	0
RESERVED		LDO3_SLEW_RATE			BUCK5_SLEW_RATE		
R - 00000000b							

Figure 69. BUCK_SLEW_RATE3R

Table 17. BUCK Slew Rate 3 Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5:3	LDO3_SLEW_RATE	R	000	LDO3 slew rate 000: 2 mV/μs 001: 6 mV/μs 010: 8 mV/μs 011: 12 mV/μs 100: 24 mV/μs 101: 48 mV/μs 110: 72 mV/μs 111: 96 mV/μs
2:0	BUCK5_SLEW_RATE	R	000	Buck5 slew rate 000: 2 mV/μs 001: 6 mV/μs 010: 12 mV/μs 011: 18 mV/μs 100: 36 mV/μs 101: 54 mV/μs 110: 72 mV/μs 111: 90 mV/μs

LDO Slew Rate Setting Register (Address=15h)

7	6	5	4	3	2	1	0
RESERVED		LDO2_SLEW_RATE			LDO1_SLEW_RATE		
R - 00000000b							

Figure 70. LDO_SLEW_RATER

Table 18. LDO Slew Rate Setting Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5:3	LDO2_SLEW_RATE	R	000	LDO2 slew rate 000: 2 mV/μs 001: 6 mV/μs 010: 8 mV/μs 011: 12 mV/μs 100: 24 mV/μs 101: 48 mV/μs 110: 72 mV/μs 111: 96 mV/μs
2:0	LDO1_SLEW_RATE	R	000	LDO1 slew rate 000: 2 mV/μs 001: 12 mV/μs 010: 24 mV/μs 011: 36 mV/μs 100: 42 mV/μs 101: 54 mV/μs 110: 60 mV/μs 111: 72 mV/μs

Buck Forced PWM Mode Register (Address=16h)

7	6	5	4	3	2	1	0
RESERVED			BUCK5_FPWM	BUCK4_FPWM	BUCK3_FPWM	BUCK2_FPWM	BUCK1_FPWM
R - 00000000b							

Figure 71. BUCK_FCPWM_CFGR

Table 19. BUCK Slew Rate 1 Register Field Description

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000	Reserved
4	BUCK5_FPWM	R/W	0	Buck5 works in forced PWM mode 0: Disabled 1: Enabled
3	BUCK4_FPWM	R/W	0	Buck4 works in forced PWM mode 0: Disabled 1: Enabled
2	BUCK3_FPWM	R/W	0	Buck3 works in forced PWM mode 0: Disabled 1: Enabled

1	BUCK2_FPWM	R/W	0	Buck2 works in forced PWM mode 0: Disabled 1: Enabled
0	BUCK1_FPWM	R/W	0	Buck1 works in forced PWM mode 0: Disabled 1: Enabled

Buck 1 Power Sequence Configuration Register (Address=17h)

7	6	5	4	3	2	1	0
RESERVED	BUCK1_PD_SQC			RESERVED	BUCK1_PU_SQC		
R - 00110011b							

Figure 72. BUCK1_POWER_SQC_CFGR

Table 20. BUCK1 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	BUCK1_PD_SQC	R/W	011	Buck1 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	BUCK1_PU_SQC	R/W	011	Buck1 power-up sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7

Buck1 Output Voltage Setting Register (Address=18h)

7	6	5	4	3	2	1	0
BUCK1_VOUT							
R - 10100000b							

Figure 73. BUCK1_VOUT_CFGR

Table 21. BUCK1 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	BUCK1_VOUT	R/W	10100000	Buck1 output voltage setting from 0.6V to 1.275V with step 5mV.

				00000000: 0V 00000001~01111000: 0.6V 01111001: 0.605V …… 11111111: 1.275V

Buck2 Power Sequence Configuration Register (Address=19h)

7	6	5	4	3	2	1	0
RESERVED	BUCK2_PD_SQC			RESERVED	BUCK2_PU_SQC		
R - 00010101b							

Figure 74. BUCK2_POWER_SQC_CFGR

Table 22. BUCK2 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	BUCK2_PD_SQC	R/W	001	Buck2 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	BUCK2_PU_SQC	R/W	101	Buck2 power-up sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7

Buck2 Output Voltage Setting Register (Address=1Ah)

7	6	5	4	3	2	1	0
BUCK2_VOUT							
R - 10100000b							

Figure 75. BUCK2_VOUT_CFGR

Table 23. BUCK2 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	BUCK2_VOUT	R/W	10100000	Buck2 output voltage setting from 0.6V to 1.275V with step 5mV. 00000000: 0V

				00000001~01111000: 0.6V 01111001: 0.605V …… 11111111: 1.275V

Buck3 Power Sequence Configuration Register (Address=1Bh)

7	6	5	4	3	2	1	0
RESERVED	BUCK3_PD_SQC			RESERVED	BUCK3_PU_SQC		
R - 00110011b							

Figure 76. BUCK3_POWER_SQC_CFGR

Table 24. BUCK3 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	BUCK3_PD_SQC	R/W	011	Buck3 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	BUCK3_PU_SQC	R/W	011	Buck3 power-up sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7

Buck3 Output Voltage Setting Register (Address=1Ch)

7	6	5	4	3	2	1	0
BUCK3_VOUT							
R - 10100000b							

Figure 77. BUCK3_VOUT_CFGR

Table 25. BUCK3 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	BUCK3_VOUT	R/W	10100000	Buck3 output voltage setting from 0.6V to 1.275V with step 5mV. 00000000: 0V 00000001~01111000: 0.6V

				01111001: 0.605V …… 11111111: 1.275V

Buck4 Power Sequence Configuration Register (Address=1Dh)

7	6	5	4	3	2	1	0
RESERVED	BUCK4_PD_SQC			RESERVED	BUCK4_PU_SQC		
R - 00100100b							

Figure 78. BUCK4_POWER_SQC_CFGR

Table 26. BUCK4 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	BUCK4_PD_SQC	R/W	010	Buck4 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	BUCK4_PU_SQC	R/W	100	Buck4 power-up sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7

Buck4 Output Voltage Setting Register (Address=1Eh)

7	6	5	4	3	2	1	0
BUCK4_VOUT							
R - 11011100b							

Figure 79. BUCK4_VOUT_CFGR

Table 27. BUCK4 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	BUCK4_VOUT	R/W	11011100	Buck4 output voltage setting from 0.6V to 1.275V with step 5mV. 00000000: 0V 00000001~01111000: 0.6V

				01111001: 0.605V …… 11111111: 1.275V

Buck5 Power Sequence Configuration Register (Address=1Fh)

7	6	5	4	3	2	1	0
RESERVED	BUCK5_PD_SQC			RESERVED	BUCK5_PU_SQC		
R - 00110011b							

Figure 80. BUCK5_POWER_SQC_CFGR

Table 28. BUCK5 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	BUCK5_PD_SQC	R/W	011	Buck5 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	BUCK5_PU_SQC	R/W	011	Buck5 power-up sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7

Buck5 Output Voltage Setting Register (Address=20h)

7	6	5	4	3	2	1	0
BUCK5_VOUT							
R - 01111000b							

Figure 81. BUCK5_VOUT_CFGR

Table 29. BUCK5 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	BUCK5_VOUT	R/W	01111000	Buck5 output voltage setting from 0V to 3.825V with step 15mV. The output voltage must be programmed larger than 0.6V. 00000000: 0V

				00000001: 0.015V 00000010: 0.030V …… 11111111: 3.825V

LDO1 Power Sequence Configuration Register (Address=21h)

7	6	5	4	3	2	1	0
RESERVED	LDO1_PD_SQC			RESERVED	LDO1_PU_SQC		
R - 00011001b							

Figure 82. LDO1_POWER_SQC_CFGR

Table 30. LDO1 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	LDO1_PD_SQC	R/W	001	LDO1 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	LDO1_PU_SQC	R/W	101	LDO1 power-up sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7

LDO1 Output Voltage Setting Register (Address=22h)

7	6	5	4	3	2	1	0
LDO1_VOUT							
R - 01010000b							

Figure 83. LDO1_VOUT_CFGR

Table 31. LDO1 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	LDO1_VOUT	R/W	01010000	LDO1 output voltage setting from 0.6V to 1.3V with step 10mV. 00000000: 0V 00000001~00111100: 0.6V

				00111101: 0.61V …… 10000001: 1.29V 10000010~11111111: 1.30V

LDO2 Power Sequence Configuration Register (Address=23h)

7	6	5	4	3	2	1	0
RESERVED	LDO2_PD_SQC			RESERVED	LDO2_PU_SQC		
R - 00100100b							

Figure 84. LDO2_POWER_SQC_CFGR

Table 32. LDO2 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	LDO2_PD_SQC	R/W	010	LDO2 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	LDO2_PU_SQC	R/W	100	LDO2 power-up sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7

LDO2 Output Voltage 1 Setting Register (Address=24h)

7	6	5	4	3	2	1	0
LDO2_VOUT1							
R - 10100101b							

Figure 85. LDO2_VOUT_CFG1R

Table 33. LDO2 Output 1 Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	LDO2_VOUT1	R/W	10100101	LDO2 output voltage setting from 1.2V to 3.7V with step 20mV. 00000000: 0V 00000001~00111100: 1.2V

				00111101: 1.22V …… 10111000: 3.68V 10111001~11111111: 3.70V

LDO2 Output Voltage 2 Setting Register (Address=25h)

7	6	5	4	3	2	1	0
LDO2_VOUT2							
R - 01011010b							

Figure 86. LDO2_VOUT_CFG2R

Table 34. LDO3 Output 2 Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	LDO2_VOUT2	R/W	01011010	LDO2 output voltage setting from 1.2V to 3.7V with step 20mV. 00000000: 0V 00000001~00111100: 1.2V 00111101: 1.22V …… 10111000: 3.68V 10111001~11111111: 3.70V

LDO3 Power Sequence Configuration Register (Address=26h)

7	6	5	4	3	2	1	0
RESERVED	LDO3_PD_SQC			RESERVED	LDO3_PU_SQC		
R - 00010101b							

Figure 87. LDO3_POWER_SQC_CFGR

Table 35. LDO3 Power Sequence Configuration Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	LDO3_PD_SQC	R/W	001	LDO3 power-down sequence 000: group 0 001: group 1 010: group 2 …… 111: group 7
3	RESERVED	R	0	Reserved
2:0	LDO3_PU_SQC	R/W	101	LDO3 power-up sequence 000: group 0

				001: group 1 010: group 2 …… 111: group 7

LDO3 Output Voltage Setting Register (Address=27h)

7	6	5	4	3	2	1	0
LDO3_VOUT							
R - 01011010b							

Figure 88. LDO3_VOUT_CFGR

Table 36. LDO3 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7:0	LDO3_VOUT	R/W	01011010	LDO3 output voltage setting from 1.2V to 3.7V with step 20mV. 00000000: 0V 00000001~00111100: 1.2V 00111101: 1.22V …… 10111000: 3.68V 10111001~11111111: 3.70V

RTC Initialization and Status Register (Address=30h)

7	6	5	4	3	2	1	0
RESERVED	INIT_F	ALARM_F	INITS	RESERVED	ALARM_EN	OPSEL	INIT
R - 00000000b							

Figure 89. RTC_ISR

Table 37. LDO3 Output Setting Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6	INIT_F	R	0	Initialization flag. When this bit is set to 1, the RTC is in initialization state, the Calendar registers can be updated. 0: Calendar register update is not allowed 1: Calendar register update is allowed
5	ALARM_F	R/W1C	0	Alarm flag indicating the date register matching the alarm register. Cleared after read. Automatically set to 1 when the date register matches the alarm register.

				0: No alarm happened 1: Alarm happened
4	INITS	R	0	Initialization status 0: Date not initialized 1: Date initialized
3	Reserved	R	0	Reserved
2	ALARM_EN	R/W	0	Enable alarm function 0: disabled, the ALARM register update is allowed 1: enabled, the ALARM register update is not allowed
1	OPSEL	R/W	0	Alarm output signal polarity 0: active low when ALARM_F is set 1: active high when ALARM_F is set
0	INIT	R/W	0	Initialization 0: Normal mode 1: Initialization mode

RTC Year Register (Address=31h)

7	6	5	4	3	2	1	0
YEAR_T				YEAR_U			
R - 00000000b							

Figure 90. RTC_YEAR

Table 38. RTC Year Register Field Description

Bit	Field	Type	Reset	Description
7:4	YEAR_T	R/W	0000	Ten digit of year in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9
3:0	YEAR_U	R/W	0000	Unit digit of year in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Month Register (Address=32h)

7	6	5	4	3	2	1	0

RESERVED	MONTH_T	MONTH_U
R - 00000000b		

Figure 91. RTC_MONTH

Table 39. RTC Month Register Field Description

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000	Reserved
4	MONTH_T	R/W	0	Ten digit of month in BCD format 0: 0 1: 1
3:0	MONTH_U	R/W	0000	Unit digit of month in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Day Register (Address=33h)

7	6	5	4	3	2	1	0
RESERVED		DAY_T		DAY_U			
R - 00000000b							

Figure 92. RTC_DAY

Table 40. RTC Day Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5:4	DAY_T	R/W	00	Ten digit of day in BCD format 00: 0 01: 1 10: 2 11: 3
3:0	DAY_U	R/W	0000	Unit digit of day in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Hour Register (Address=34h)

7	6	5	4	3	2	1	0
RESERVED		HOUR_T		HOUR_U			

R - 00000000b

Figure 93. RTC_HOUR

Table 41. RTC Hour Register Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5:4	HOUR_T	R/W	00	Ten digit of hour in BCD format 00: 0 01: 1 10: 2
3:0	HOUR_U	R/W	0000	Unit digit of hour in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Minute Register (Address=35h)

7	6	5	4	3	2	1	0
RESERVED	MIN_T			MIN_U			
R - 00000000b							

Figure 94. RTC_MIN

Table 42. RTC Minute Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	MIN_T	R/W	000	Ten digit of minute in BCD format 000: 0 001: 1 010: 2 011: 3 100: 4 101: 5
3:0	MIN_U	R/W	0000	Unit digit of minute in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Second Register (Address=36h)

7	6	5	4	3	2	1	0
RESERVED	SEC_T			SECOND_U			
R - 00000000b							

Figure 95. RTC_SEC

Table 43. RTC Second Register Field Description

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6:4	SEC_T	R/W	000	Ten digit of second in BCD format 000: 0 001: 1 010: 2 011: 3 100: 4 101: 5
3:0	SEC_U	R/W	0000	Unit digit of second in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Alarm Day Register (Address=37h)

7	6	5	4	3	2	1	0
DATE_MASK	RESERVED	ALARM_DAY_T		ALARM_DAY_U			
R - 00000000b							

Figure 96. RTC_ALARM_DAY

Table 44. RTC Alarm Day Register Field Description

Bit	Field	Type	Reset	Description
7	DAY_MASK	R/W	0	Alarm mask for day 0: No mask for day 1: Mask for day
6	RESERVED	R	0	Reserved
5:4	ALARM_DAY_T	R/W	00	Ten digit of day in BCD format 00: 0 01: 1

				10: 2 11: 3
3:0	ALARM_DAY_U	R/W	0000	Unit digit of day in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Alarm Hour Register (Address=38h)

7	6	5	4	3	2	1	0
HOUR_MASK	RESERVED	ALARM_HOUR_T		ALARM_HOUR_U			
R - 00000000b							

Figure 97. RTC_ALARM_HOUR

Table 45. RTC Alarm Date Register Field Description

Bit	Field	Type	Reset	Description
7	HOUR_MASK	R/W	0	Alarm mask for hour 0: No mask for hour 1: Mask for hour
6	RESERVED	R	0	Reserved
5:4	ALARM_HOUR_T	R/W	00	Ten digit of hour in BCD format 00: 0 01: 1 10: 2
3:0	ALARM_HOUR_U	R/W	0000	Unit digit of hour in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Alarm Minute Register (Address=39h)

7	6	5	4	3	2	1	0
MIN_MASK	ALARM_MIN_T			ALARM_MIN_U			
R - 00000000b							

Figure 98. RTC_ALARM_MIN

Table 46. RTC Alarm Minute Register Field Description

Bit	Field	Type	Reset	Description
7	MIN_MASK	R	0	Alarm mask for minute 0: No mask for minute 1: Mask for minute
6:4	ALARM_MIN_T	R/W	000	Ten digit of minute in BCD format 000: 0 001: 1 010: 2 011: 3 100: 4 101: 5
3:0	ALARM_MIN_U	R/W	0000	Unit digit of minute in BCD format 0000: 0 0001: 1 0010: 2 …… 1001: 9

RTC Alarm Second Register (Address=3Ah)

7	6	5	4	3	2	1	0
SEC_MASK	ALARM_SEC_T			ALARM_SEC_U			
R - 00000000b							

Figure 99. RTC_ALARM_SEC

Table 47. RTC Second Register Field Description

Bit	Field	Type	Reset	Description
7	SEC_MASK	R	0	Alarm mask for second 0: No mask for second 1: Mask for second
6:4	ALARM_SEC_T	R/W	000	Ten digit of second in BCD format 000: 0 001: 1 010: 2 011: 3 100: 4 101: 5
3:0	ALARM_SEC_U	R/W	0000	Unit digit of second in BCD format 0000: 0

				0001: 1 0010: 2 …… 1001: 9

Application and Implementation

Application Information

The HPU3501 is designed to support Horizon X5 SoC.

Typical Application

Work with X5 SoC

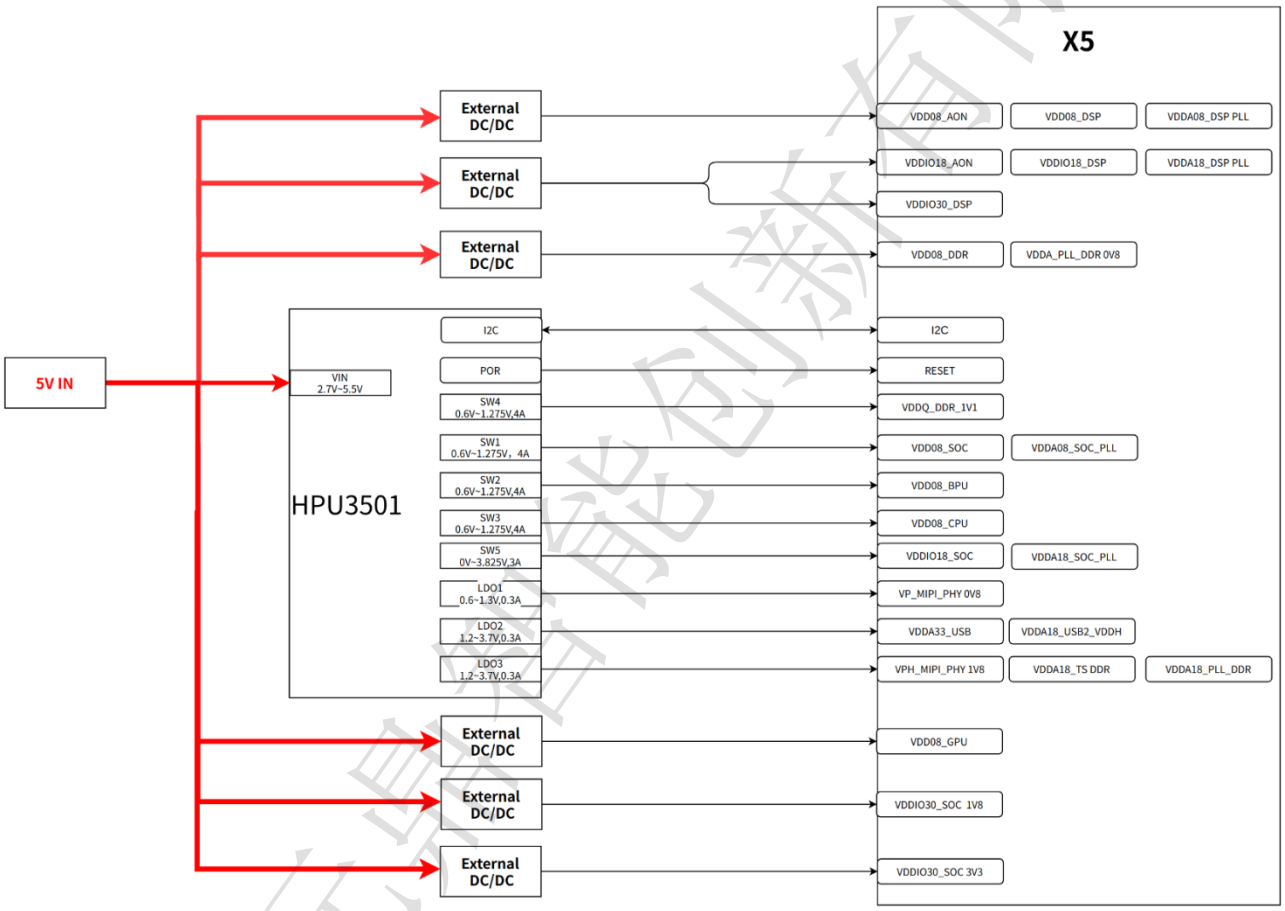


Figure 100. Typical Application with X5 SoC

Layout

Layout Guideline

It is important to have a good PCB layout for high frequency and large switching current PMIC of the HPU3501. Proper design and layout can get good performance of the output power supplies. Layout affects noise generation and pickup, and also can cause an unexpected abnormal status of the power supply. With a range of output currents from milliamps to 4 A per buck converter rail, following PCB layout should be used as a reference to ensure the device works stable and maintains proper output voltage and current regulation.

1. Place the input ceramic capacitor as close as possible to the PVINx pin and the PGND pin. Route the PVINx trace wide and thick to avoid voltage drops caused by the trace resistance. The trace between the positive node of the input capacitor and the PVINx pins of the HPU3501, as well as the trace between the negative node of the input capacitor and the PGND pin of the HPU3501 must be kept as short as possible. The parasitic inductance of the loop from PVINx to the input capacitor and back to the PGND pin must be kept as tiny as possible for proper device operation. A large ground plane should be connected to the PGND pin through multi-vias underneath the package. This ground plane can reduce the parasitic inductance and improve the thermal dissipation.
2. The output filter, consisting of the inductor and the output capacitor, converts the switching voltage at the SWx pin to the regulated DC output voltage. The output filter must be placed as close as possible to the device keeping the switch node small, for better EMI behavior. The traces between the output capacitor to the load must be wide and thick to avoid the efficiency loss and the voltage drop due to the high load current.
3. Connect the AGND to the PGND directly to avoid any large transient current going through the trace between the AGND pin and PGND pin. Place the decoupling capacitor as close as possible between the AVIN and AGND pins.
4. When using remote voltage sensing by connecting the VOUTx pins to the respective sense pins on the load, the sense lines are sensitive to noise. The sense lines must be kept away from noisy signals as switch nodes and PVINx, as well as the digital signals such as I^2C. Avoid bot capacitive and inductive coupling by making the sense lines short and direct. Isolate the sense lines by a power or ground plane if possible.

Layout Example

This PCB layout example uses four-layer PCB. The components are on the top layer. The second layer is the ground plane. The PMIC's PGND pin underneath the package is connected to the ground plane with 16 vias.

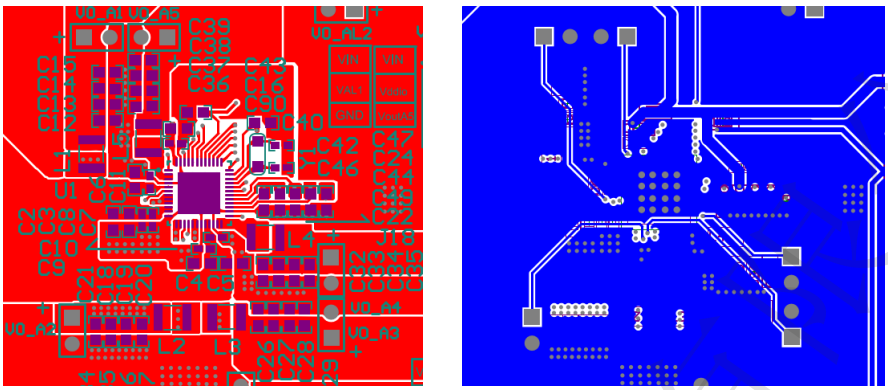
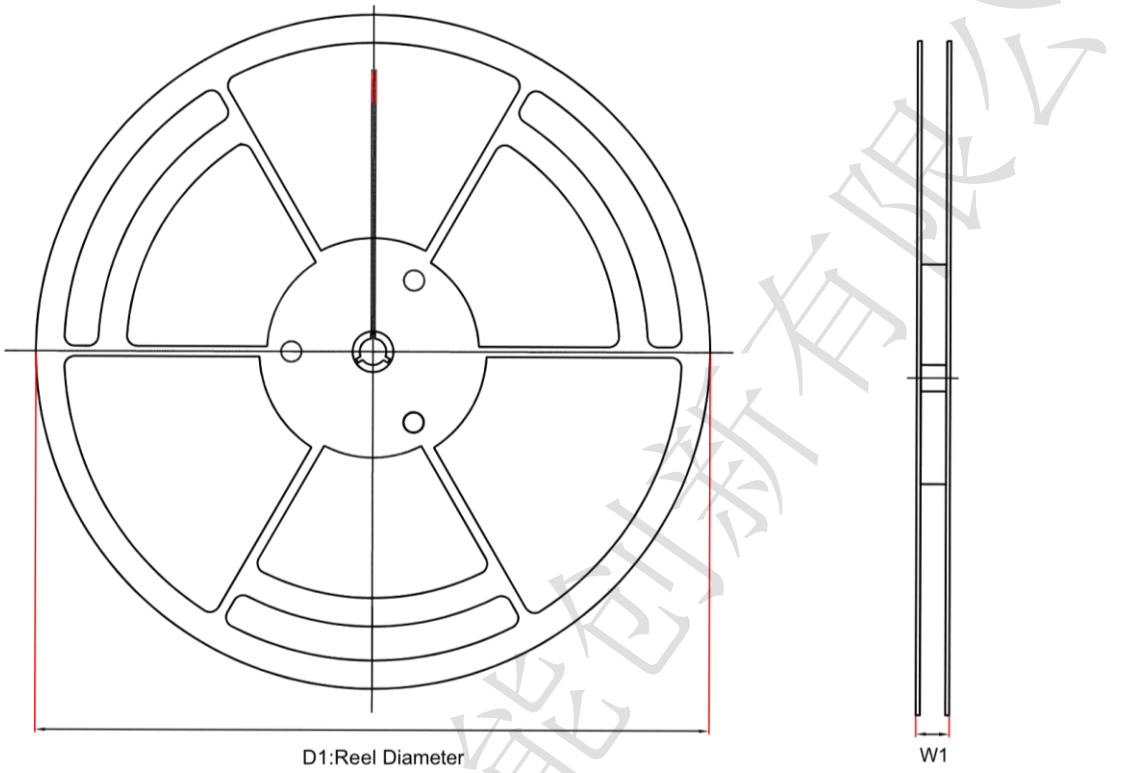


Figure 101. Layout Example (Top Layer and Bottom Layer)

Tape and Reel Information

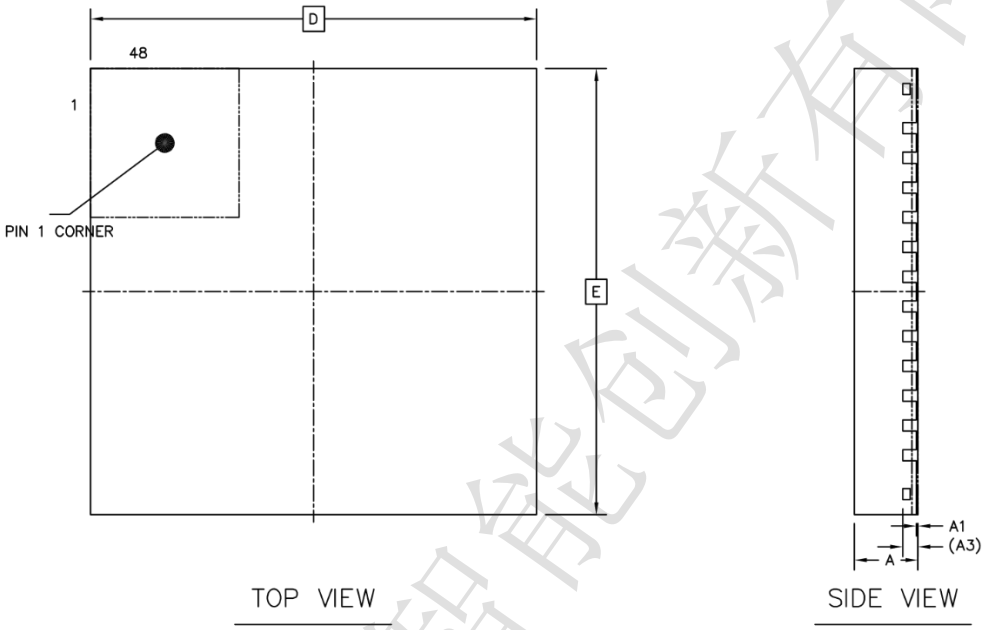


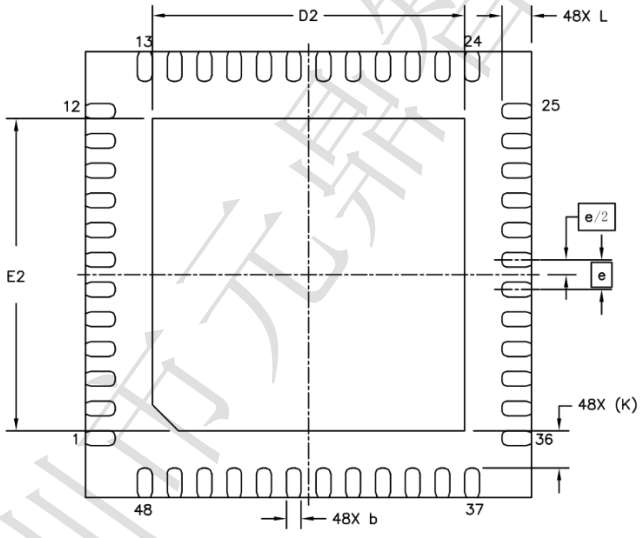
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
HPU3501A10CQNXMA	QFN6x6-48	330	21	6.3	6.3	1.1	12	16	Q1
HPU3501A10CQNXMB	QFN6x6-48	330	21	6.3	6.3	1.1	12	16	Q1
HPU3501A13CQNXMA	QFN6x6-48	330	21	6.3	6.3	1.1	12	16	Q1
HPU3501A13CQNXMB	QFN6x6-48	330	21	6.3	6.3	1.1	12	16	Q1

Package Outline Dimensions

QFN 6x6-48

Package Outline Dimensions FS5(QFN6X6-48-A)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
A3	0.203 REF		0.008 REF	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
e	0.400 BSC		0.016 BSC	
L	0.300	0.500	0.012	0.020
D2	4.100	4.300	0.161	0.169
E2	4.100	4.300	0.161	0.169
K	0.500 REF		0.020 REF	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	RoHS Compatible
HPU3501A10CQNXMA	-40ºC - 125ºC	QFN6x6-48	3501A	MSL3	3150	Green
HPU3501A10CQNXMB	-40ºC - 125ºC	QFN6x6-48	3501A	MSL3	3150	Green
HPU3501A13CQNXMA	-40ºC - 125ºC	QFN6x6-48	3501A	MSL3	3150	Green
HPU3501A13CQNXMB	-40ºC - 125ºC	QFN6x6-48	3501A	MSL3	3150	Green

Green: "Green" means RoHS compatible and free of halogen substances.

Part Number Naming Rule