Sunrise 5 (X5)

Datasheet

Rev. 1.0

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
0.8	2024-01-20	Initial draft.
0.81	2024-02-21	Minor update
0.82	2024-02-27	Minor update
0.83	2024-03-25	Minor update
0.84	2024-04-25	Update the strap pin description
0.85	2024-06-16	Modify the PIN name of the chip to keep consistent with the software.
0.86	2024-08-21	Update the description of CPU frequency for X5H Fix a typo in the description of 2D engine performance Update the part number and description for X5H
1.0	2024-08-25	Update for RDK release Add the min and max voltage of each power domain Add the Electrical Specification of USB3.0 and USB2.0

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1 Overview

1.1 General Product Description

The Sunrise 5(X5) is a highly-integrated, high-performance and power-efficient artificial intelligence System-on-Chip (SoC) powered by D-Robotics. Based on the Single-core BPU with Bayers-architecture, X5 support real-time pixel-level video segmentation, structured video analysis and attention-based vision perception. Video streams(max. resolution up to 16Mpixel@30fps)inputs from MIPI CSI -2 Receivers (Rx) are processed by the image signal processing(ISP) and video processing units before being passed to BPU for artificial intelligence inference computing such as video object detection, sentiment segmentation, scene parsing, etc.

The X5 SoC also integrates an Octa-core Cortex A55 CPU, one HiFi5 DSP which can support voice wakeup , an image signal processing (ISP) unit for wide/high dynamic range (WDR or HDR) and noise reduction (3DNR) in the camera input images processing, H.265/H.264/MJPEG video codecs, a 3D GPU supporting OpenGL ES 3.1/3.0 /2.0/1.1, a DDR controller for LPDDR4/LPDDR4X, and other on-chip modules and rich off-chip sensors connectivity peripheral interfaces, which enable greater flexibility and faster delivery for customers to implement their own products for different kinds of targeted applications.

Except of video/image artificial intelligence detections, segmentation and recognitions, the X5 BPU can also support intelligent speech algorithms like keyword spotting, speech recognition, text-to-speech and so on to enable more Robotics Applications.

The advanced toolkit from D-Robotics provides a Linux-based training framework and development environment to assist customers in rapid application implementation and deployment. The BPU toolkit also support floating point neural network model to fixed point neural network model conversion.

1.2 Chip Block Diagram

Figure 1-1 shows the chip-level functional block diagram of the X5, providing a view of the major subsystems (CPU subsystem, BPU subsystem, DDR subsystem, Camera subsystem, Video subsystem, GPU subsystem, DSP subsystem, peripheral interface, memories, etc.) and logical connectivity.

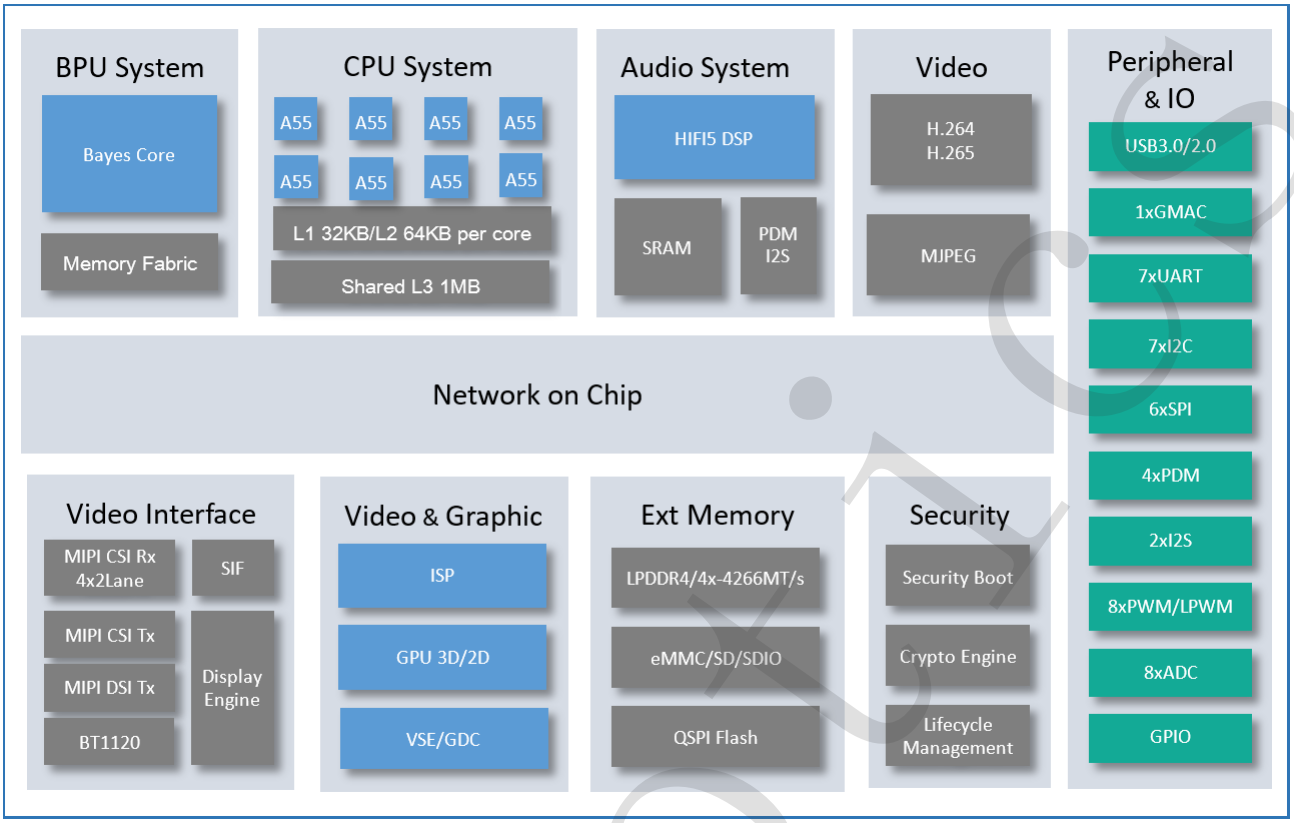


Figure 1-1 X5 Chip Block Diagram

1.3 Features

1.3.1 General

- TSMC 12nm FFC (FinFET Compact Technology) Process
- FCCSP563 Package with 0.65 mm ball pitch, 16 mm x 16 mm body size
- Ambient operating temperature: -25°C ~ +85°C
- Designed for Robotics, specifically for Robot vacuum cleaners, Robot lawn mowers, Home Companion Robots, etc.

1.3.2 CPU

- Octa-core Arm® Cortex® A55
- Each core with 32 KB/32 KB L1 I/D cache and 64 KB L2 cache
- 1MB L3 cache shared by 8x cores
- Support FPU and NEON
- Separate VDD_CPU voltage domain
- Typical Operating Frequency
  - X5H : 1.8GHz@1.0V
  - X5M : 1.5GHz@0.85V
- Include the Advanced SIMD and floating-point unit in each core

- Support DVFS (Dynamic Voltage and Frequency Scaling)
- Integrated GIC-600 interrupt controller
- CoreSight® debug and trace, including self-hosted debug

1.3.3 BPU

- Bayers-architecture BPU capable of 10 TOPS computing performance on deep neural network inferences
- Separate power domain for VDD_BPU
- Typical operating frequency: 1.0GHz
- Support DVFS (Dynamic Voltage and Frequency Scaling)
- Advanced toolkit supported by D-Robotics

1.3.4 Audio DSP

A minimum system for audio processing with independent power supply

- Cadence HiFi 5 Audio DSP for Audio processing
  - Maximum Operating Frequency: 812MHz
  - 32KB instruction/ 48KB data L1 cache
  - 64KB instruction/ 128KB data RAM
  - Internal watch dog
- Support Voice Wake-up Processing in lite sleep mode with total 1.5MB shared SRAM
- Multichannel AXI DMA for audio data transmission
- 4-counter Timer
- CRM with one audio PLL
- A simple set of peripheral interfaces meets the requirements of the minimum speech reception and processing system, and they can be shared with CPU
  - 1x SPI, up to 50Mbps in master mode
  - 1x I2C which Support SMBUS, up to 400KHz
  - 2x full-duplex I2S, up to 40Mbps in master mode
    - Support both master and slave modes
    - RX Support 1/2/4/8/16-channel audio input
    - TX Support 1/2-channel audio output
    - Support 8/16/32/44.1/48/64 KHz sample rate
  - 1x UART with 9600 to 4M baud rate
  - 8x channel PDM

1.3.5 Memory

- **Internal memory**
  - BootROM

- Support system boot from the following device:
  - QSPI Flash interface
  - Nand Flash
  - Nor Flash
  - eMMC interface
  - SDMMC interface
- Support system code download by the following interface:
  - USB3.0 interface (Device mode)
  - USB2.0 interface (Device mode)
- Support security boot

- 128KB AON_SRAM in the voltage domain of VDD_AON for low power application
- 1.5MB SYS_SRAM (SYS_SRAM0 and SYS_SRAM1) in the voltage domain of VDD_DSP for Voice Wake-up Processing or Image Signal Processing

External memory

- LPDDR4/LPDDR4x
  - Compatible with JEDEC standards
  - Support x32 off-chip LPDDR4/LPDDR4X DRAM
  - Up to 8 GB capacity supported
  - Support maximum 2 ranks
  - Separate VDD_DDR voltage domain for DDR Controller and DDR PHY
  - Support LPDDR4/LPDDR4X maximum speed up to 4266MT/s
  - Support DFS (Dynamic Frequency Scaling)
  - Embedded performance monitor measuring bandwidth, latency, and other metrics on internal bus and DDR Controller, used for debug and performance optimization
- eMMC
  - Support eMMC5.1 protocols up to HS200(maximum data rate 192 MB/s)
  - Support 1/4/8 bit data interface, only Support 1.8V SDIO
  - Support legacy, high-speed SDR, HS200 speed modes
- SD-Card
  - Support SD memory and compliant with SD HCI specification
  - Support Default Speed (DS), high-speed (HS), SDR12, SDR25, SDR50 and SDR104 speed modes
  - Support 1.8/3.3v SDIO
  - Support UHS-I mode
  - Support SDIO read wait
  - Support SDIO card interrupts in both 1-bit and 4-bit modes
  - Wake up on card interrupt
- QSPI Nor/Nand Flash

- Support 1/2/4 wire mode, up to 100MHz
- Enhanced Quad SPI features:
  - Programmable address, instruction, wait cycles, and data frame size
  - Clock stretching support

1.3.6 Video Input Interface

- MIPI CSI RX
  - Support MIPI CSI video input:
    - Compatible with the MIPI Alliance Interface specification v2.1
    - Up to 8 data lanes, 2.5Gbps maximum data rate per lane
    - Support MIPI-HS, MIPI-LP mode
    - Each 4 data lanes support two modes
      - One interface with 1 clock lane and 4 data lanes, support up to 2 virtual channels
      - Two interface, each with 1 clock lane and 2 data lanes, support up to 4 virtual channels
    - Up to 5472 x 3076 pixels@30fps video input with limited video h-blank duration
    - Support RAW 8-/10-/12-/14-/16-bit format and 8-/10-bit YUV 422 format
  - Support video in-to-out bypass, MIPI CSI RX to MIPI CSI TX back-to-back bypass

1.3.7 Image Signal Processing (ISP)

- Built-in Image Signal Processor (ISP) supporting RAW to YUV conversion
- Maximum processing ability: 3840x2160@60fps
  - Hardware mode: 4096x3072
  - Software mode(tile mode) : 5472x3076
- Support High Dynamic Range (HDR) sensors:
  - Max 20-bit HDR Processing
  - Support Digital Overlap (DOL2) HDR sensor
  - Support linearized HDR sensors
  - Support native (on sensor) companded HDR sensors
- Support Auto-Exposure, Auto-White balance, and Auto-Focus (3A) histogram statistics
- Support Lens Shading Correction
- Support Defect Pixel Correction (DPC)
- Support Spatial Noise Reduction(2DNR)
- Support Temporal Noise Reduction (3DNR)
- Support Color Noise Reduction
- Support RGB Sharpening and Edge Enhancement
- Support Gamma Correction
- Black level Compensation

- Sensor Linear Correction
- Green Equalization
- Digital Gain
- Enhanced Color Interpolation (Bayer De-mosaic filter)
- Chromatic Aberration Correction (CAC)
- Color Correction (Xtalk) Matrix (CCM)
- Color Space Conversion (CSM)
- Anti-flicker
- Color Processing: Contrast, Saturation, Brightness, Hue (CPROC)
- Sharpen/Blur Filter
- RGB-IR 4x4 pattern
- Support WDR combining global and local tone mapping
- PDAF support
- ISP tuning tool on the PC

1.3.8 Video Scaler Engine (VSE)

- Supports input data format YUV422sp, YUV422 interleave and YUV420sp
- Supports different output formats: YUV444, YUV422, YUV420, RGB888
- Support 8-bit component data as input and output data format
- Maximum processing ability: 3840x2160@60fps
- 1 up-scaler integrated
  - Maximum upscale ratio is 4X, such as 4x1, 2x2, 1x4, etc.
  - Maximum output image size is 3840x2160
- 5 down-scaler integrated
  - 1x scaler Support that the maximum output image size is 3840x2160
  - 2x scalers support that the maximum output image size is 1920x1080
  - 2x scalers support that the maximum output image size is 1280x720
  - Down scale minimum resolution to 64x64, and support any downscale factor
- Each scaler Support frame rate control
- Each scaler Support OSD
- Each OSD Support up to 4 overlay regions (4 ROI do not overlap in vertical direction) and 8 histogram statistics region
- Each scaler engine can choose one of three source data (1 stream from ISP, 1 DMA and 1 TPG) as input, and the TPG has a higher priority than stream 0 input
- Support input crop Separate scaling in horizontal and vertical directions, and for chrominance and luminance components
- Shadow registers for on-the-fly reprogramming of control registers

1.3.9 Geometry Distortion Correction (GDC)

- Support input data formats
  - RGB and YUV Color Formats
  - 8-bit Data Width
  - 4:2:0 and 4:4:4 Samplings
- Maximum resolution is up to 4096 x 2160@60fps
- Support Lens GDC and Fisheye correction
- Support Transformations, Panoramic, Cylindrical, Stereographic, and Digital PTZ (Pan, Tilt, and Zoom control)
- Support Image storing formats
  - Planar (YV12)
  - Semi Planar (NV12, Only for YUV 4:2:0)
  - GDC transforms the image by applying pre-defined coordinate mapping

1.3.10 Video Codec

- H265/HEVC codec supports HEVC Main and Main Still Picture Profile @L5.1 High tier
- H264/AVC codec supports Baseline/Constrained Baseline/Main/High Profiles Level @L5.2
- Supports YUV420 input
- Maximum resolution is 8192x4096 and performance is not considered
- Maximum processing ability:
  - 3840x2160@60fps for encoder
  - 3840x2160@60fps for decoder
  - 3840x2160@30fps if encoder and decoder work simultaneously
- Adjustable bitrate for performance consideration, support CBR/VBR/AVBR
- Adjustable fps for performance consideration
- Supports I/P frame, do NOT support B frame
- H.264 supports SVC-T Encoding

1.3.11 JPEG Codec

- Support JPEG baseline/extended sequential and M-JPEG decoding and encoding
- Support YUV444/YUV422/YUV420/YUV400/YUV440 input and output format
- Support max resolution of encode/decode is 32768x32768
- Maximum processing ability:
  - 3840x2160@60fps for encoder
  - 3840x2160@60fps for decoder
  - 3840x2160@30fps if encoder and decoder co-work simultaneously
- Minimum encoding size is 16x16 pixels

1.3.12 Graphics Engine

- 3D GPU
  - Support 32GFLOPs under 1.0GHz engine clock
  - API Support Feature
    - OpenGL ES 3.1/ 3.0/ 2.0/1.1
    - OpenCL 1.1/1.2/3.0
    - DirectX 11
    - Vulkan 1.0/1.2
  - Dynamic Voltage and Frequency Scaling(DVFS) based on current load
  - Support 3D Composition process
  - Support graphic resolving and fast clearing
- 2D GPU
  - The capability of 2D graphic processing is up to 750M pixel/s
  - Support more than 8 layers of overlay
  - Output format support YUV422/YUV420
  - Support 2D Graphics API
  - Composition Processing Core Module Features
    - Bit Blit
    - Stretch Blit
    - Rectangle fill and clear
    - One Pass Filter Blit
    - Alpha blending, including Java 2 Porter-Duff compositing blending rules
    - 32K x 32K coordinate system
    - 90/180/270 degree rotation, clockwise and counter clockwise
    - Flip and mirror operation
    - Source, pattern and destination ROP support, in which, pattern support is optional
    - Clipping
  - Support Multi Source Blending

1.3.13 Display interface

- Display interface
  - Support MIPI DSI interface
  - Support BT1120 interface
- MIPI DSI TX interface
  - Compatible with MIPI Alliance Interface specification v1.2
  - Support 1 clock lane and up to 4 data lanes, up to 2.5 Gbps per lane

- Support output format16/18/24-bit RGB and YUV422
- Up to 2560x1440@60fps video output

■ BT1120 interface

- Supports BT1120 video display output:
  - Output pixel data width is 16bit. Support pixel clock output DDR or SDR mode
  - Support up to 3840x2160@30fps YUV422 resolution output, output clock rate is up to 148.5MHz
  - Support progress mode and interleaved mode
  - Support input video format:
    - 8-bit YUV 4:2:2, 8-bit YUV 4:2:0
    - Semi-planer feature to store in Y and UV memory buffers for YUV422,YUV420
    - Support YUV422 packed mode store in memory
    - Support offline mode which read pixel data from DRAM or online mode that receive data from Display Process Engine

■ Display Process Engine

- Support parallel RGB video display output, maximum resolution is up to 2560x1440@60fps in linear mode
- Support input data formats such as ARGB8888, ARGB1555, RGB565, ARGB4444, A8RGB565, RGB888,NV12 in linear mode; or ARGB8888 and YUY2, NV12 in tiled mode
- One cursor layer, and cursor size is 32x32 pixels
- Cursor format: ARGB8888 and masked formats
- Support three layers, maximum size is 2560×1440
  - One layer is video/graphic layer,
  - the other two are overlay 0 and overlay 1
- Support swizzle and color keying
- The display controller supports 180-degree rotation or flip (flip x/flip y/flip xy) at the video/graphic and overlay layers
- Only the video/graphic and overlay 0 layers support Programmable color space conversion
- Post-processing for pixel composition: Alpha blending; Gamma correction with three separate lookup tables; Dither with one lookup table
- Power management with clock gating for RAM and video/graphic and overlay layers
- Video timing generation with HSYNC, VSYNC, Data Enable (DE) signals Programmable timings

1.3.14 Peripheral Interfaces

■ USB 3.0 Host/Device dual-role SuperSpeed interface

- Compatible with Universal Serial Bus Specification, Revision 3.0
- Support SuperSpeed (SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)

- Support PIPE3 PHY (125/250/500 MHz)
- Keep-Alive feature in LS mode and (micro-)SOFs in HS/FS modes
- Hardware controlled USB bus level and packet level error handling

■ USB 2.0 Host/Device dual-role interface

- Compatible with Universal Serial Bus Specification, Revision 2.0
- Support High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)
- Keep-Alive feature in LS mode and (micro-)SOFs in HS/FS modes
- Hardware controlled USB bus level and packet level error handling

■ MAC 10/100/1000 Ethernet Controller

- Support 10/100/1000 Mbps data transfer rates with the RGMII interfaces
- Support 10/100 Mbps data transfer rates with the RMII interfaces
- Support both full-duplex and half-duplex operation
- IEEE 802.3-2015 for Ethernet MAC, support Time-Sensitive Networking (TSN) traffic
- IEEE 1588-2008 for precision networked clock synchronization
- TCP/UDP offload is supported to reduce CPU loading

■ SDIO

- Support 2 SDIO interfaces
- Each SDIO interface support 4bits data bus widths
- Supports Default Speed (DS), high-speed (HS), SDR12, SDR25, SDR50 and SDR104 speed modes
- Support 1.8/3.3v SDIO

■ QSPI

- Support 1 QSPI interface
- Only supports master mode,
- Supports 1/2/4 wire mode, up to 100MHz
- Enhanced Quad SPI features:
  - Programmable address, instruction, wait cycles, and data frame size
  - Clock stretching support

■ SPI

- Support 6 SPI interfaces
- Support Master Mode and maximum data rate is 50Mbps
- Support Slave Mode and maximum data rate is 32Mbps

■ UART

- Support 7 UART interfaces
- UART0 and UART1 support auto flow control mode
- UART2/UART3/UART4/UART5/UART6 support standard mode
- Support Baud rate 9600/38400/57600/921600/115200/4M

■ I2C

- Support 7 I2C interfaces
- Only I2C4 support 3.4Mbps data rate
- I2C0/I2C1/I2C2/I2C3/I2C5/I2C6 only support up to 400KHz and sm_bus

■ PWM

- Support 8 PWM interfaces
- The frequency of the output waveform is programmable, and its range is from 0.05Hz to 1MHz
- Provides reference mode and output various duty-cycle waveform

■ LPWM

- Support 8 LPWM interfaces
- The frequency of the output pulse is programmable, and its range is from 1Hz to 1MHz
- The width of output pulse is programmable, and its range is from 1us to 4ms
- Support generating output pulse with multi-trigger source, such as PPS, EMAC and internal system timer

■ GPIO

- Support 7 group, total 129 GPIOs, which share the pins with other interfaces
- Support to be configured as interrupt sources or wakeup sources, triggered by positive, negative, or both edges

1.3.15 SoC Component

■ PMU(power management unit)

- 7 separate voltage domains (VDD_SOC /VDD_CPU /VDD_BPU /VDD_DSP /VDD_GPU /VDD_DDR /VDD_AON)
- 11 separate power domains, which can be power up/down by software based on different application scenes
  - 8x Cortex-A55 can be powered on/off separately
  - HiFi5 DSP/Video Codec/ISP can be powered on/off independently
- Multiple configurable work modes to save power
  - Supports deep sleep mode, in which only Always-On (AO) power domain active in sleep mode
  - Supports lite sleep mode, in which only the power domains of Always-On and HiFi5 DSP Subsystem are active for Voice Wake-up Processing

■ Timer

- 4x 32bits timers
- Support two operation modes: free-running and user-defined count
- Single interrupt for each timer

■ Watch Dog

- Programmable timeout range (period)
- Optional support for Pause mode with the use of external pause enable signal

- Prevention of accidental restart of the watchdog of counter

■ Mailbox

- One Mailbox in SoC to service Cortex-A55 and HiFi5 DSP communication
- Support security and non-security interrupt

■ DMAC

- 1x identical DMAC blocks supported for whole chip system
- Support Scatter Gather Mode, Buffer Descriptor and Buffer Chaining
- Support memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
- DMAC features:
  - 12 channels
  - 43 hardware request from peripherals

■ Trust Execution Environment (TEE) system

- Support TrustZone technology for the following components
- Cortex-A55, support security and non-security mode, switch by software
- Secure OTP, only can be accessed by Cortex-A55 in secure mode and secure key reader block
- DDR, AON_SRAM and SYS_SRAM can be accessed some part of space is addressed only in security mode, detailed size is software-programmable together with TZMA (TrustZone memory adapter)
- Support to manager the accessing address space of each master, such as Cortex-A55, BPU and GPU, by integrating a Memory Firewall Unit
- Cipher engine
  - Symmetric schemes, AES-ECB/CBC/CTR/OFB/XTS/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit).
  - Symmetric schemes, DES/TDES-ECB/CBC/CTR/OFB/CBC-MAC/CMAC
  - Support Digest schemes, SHA1/224/256/384/512
  - Asymmetric schemes, RSA 1024/2048/3072/4096/8192 and ECCP 192/224/256/384/512/521
  - Asymmetric scheme, SM2
  - Support HMAC-SHA1/224/256/384/512/SM3/MD5
  - Key ladder for key management.
  - Lifecycle management
  - True Random Number Generator (TRNG).
  - One Time Programming (OTP) and Physical Unclonable Function (PUF)
  - Support secure OTP
  - Support secure boot
  - Support secure debug
  - Support secure OS

1.3.16 Others

- ADC
  - 10-bit precision
  - Sampling rate up to 2MHz
  - Support 8 channels
  - INL < +/-2 LSB, DNL < +/-1.5 LSB
  - Support input voltage range: 0~1.8V
- Temperature Sensor
  - Support four embedded temperature sensor
  - Two programmable (rise or fall) HW alarms incorporating hysteresis for each sensor
  - -20~120℃ temperature range and 5℃ temperature resolution
- eFuse
  - Support 2 banks , total 2x1024bit
  - Support security eFuse bank and non-security eFuse bank
  - Support double bit for avoiding miswriting

1.4 Application Scenarios

The X5 is highly-integrated System-on-Chip (SoC) that provides powerful intelligent perception capabilities and controls peripheral devices to accomplish specific tasks for Robotics, specifically for Robot vacuum cleaners, Robot lawn mowers, Home Companion Robots, etc.

1.4.1 SoC as AP

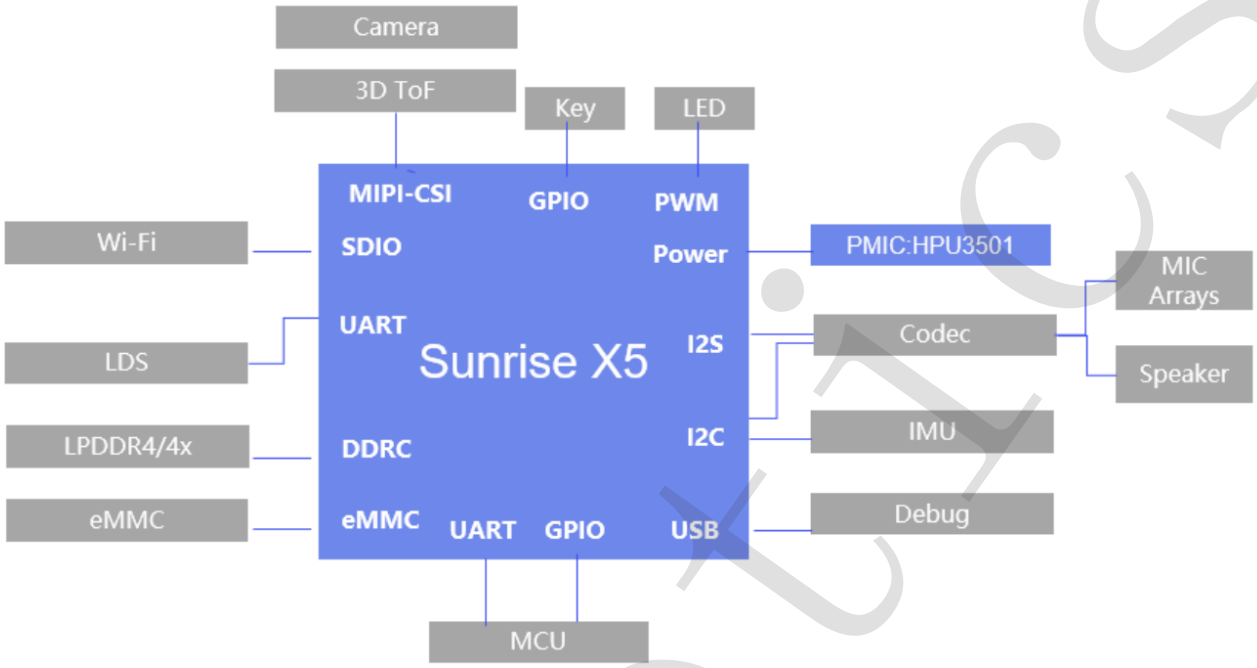


Figure 1-2 X5 Intelligent Robot Vacuum Cleaner Solution

In this scenario, a mono or two cameras (the MIPI or DVP but not both) are connected to the X5 directly. The data paths are detailed as follows:

1. The input video stream is received through the MIPI CSI RX, then processed by ISP, VSE, and GDC, and finally stored into the DDR in YUV420 semi-planar format
2. The BPU reads the images from the DDR and runs neural networks
3. The BPU finally writes the analysis results into the DDR
4. The CPU can implement further functions based on the intelligent analysis results
5. The Video codecs encodes the input video in DDR and writes the stream to DDR

1.5 Boot Mode

When power-up or wake-up from sleep mode, CPU starts executing the boot flow. The boot process can be divided into two stages, 1st boot and 2nd boot, which is introduced in the following sections.

1.5.1 1st Boot Mode

After the reset signal is released, CPU fetches its first instruction and starts the 1st boot stage. 1st boot mode includes on-chip ROM boot.

The procedure of the 1st boot stage is as follows:

1. Initialize the CPU itself and set up the running environment

2. Switch the CPU and internal bus to higher frequency to speed up
3. Initialize the necessary modules and peripherals
4. Obtain the selected 2nd boot mode and security boot enable from strap pins
5. Load 2nd boot firmware to on-chip SRAM
6. Jump to SRAM and execute the 2nd boot firmware

1.5.2 2nd Boot Mode

X5 support security boot and non-security boot in 2nd Boot Mode stage. And there are seven 2nd boot modes, including eMMC boot, QSPI NAND boot, QSPI NAND boot without MMU, QSPI NOR boot, USB2.0 boot, USB3.0 boot, and UART-XMODEM boot. 1st boot program obtains the selected 2nd boot mode from strap pins and 2nd boot firmware from off-chip storage devices (like eMMC, SPI NAND or SPI NOR) or from communication interfaces (like USB). Since the 2nd boot firmware is loaded from outside, it is programmable to minimize risks.

1.5.3 Strap Pin Definitions

The X5 selects BT1120 interface signals, which include BT1120_O_DATA15, BT1120_O_DATA14, BT1120_O_DATA1 ... BT1120_O_DATA0 and BT1120_O_PIXELCLK total 17 pins, as the strap pins. The strap pins are set to GPIO input mode at reset (RSTN = 0). When RSTN is released, the logic state of the strap pins will be latched into the PADC registers of the Display subsystem, whose address is 0x0_3E0A_00A4, and keep stable until the reset signal RSTN becomes active again. During the reset the logic state of the strap pin chooses boot branches and options, as shown in Table 1-1 below.

Table 1-1 Strap Pin Definition

Strap Pin	Share Pin	Default	Function
2NDBOOT_SEL	{BT1120_O_DATA2, BT1120_O_DATA1, BT1120_O_DATA0}	000	2NDBOOT_SEL: 000: 2NDBOOT UART 001: 2NDBOOT eMMC 010: 2NDBOOT USB2.0 DFU 011: 2NDBOOT SD Card 100: 2NDBOOT QSPI Nor Flash 101: 2NDBOOT QSPI Nand Flash 110: 2NDBOOT USB3.0 DFU 111: 2NDBOOT QSPI Nand Flash (disable mmu)
FORCE_SECURE_BOOT	BT1120_O_DATA3	0	If eFuse secure boot bit = 0, and FORCE_SECURE_BOOT: 1: X5 will be forced into secure boot (Secure_chip_1)

Strap Pin	Share Pin	Default	Function
			0: X5 will be into non-secure boot If eFuse secure boot bit = 1, X5 will be forced into secure boot
UART_BPS	BT1120_O_DATA4	0	UART_BPS: 0: 115200bps 1: 921600bps
RSVD	{BT1120_O_DATA6, BT1120_O_DATA5}	00	Reserved, these pins should be pull-down
DISABLE_LOG	BT1120_O_DATA7	0	DISABLE_LOG: 0: log print on during ROM boot 1: log print off during ROM boot
RSVD	{BT1120_O_DATA10, BT1120_O_DATA9, BT1120_O_DATA8}	000	Reserved, these pins should be pull-down
eMMC boot mode			
EMMC_CLK_LATCH	BT1120_O_DATA11	0	EMMC_CLK_LATCH: 0: eMMC clk falling latch data 1: eMMC clk rising latch data
EMMC_CLK_RATE	{BT1120_O_DATA13, BT1120_O_DATA12}	00	EMMC_CLK_RATE: 00: eMMC 12.5M 01: eMMC 25M 10: eMMC 33.3M 11: eMMC 50M
EMMC_DATA_WIDTH	BT1120_O_DATA14	0	EMMC_DATA_WIDTH: 0: 1 bit 1: 8 bits
EMMC_SECTION_SEL	{ BT1120_O_PIXELCLK, BT1120_O_DATA15}	00	EMMC_SECTION_SEL: 00: Read info from user data area 01: Read info from emmc boot partition 1 10: Read info from emmc boot partition 2 11: Disable MMU
QSPI Nand Flash boot mode			
NAND_PAGE_SIZE	BT1120_O_DATA11	0	NAND_PAGE_SIZE: 0: Nand flash 2k page size 1: Nand flash 4k page size.
NAND_CLK_RATE	{ BT1120_O_DATA13,	00	NAND_CLK_RATE:

Strap Pin	Share Pin	Default	Function
	BT1120_O_DATA12}		00: Nand 12.5M 01: Nand 33.3M 10: Nand 50M 11: Nand 100M
NAND_RESET	BT1120_O_DATA14	0	NAND_RESET: 0:before performing the operation, run reset command; 1: before performing the operation, close reset command.
NAND_NAND_RDID	BT1120_O_DATA15	0	NAND_NAND_RDID: 0: SPI NAND `s Read ID command comes with dummy byte 1: SPI NAND `s Read ID command does not take the dummy byte
NAND_2PLANES	BT1120_O_PIXELCLK	0	NAND_2PLANES: 0: The SPI NAND has only one plane, not need to set plane select 1: The SPI NAND has two planes, need to set plane select
QSPI Nor Flash boot mode			
NOR_ADDRESS_MODE	BT1120_O_DATA11	0	NOR_ADDRESS_MODE: 0: Nor flash 24bits address mode 1: Nor flash 32bits address mode
NOR_CLK_RATE	{BT1120_O_DATA13, BT1120_O_DATA12}	00	NOR_CLK_RATE: 00: spi flash 25M 01: spi flash 50M 10: spi flash 50M 11: spi flash 100M
NOR_RESET	BT1120_O_DATA14	0	NOR_RESET: 0: before performing the operation, run reset command 1: before performing the operation, close reset command
SWITCH MMU	{ BT1120_O_PIXELCLK, BT1120_O_DATA15}	00	SWITCH MMU: 11: Disable MMU Others : Enable MMU
SD Card boot mode			
SD_CLK_LATCH	BT1120_O_DATA11	0	0: SD clk falling latch data

Strap Pin	Share Pin	Default	Function
			1: SD clk rising latch data
SD_CLK_RATE	{ BT1120_O_DATA13, BT1120_O_DATA12}	00	SD_CLK_RATE: 00: SD 12.5M 01: SD 25M 10: SD 33.3M 11: SD 50M
SD_DATA_WIDTH	BT1120_O_DATA14	0	SD_DATA_WIDTH 0: 1 bit 1: 4 bits
SWITCH MMU	{ BT1120_O_PIXELCLK, BT1120_O_DATA15}	00	11: Disable MMU Others: Enable MMU

1.6 Memory Map

Table 1-2 shows part of memory map of the chip.

Table 1-2 Memory Map

Region	Start Address	End Address	Size
Boot ROM	0x0_0000_0000	0x0_0001_FFFF	128KB
RSVD	0x0_0002_0000	0x0_1FE7_FFFF	NA
SYS_SRAM0	0x0_1FE8_0000	0x0_1FEF_FFFF	512KB
SYS_SRAM1	0x0_1FF0_0000	0x0_1FFF_FFFF	1024KB
AON_SRAM	0x0_2000_0000	0x0_2001_FFFF	128KB
RSVD	0x0_2020_0000	0x0_7FFF_FFFF	NA
LPDDR4/LPDDR4x	0x0_8000_0000	0x2_7FFF_FFFF	8GB

2 Ordering Parts

The ordering part number is formed by a valid combination of the following:

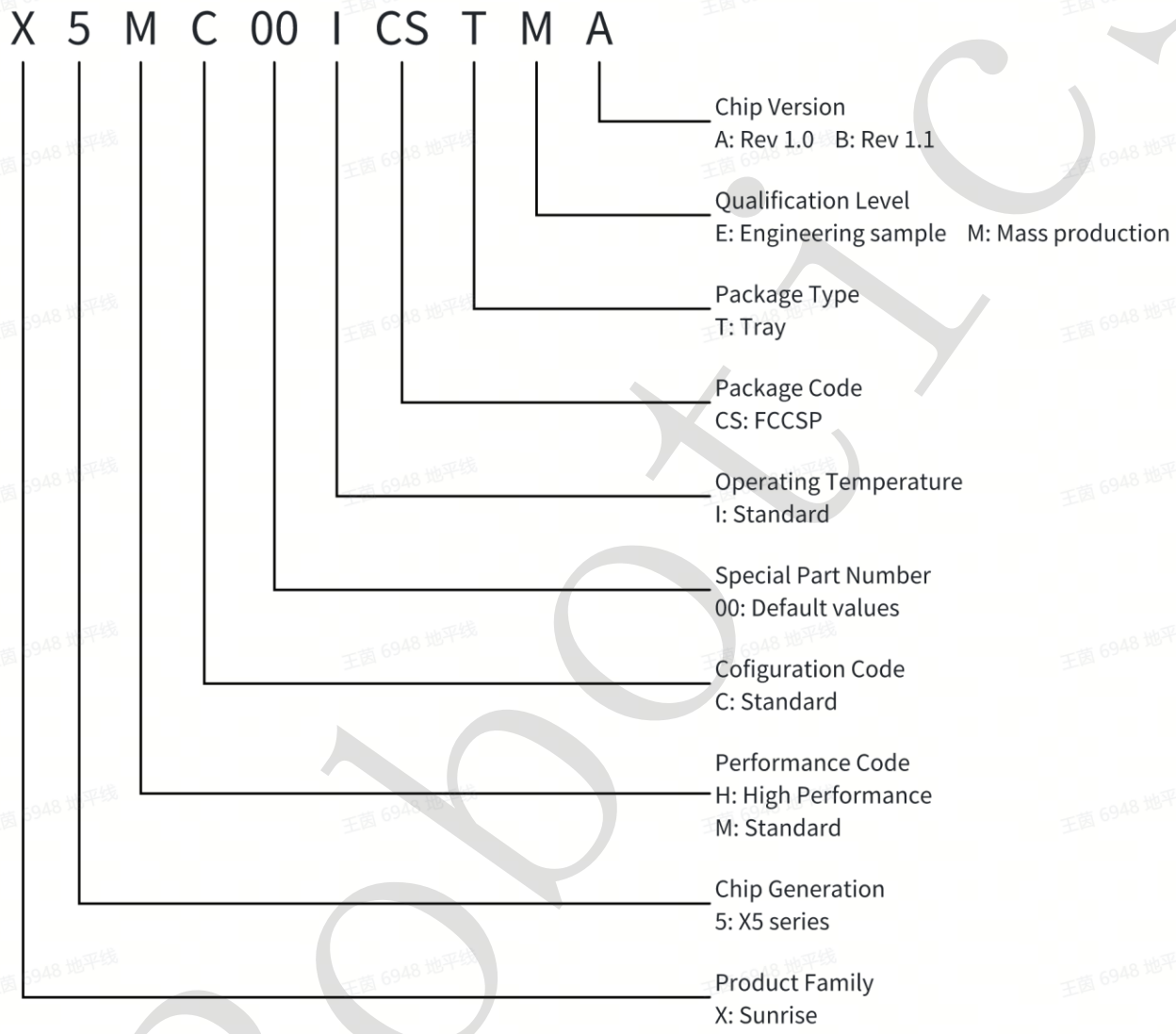


Figure 2-1 Part Number Definitions

3 Package Information

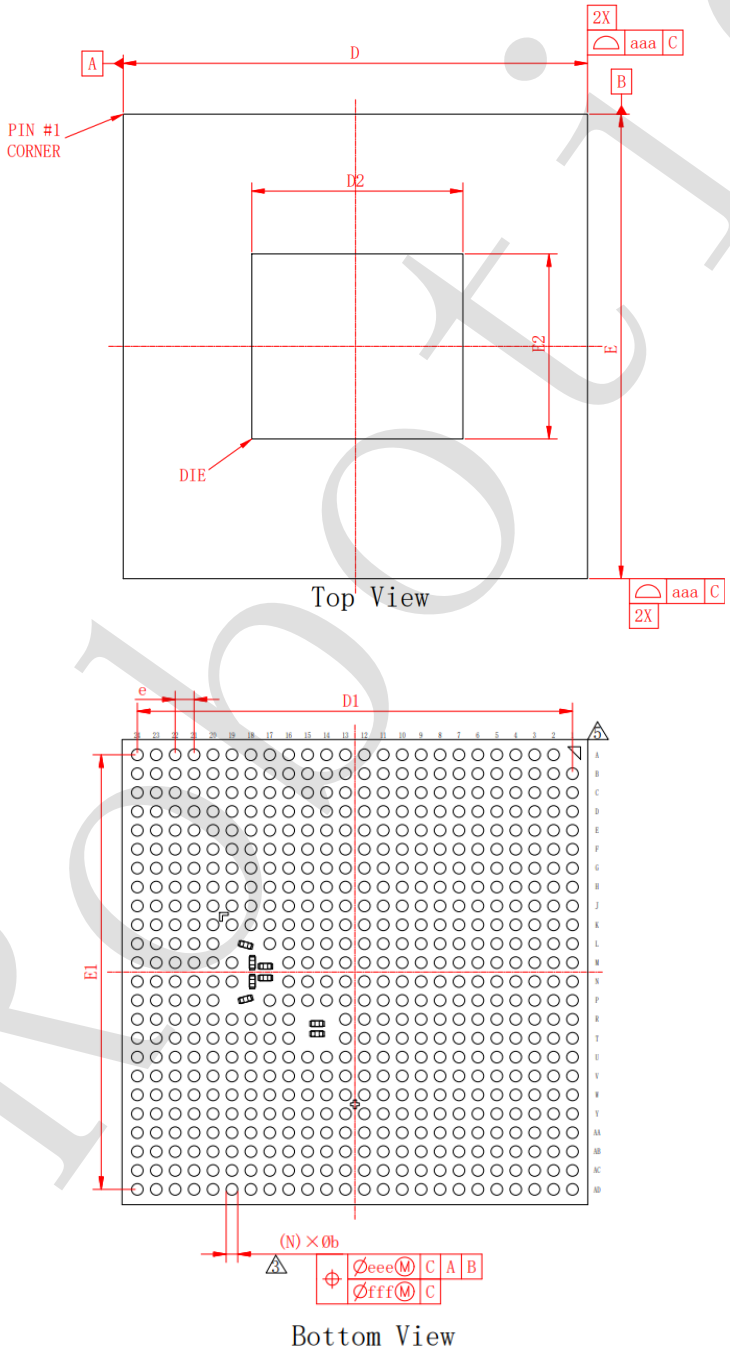
This chapter describes the hardware information in the following topics:

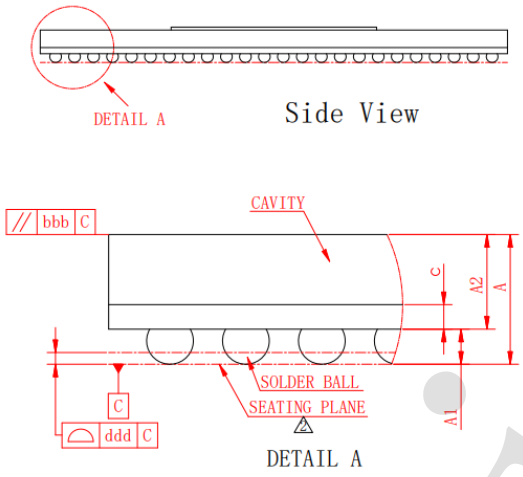
- Package and Ball Map
- Pin Description

3.1 Package and Ball Map

3.1.1 Package

The X5 uses the Flip-Chip Chip Scale Package (FCCSP) with 563 balls, 0.65 mm pitch and 16 mm x 16 mm size. Figure 3-1 shows the Package Outline Dimensions (POD) of the X5 FCCSP563



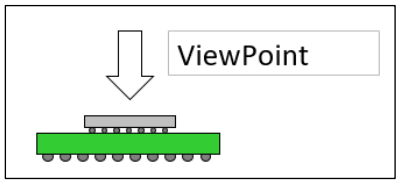


symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.010	1.110	1.210	0.040	0.044	0.048
A1	0.250	0.300	0.350	0.010	0.012	0.014
A2	0.740	0.810	0.880	0.029	0.032	0.035
c	0.170	0.210	0.250	0.007	0.008	0.010
D	15.900	16.000	16.100	0.626	0.630	0.634
E	15.900	16.000	16.100	0.626	0.630	0.634
D1	---	14.950	---	---	0.589	---
E1	---	14.950	---	---	0.589	---
D2	---	7.279	---	---	0.287	---
E2	---	6.375	---	---	0.251	---
e	---	0.650	---	---	0.026	---
b	0.350	0.400	0.450	0.014	0.016	0.018
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.100			0.004		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.400			0.016		
N	563			563		
MD/ME	24/24			24/24		

Figure 3-1 X5 FCCSP563 Package Outline

3.1.2 Ball Map

The FCCSP uses 563 (24 x 24) ball BGA with 13 blanks. Figure 3-2 to Figure 3-6 show the ball map for the X5.



Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	X	VSS	**USB3_RX0_P**	**USB3_TX0_P**	**USB3_REF_CLK_P**	**USB3_DP0**	USB2_VBUS0	**USB2_DP0**	HSIO_SDIO_DAT2	HSIO_SD_DAT2	HSIO_SD_CMD	HSIO_QSPI_DATA_3	HSIO_QSPI_SSN_0	HSIO_ENET_RXDV	HSIO_ENET_RXD_1	HSIO_ENET_RX_CLK	HSIO_ENET_RXD_0	HSIO_ENET_TXD_3	DRAM_BP_DB5	DRAM_BP_DB4	**DRAM_BP_DB10**	DRAM_BP_DB17	VSS	VSS	A
B	VSS	AON_TEST_MODE	**USB3_RX0_M**	**USB3_TX0_M**	**USB3_REF_CLK_M**	**USB3_DM0**	USB3_VBUS0	**USB2_DM0**	HSIO_SDIO_DAT3	HSIO_SD_DAT3	HSIO_SD_DAT1	HSIO_SD_SDCLK	VSS	HSIO_QSPI_DATA_0	HSIO_QSPI_SSN_1	VSS	HSIO_ENET_TXEN	HSIO_ENET_TX_CLK	DRAM_BP_DB7	VSS	**DRAM_BP_DB9**	DRAM_BP_DB19	DRAM_BP_DB18	VSS	B
C	AON_XTALI_24M	AON_XTALO_24M	VSS	EMMC_RST_N	EMMC_DAT7	VSS	USB3_RESREF	EMMC_CMD	VSS	HSIO_SDIO_DAT0	HSIO_SDIO_SDCLK	HSIO_SD_DAT0	HSIO_SD_WP	HSIO_QSPI_DATA_2	HSIO_QSPI_SCLK	HSIO_ENET_RXD_2	HSIO_ENET_TXD_1	HSIO_ENET_TXD_0	DRAM_BP_DB6	DRAM_BP_DB8	VSS	DRAM_BP_DB1	**DRAM_BP_DB21**	**DRAM_BP_DB22**	C
D	AON_ENV_VDD	AON_PMIC_EN	AON_HW_RESETN	AON_CLK_32K	EMMC_DAT6	EMMC_DAT5	EMMC_DAT4	EMMC_DAT1	USB2_TXRTUNE	HSIO_SDIO_DAT1	HSIO_SDIO_WP	VSS	HSIO_SD_CDN	HSIO_QSPI_DATA_1	VSS	HSIO_EPHY_CLK	HSIO_ENET_TXD_2	HSIO_ENET_MDIO	VSS	DRAM_BP_DB3	DRAM_BP_DB0	VSS	DRAM_BP_DB20	DRAM_BP_DB15	D
E	AON_ENV_CNN0	AON_ENV_CNN1	AON_RESETN_OUT	AON_IRQ_OUT	AON_GPIO0_PIN00	EMMC_DAT3	EMMC_DAT2	EMMC_DAT0	EMMC_SDCLK	HSIO_SDIO_CDN	HSIO_SDIO_CMD	VDDPST33_EMMC	AVDD33_USB2_VDD330	VDDPST33_HS_SDIO	VDDPST33_SD	HSIO_ENET_RXD_3	HSIO_ENET_MDC	VDDPST18_QSPI	VSS	DRAM_BP_DB2	VDDQ_DDR	DRAM_BP_DB14	VSS	E
F	AON_GPIO0_PIN01	AON_GPIO0_PIN02	VSS	AON_GPIO0_PIN03	AON_GPIO0_PIN04	VSS	VSS	AVDD33_USB3	VSS	DVDD08_USB3_DVDD	VSS	VSS	VSS	VSS	VSS	VSS	AVDD18_TS_DDR	VSS	VDDPST33_ENET	VSS	VSS	DRAM_BP_AC11	DRAM_BP_DB16	DRAM_BP_DB13	F
G	DSP_I2S1_WS	DSP_I2S1_SCLK	DSP_I2S1_DO	DSP_I2S1_DI	DSP_I2S1_MCLK	VSS	VDDPST18_AON_IO	VSS	AVDD18_PLL_DSP	DVDD08_USB3_VP	VDDPST18_EMMC_D1_CAP	VDDPST18_EMMC_D3_CAP	AVDD18_USB2_VDDH0	VDDPST18_SDIO_D1_CAP	VDDPST18_SD_D1_CAP	VDDPST18_SD_D2_CAP	VSS	VSS	VDDPST18_ENET_D2_CAP	VSS	VDDQ_DDR	DRAM_BP_AC8	DRAM_BP_AC13	DRAM_BP_DB12	G
H	DSP_UART0_TXD	DSP_UART0_RXD	DSP_SPI6_SCLK	DSP_SPI6_SSN	DSP_SPI6_MOSI	VDDPST18_AON_IO	VSS	VDD08_AON	AVDD08_PLL_DSP	AVSS_PLL_DSP	VDD08_AON	VDDPST18_EMMC_D2_CAP	VSS	VDDPST18_SDIO_D2_CAP	VSS	VDD08_GPU	VDDPST18_ENET_D1_CAP	VDDPST18_ENET_D3_CAP	VSS	VDDQ_DDR	VSS	DRAM_BP_AC19	DRAM_BP_AC10	VSS	H
J	DSP_I2S0_MCLK	DSP_SPI6_MISO	DSP_I2S0_WS	DSP_I2S0_SCLK	VDDPST33_DSP_SDIO	VSS	VDDPST18_DSP_CAP	VSS	VDD08_DSP	VSS	VSS	VSS	DVDD08_USB2_DVDD	VSS	VDD08_GPU	VSS	VDD08_DDR	VDD08_DDR	VSS	VSS	VDDQ_DDR	VSS	**DRAM_BP_AC5**	**DRAM_BP_AC4**	J
K	DSP_I2S0_DI	DSP_I2S0_DO	VSS	DSP_I2C7_SDA	DSP_I2C7_SCL	VDDPST18_DSP_IO	VSS	VDD08_DSP	VSS	VDD08_DSP	VDD08_DSP	VDD08_SOC	VSS	VDD08_SOC	VSS	VDD08_GPU	VSS	VDDQ_DDR	VDDQ_DDR_LP	VSS	VSS	DRAM_BP_ZN	DRAM_BP_AC2	DRAM_BP_AC0	K
L	DSP_PDM_IN1	DSP_PDM_IN0	DSP_PDM_IN2	DSP_PDM_CKO	DSP_PDM_IN3	VSS	VDDPST18_DSP_IO	VSS	VDD08_CPU	VSS	VDD08_CPU	VSS	VDD08_SOC	VSS	VDD08_GPU	VSS	VDD08_DDR	X	X	VDDQ_DDR_LP	VDDQ_DDR_LP	DRAM_BP_AC3	DRAM_BP_AC1	VDDQ_DDR_LP	L
M	LSIO_UART7_TXD	LSIO_UART7_RXD	LSIO_UART7_CTS_N	LSIO_UART7_RTS_N	LSIO_UART1_RXD	VDDPST33_SDIO9	VSS	VDD08_CPU	VSS	VDD08_CPU	VSS	VOPS_EFUSE	VSS	AVDD08_PLL_DDR	AVDD18_PLL_DDR	VDD08_DDR	X	X	VDDQ_DDR	VSS	VDDA18_DDR_PHY	DRAM_BP_MEMRESET_L	DRAM_BP_AC9	DRAM_BP_AC12	M
N	LSIO_UART1_TXD	LSIO_UART1_CTS_N	LSIO_UART1_RTS_N	LSIO_UART2_TXD	VSS	VSS	VDDPST18_SDIO9_CAP	VSS	VDD08_CPU	VSS	AVDD18_VT	AVDD18_PLL	VDD08_SOC	AVSS_PLL_DDR	VDD08_DDR	VDD08_DDR	X	X	VDDQ_DDR	VDDQ_DDR	VSS	DRAM_BP_VREF	DRAM_BP_AC31	DRAM_BP_AC28	N
P	LSIO_UART2_RXD	LSIO_UART3_RXD	LSIO_UART3_TXD	LSIO_I2C0_SCL	VDDPST33_SDIO8	VSS	VDDPST18_SDIO8_CAP	VDD08_CPU	VSS	VDD08_CPU	AVSS_PLL	AVDD08_PLL	VSS	VDD08_BPU	VSS	VDD08_BPU	VSS	X	X	VDDQ_DDR_LP	VDDQ_DDR_LP	VSS	DRAM_BP_AC23	VSS	P
R	LSIO_I2C0_SDA	LSIO_UART4_TXD	VSS	LSIO_UART4_RXD	VDDPST33_SDIO7	VSS	VDDPST18_SDIO7_CAP	VSS	VDD08_SOC	VSS	VDD08_SOC	VSS	VDD08_BPU	X	X	VSS	VDD08_DDR	VDDQ_DDR	VDDQ_DDR_LP	VSS	VSS	DRAM_BP_AC21	DRAM_BP_AC20	DRAM_BP_AC22	R
T	LSIO_I2C1_SCL	LSIO_I2C1_SDA	LSIO_I2C2_SDA	LSIO_I2C2_SCL	VSS	VSS	VDDPST18_SDIO6_CAP	VDD08_SOC	VSS	VDD08_SOC	VSS	VDD08_SOC	VSS	X	X	VDD08_BPU	VDD08_DDR	VDD08_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VSS	**DRAM_BP_AC25**	**DRAM_BP_AC24**	T
U	LSIO_I2C3_SDA	LSIO_I2C3_SCL	LSIO_I2C4_SDA	LSIO_I2C4_SCL	LSIO_SPI0_SSN	VDDPST33_SDIO6	VSS	VSS	VDDPST18_GPIO1	VSS	AVDD08_VP_MIPI_RX	VDDPST18_SDIO5_CAP	VDD08_BPU	VDDPST18_SDIO3_CAP	VDD08_BPU	VSS	VSS	AVDD18_ADC	VDDQ_DDR	VSS	VDDQ_DDR	DRAM_BP_ALERT_N	DRAM_BP_AC32	VSS	U
V	LSIO_SPI0_SCLK	LSIO_SPI0_MISO	LSIO_SPI0_MOSI	LSIO_SPI1_SCLK	LSIO_SPI1_SSN_1	VSS	VSS	VDDPST18_GPIO1	VSS	VSS	AVDD18_VPH_MIPI_RX	VSS	VDDPST18_SDIO4_CAP	VSS	VDDPST18_SDIO2_CAP	VSS	AVDD08_VP_MIPI_TX	AVSS_ADC	VSS	VDDQ_DDR	VSS	DRAM_BP_AC33	DRAM_BP_AC30	DRAM_BP_DB28	V
W	**CSI_PHY3_CLKN**	**CSI_PHY3_CLKP**	VSS	LSIO_SPI1_SSN	LSIO_SPI1_MISO	LSIO_SPI4_MOSI	VSS	CSI_REXT	VSS	VDDPST33_SDIO5	VDDPST33_BT1120	AVDD18_TS_BPU	VSS	VDDPST18_SDIO1_CAP	VSS	AVDD18_VPH_MIPI_TX	AVSS_ADC	AVDD18_ADC	AVSS_ADC	VSS	VDDQ_DDR	DRAM_BP_AC29	DRAM_BP_DB29	DRAM_BP_DB31	W
Y	**CSI_PHY3_DATAN1**	**CSI_PHY3_DATAP1**	LSIO_SPI1_MOSI	LSIO_SPI3_SCLK	LSIO_SPI4_SSN	LSIO_SPI5_SCLK	LSIO_SPI5_MISO	LSIO_SPI2_SSN	LSIO_SPI2_SCLK	LSIO_SPI2_MOSI	LSIO_SPI2_MISO	VSS	DISP_DPHY_REXT	VSS	ADC_REXT	AVSS_ADC	**ADC_VREFP**	**ADC_VREFN**	ADC_VINS[1]	VSS	DRAM_BP_DB41	VDDQ_DDR	DRAM_BP_DB30	VSS	Y
AA	**CSI_PHY3_DATAN0**	**CSI_PHY3_DATAP0**	LSIO_SPI3_SSN	LSIO_SPI3_MISO	LSIO_SPI4_SCLK	LSIO_SPI5_SSN	LSIO_SPI5_MOSI	BT1120_O_DATA2	BT1120_O_DATA3	BT1120_O_DATA4	BT1120_O_DATA6	BT1120_O_DATA10	BT1120_O_DATA14	BT1120_O_DATA15	AVSS_ADC	ADC_VINS[5]	ADC_VINS[2]	AVSS_ADC	DRAM_BP_DB36	DRAM_BP_DB40	DRAM_BP_DB42	VSS	DRAM_BP_DB32	DRAM_BP_DB25	AA
AB	**CSI_PHY2_DATAN0**	**CSI_PHY2_DATAP0**	VSS	LSIO_SPI3_MOSI	LSIO_SPI4_MISO	VSS	BT1120_O_DATA0	BT1120_O_DATA1	VSS	BT1120_O_DATA5	BT1120_O_DATA7	BT1120_O_DATA11	VSS	BT1120_O_PIXELCLK	ADC_VINS[7]	ADC_VINS[6]	ADC_VINS[3]	ADC_VINS[0]	VSS	DRAM_BP_DB44	VSS	DRAM_BP_DB43	**DRAM_BP_DB34**	**DRAM_BP_DB33**	AB
AC	VSS	VSS	**CSI_PHY2_DATAP1**	**CSI_PHY2_CLKP**	**CSI_PHY1_CLKP**	**CSI_PHY1_DATAP1**	**CSI_PHY1_DATAP0**	**CSI_PHY0_DATAP0**	**CSI_PHY0_DATAP1**	**CSI_PHY0_CLKP**	BT1120_O_DATA9	BT1120_O_DATA13	**DISP_DPHY_CLKN**	**DISP_DPHY_DATAN2**	**DISP_DPHY_DATAN3**	**DISP_DPHY_DATAP1**	**DISP_DPHY_DATAP0**	ADC_VINS[4]	DRAM_BP_DB37	DRAM_BP_DB39	**DRAM_BP_DB46**	DRAM_BP_DB26	DRAM_BP_DB27	VSS	AC
AD	VSS	VSS	**CSI_PHY2_DATAN1**	**CSI_PHY2_CLKN**	**CSI_PHY1_CLKN**	**CSI_PHY1_DATAN1**	**CSI_PHY1_DATAN0**	**CSI_PHY0_DATAN0**	**CSI_PHY0_DATAN1**	**CSI_PHY0_CLKN**	BT1120_O_DATA8	BT1120_O_DATA12	**DISP_DPHY_CLKP**	**DISP_DPHY_DATAP2**	**DISP_DPHY_DATAP3**	**DISP_DPHY_DATAN1**	**DISP_DPHY_DATAN0**	AVSS_ADC	DRAM_BP_DB38	VSS	**DRAM_BP_DB45**	DRAM_BP_DB24	VSS	VSS	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

X No Ball In Matrix

Figure 3-2 X5 FCCSP563 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	
A	X	VSS	USB3_RX0_P	USB3_TX0_P	USB3_REF_CLK_P	USB3_DP0	USB2_VBUS0	USB2_DP0	HSIO_SDIO_DAT2	HSIO_SD_DAT2	HSIO_SD_CMD	HSIO_QSPI_DATA_3	A
B	VSS	AON_TEST_MODE	USB3_RX0_M	USB3_TX0_M	USB3_REF_CLK_M	USB3_DM0	USB3_VBUS0	USB2_DM0	HSIO_SDIO_DAT3	HSIO_SD_DAT3	HSIO_SD_DAT1	HSIO_SD_SDCLK	B
C	AON_XTALI_24M	AON_XTALO_24M	VSS	EMMC_RST_N	EMMC_DAT7	VSS	USB3_RESREF	EMMC_CMD	VSS	HSIO_SDIO_DAT0	HSIO_SDIO_SDCLK	HSIO_SD_DAT0	C
D	AON_ENV_VDD	AON_PMIC_EN	AON_HW_RESETN	AON_CLK_32K	EMMC_DAT6	EMMC_DAT5	EMMC_DAT4	EMMC_DAT1	USB2_TXRTUNE	HSIO_SDIO_DAT1	HSIO_SDIO_WP	VSS	D
E	AON_ENV_CNN0	AON_ENV_CNN1	AON_RESETN_OUT	AON_IRQ_OUT	AON_GPIO0_PIN00	EMMC_DAT3	EMMC_DAT2	EMMC_DAT0	EMMC_SDCLK	HSIO_SDIO_CDN	HSIO_SDIO_CMD	VDDPST33_EMMC	E
F	AON_GPIO0_PIN01	AON_GPIO0_PIN02	VSS	AON_GPIO0_PIN03	AON_GPIO0_PIN04	VSS	VSS	AVDD33_USB3	VSS	DVDD08_USB3_DVDD	VSS	VSS	F
G	DSP_I2S1_WS	DSP_I2S1_SCLK	DSP_I2S1_DO	DSP_I2S1_DI	DSP_I2S1_MCLK	VSS	VDDPST18_AON_IO	VSS	AVDD18_PLL_DSP	DVDD08_USB3_VP	VDDPST18_EMMC_D1_CAP	VDDPST18_EMMC_D3_CAP	G
H	DSP_UART0_TXD	DSP_UART0_RXD	DSP_SPI6_SCLK	DSP_SPI6_SSN	DSP_SPI6_MOSI	VDDPST18_AON_IO	VSS	VDD08_AON	AVDD08_PLL_DSP	AVSS_PLL_DSP	VDD08_AON	VDDPST18_EMMC_D2_CAP	H
J	DSP_I2S0_MCLK	DSP_SPI6_MISO	DSP_I2S0_WS	DSP_I2S0_SCLK	VDDPST33_DSP_SDIO	VSS	VDDPST18_DSP_CAP	VSS	VDD08_DSP	VSS	VSS	VSS	J
K	DSP_I2S0_DI	DSP_I2S0_DO	VSS	DSP_I2C7_SDA	DSP_I2C7_SCL	VDDPST18_DSP_IO	VSS	VDD08_DSP	VSS	VDD08_DSP	VDD08_DSP	VDD08_SOC	K
L	DSP_PDM_IN1	DSP_PDM_IN0	DSP_PDM_IN2	DSP_PDM_CKO	DSP_PDM_IN3	VSS	VDDPST18_DSP_IO	VSS	VDD08_CPU	VSS	VDD08_CPU	VSS	L
M	LSIO_UART7_TXD	LSIO_UART7_RXD	LSIO_UART7_CTS_N	LSIO_UART7_RTS_N	LSIO_UART1_RXD	VDDPST33_SDIO9	VSS	VDD08_CPU	VSS	VDD08_CPU	VSS	VQPS_EFUSE	M
	1	2	3	4	5	6	7	8	9	10	11	12	

X No Ball In Matrix

Figure 3-3 X5 FCCSP563 Ball Map (Top-Left Part)

	13	14	15	16	17	18	19	20	21	22	23	24	
A	HSIO_QSPI_SSN_0	HSIO_ENET_RXDV	HSIO_ENET_RXD_1	HSIO_ENET_RX_CLK	HSIO_ENET_RXD_0	HSIO_ENET_TXD_3	DRAM_BP_DB5	DRAM_BP_DB4	**DRAM_BP_DB10**	DRAM_BP_DB17	VSS	VSS	A
B	VSS	HSIO_QSPI_DATA_0	HSIO_QSPI_SSN_1	VSS	HSIO_ENET_TXEN	HSIO_ENET_TX_CLK	DRAM_BP_DB7	VSS	**DRAM_BP_DB9**	DRAM_BP_DB19	DRAM_BP_DB18	VSS	B
C	HSIO_SD_WP	HSIO_QSPI_DATA_2	HSIO_QSPI_SCLK	HSIO_ENET_RXD_2	HSIO_ENET_TXD_1	HSIO_ENET_TXD_0	DRAM_BP_DB6	DRAM_BP_DB8	VSS	DRAM_BP_DB1	**DRAM_BP_DB21**	**DRAM_BP_DB22**	C
D	HSIO_SD_CDN	HSIO_QSPI_DATA_1	VSS	HSIO_EPHY_CLK	HSIO_ENET_TXD_2	HSIO_ENET_MDIO	VSS	DRAM_BP_DB3	DRAM_BP_DB0	VSS	DRAM_BP_DB20	DRAM_BP_DB15	D
E	AVDD33_USB2_VDD330	VDDPST33_HS_SDIO	VDDPST33_SD	HSIO_ENET_RXD_3	HSIO_ENET_MDC	VDDPST18_QSPI	VSS	DRAM_BP_DB2	VDDQ_DDR	VDDQ_DDR	DRAM_BP_DB14	VSS	E
F	VSS	VSS	VSS	VSS	AVDD18_TS_DDR	VSS	VDDPST33_ENET	VSS	VSS	DRAM_BP_AC11	DRAM_BP_DB16	DRAM_BP_DB13	F
G	AVDD18_USB2_VDDH0	VDDPST18_SDIO_D1_CAP	VDDPST18_SD_D1_CAP	VDDPST18_SD_D2_CAP	VSS	VSS	VDDPST18_ENET_D2_CAP	VSS	VDDQ_DDR	DRAM_BP_AC8	DRAM_BP_AC13	DRAM_BP_DB12	G
H	VSS	VDDPST18_SDIO_D2_CAP	VSS	VDD08_GPU	VDDPST18_ENET_D1_CAP	VDDPST18_ENET_D3_CAP	VSS	VDDQ_DDR	VSS	DRAM_BP_AC19	DRAM_BP_AC10	VSS	H
J	DVDD08_USB2_DVDD	VSS	VDD08_GPU	VSS	VDD08_DDR	VDD08_DDR	VSS	VSS	VDDQ_DDR	VSS	**DRAM_BP_AC5**	**DRAM_BP_AC4**	J
K	VSS	VDD08_SOC	VSS	VDD08_GPU	VSS	VDDQ_DDR	VDDQ_DDR_LP	VSS	VSS	DRAM_BP_ZN	DRAM_BP_AC2	DRAM_BP_AC0	K
L	VDD08_SOC	VSS	VDD08_GPU	VSS	VDD08_DDR	X	X	VDDQ_DDR_LP	VDDQ_DDR_LP	DRAM_BP_AC3	DRAM_BP_AC1	VDDQ_DDR_LP	L
M	VSS	AVDD08_PLL_DDR	AVDD18_PLL_DDR	VDD08_DDR	X	X	VDDQ_DDR	VSS	VDDA18_DDR_PHY	DRAM_BP_MEMRESET_L	DRAM_BP_AC9	DRAM_BP_AC12	M
	13	14	15	16	17	18	19	20	21	22	23	24	

X No Ball In Matrix

Figure 3-4 X5 FCCSP563 Ball Map (Top-Right Part)

	1	2	3	4	5	6	7	8	9	10	11	12	
N	LSIO_UART1_TXD	LSIO_UART1_CTS_N	LSIO_UART1_RTS_N	LSIO_UART2_TXD	VSS	VSS	VDDPST18_SDIO9_CAP	VSS	VDD08_CPU	VSS	AVDD18_VT	AVDD18_PLL	N
P	LSIO_UART2_RXD	LSIO_UART3_RXD	LSIO_UART3_TXD	LSIO_I2C0_SCL	VDDPST33_SDIO8	VSS	VDDPST18_SDIO8_CAP	VDD08_CPU	VSS	VDD08_CPU	AVSS_PLL	AVDD08_PLL	P
R	LSIO_I2C0_SDA	LSIO_UART4_TXD	VSS	LSIO_UART4_RXD	VDDPST33_SDIO7	VSS	VDDPST18_SDIO7_CAP	VSS	VDD08_SOC	VSS	VDD08_SOC	VSS	R
T	LSIO_I2C1_SCL	LSIO_I2C1_SDA	LSIO_I2C2_SDA	LSIO_I2C2_SCL	VSS	VSS	VDDPST18_SDIO6_CAP	VDD08_SOC	VSS	VDD08_SOC	VSS	VDD08_SOC	T
U	LSIO_I2C3_SDA	LSIO_I2C3_SCL	LSIO_I2C4_SDA	LSIO_I2C4_SCL	LSIO_SPI0_SSN	VDDPST33_SDIO6	VSS	VSS	VDDPST18_GPIO1	VSS	AVDD08_VP_MIPI_RX	VDDPST18_SDIO5_CAP	U
V	LSIO_SPI0_SCLK	LSIO_SPI0_MISO	LSIO_SPI0_MOSI	LSIO_SPI1_SCLK	LSIO_SPI1_SSN_1	VSS	VSS	VDDPST18_GPIO1	VSS	VSS	AVDD18_VPH_MIPI_RX	VSS	V
W	**CSI_PHY3_CLKN**	**CSI_PHY3_CLKP**	VSS	LSIO_SPI1_SSN	LSIO_SPI1_MISO	LSIO_SPI4_MOSI	VSS	CSI_REXT	VSS	VDDPST33_SDIO5	VDDPST33_BT1120	AVDD18_TS_BPU	W
Y	**CSI_PHY3_DATAN1**	**CSI_PHY3_DATAP1**	LSIO_SPI1_MOSI	LSIO_SPI3_SCLK	LSIO_SPI4_SSN	LSIO_SPI5_SCLK	LSIO_SPI5_MISO	LSIO_SPI2_SSN	LSIO_SPI2_SCLK	LSIO_SPI2_MOSI	LSIO_SPI2_MISO	VSS	Y
AA	**CSI_PHY3_DATAN0**	**CSI_PHY3_DATAP0**	LSIO_SPI3_SSN	LSIO_SPI3_MISO	LSIO_SPI4_SCLK	LSIO_SPI5_SSN	LSIO_SPI5_MOSI	BT1120_O_DATA2	BT1120_O_DATA3	BT1120_O_DATA4	BT1120_O_DATA6	BT1120_O_DATA10	AA
AB	**CSI_PHY2_DATAN0**	**CSI_PHY2_DATAP0**	VSS	LSIO_SPI3_MOSI	LSIO_SPI4_MISO	VSS	BT1120_O_DATA0	BT1120_O_DATA1	VSS	BT1120_O_DATA5	BT1120_O_DATA7	BT1120_O_DATA11	AB
AC	VSS	VSS	**CSI_PHY2_DATAP1**	**CSI_PHY2_CLKP**	**CSI_PHY1_CLKP**	**CSI_PHY1_DATAP1**	**CSI_PHY1_DATAP0**	**CSI_PHY0_DATAP0**	**CSI_PHY0_DATAP1**	**CSI_PHY0_CLKP**	BT1120_O_DATA9	BT1120_O_DATA13	AC
AD	VSS	VSS	**CSI_PHY2_DATAN1**	**CSI_PHY2_CLKN**	**CSI_PHY1_CLKN**	**CSI_PHY1_DATAN1**	**CSI_PHY1_DATAN0**	**CSI_PHY0_DATAN0**	**CSI_PHY0_DATAN1**	**CSI_PHY0_CLKN**	BT1120_O_DATA8	BT1120_O_DATA12	AD
	1	2	3	4	5	6	7	8	9	10	11	12	

X No Ball In Matrix

Figure 3-5 X5 FCCSP563 Ball Map (Bottom-Left Part)

	13	14	15	16	17	18	19	20	21	22	23	24	
N	VDD08_SOC	AVSS_PLL_DDR	VDD08_DDR	VDD08_DDR	X	X	VDDQ_DDR	VDDQ_DDR	VSS	DRAM_BP_VREF	DRAM_BP_AC31	DRAM_BP_AC28	N
P	VSS	VDD08_BPU	VSS	VDD08_BPU	VSS	X	X	VDDQ_DDR_LP	VDDQ_DDR_LP	VSS	DRAM_BP_AC23	VSS	P
R	VDD08_BPU	X	X	VSS	VDD08_DDR	VDDQ_DDR	VDDQ_DDR_LP	VSS	VSS	DRAM_BP_AC21	DRAM_BP_AC20	DRAM_BP_AC22	R
T	VSS	X	X	VDD08_BPU	VDD08_DDR	VDD08_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VSS	**DRAM_BP_AC25**	**DRAM_BP_AC24**	T
U	VDD08_BPU	VDDPST18_SDIO3_CAP	VDD08_BPU	VSS	VSS	AVDD18_ADC	VDDQ_DDR	VSS	VDDQ_DDR	DRAM_BP_ALERT_N	DRAM_BP_AC32	VSS	U
V	VDDPST18_SDIO4_CAP	VSS	VDDPST18_SDIO2_CAP	VSS	AVDD08_VP_MIPI_TX	AVSS_ADC	VSS	VDDQ_DDR	VSS	DRAM_BP_AC33	DRAM_BP_AC30	DRAM_BP_DB28	V
W	VSS	VDDPST18_SDIO1_CAP	VSS	AVDD18_VPH_MIPI_TX	AVSS_ADC	AVDD18_ADC	AVSS_ADC	VSS	VDDQ_DDR	DRAM_BP_AC29	DRAM_BP_DB29	DRAM_BP_DB31	W
Y	DISP_DPHY_REXT	VSS	ADC_REXT	AVSS_ADC	**ADC_VREFP**	**ADC_VREFN**	ADC_VINS[1]	VSS	DRAM_BP_DB41	VDDQ_DDR	DRAM_BP_DB30	VSS	Y
AA	BT1120_O_DATA14	BT1120_O_DATA15	AVSS_ADC	ADC_VINS[5]	ADC_VINS[2]	AVSS_ADC	DRAM_BP_DB36	DRAM_BP_DB40	DRAM_BP_DB42	VSS	DRAM_BP_DB32	DRAM_BP_DB25	AA
AB	VSS	BT1120_O_PIXELCLK	ADC_VINS[7]	ADC_VINS[6]	ADC_VINS[3]	ADC_VINS[0]	VSS	DRAM_BP_DB44	VSS	DRAM_BP_DB43	**DRAM_BP_DB34**	**DRAM_BP_DB33**	AB
AC	**DISP_DPHY_CLKN**	**DISP_DPHY_DATAN2**	**DISP_DPHY_DATAN3**	**DISP_DPHY_DATAP1**	**DISP_DPHY_DATAP0**	ADC_VINS[4]	DRAM_BP_DB37	DRAM_BP_DB39	**DRAM_BP_DB46**	DRAM_BP_DB26	DRAM_BP_DB27	VSS	AC
AD	**DISP_DPHY_CLKP**	**DISP_DPHY_DATAP2**	**DISP_DPHY_DATAP3**	**DISP_DPHY_DATAN1**	**DISP_DPHY_DATAN0**	AVSS_ADC	DRAM_BP_DB38	VSS	**DRAM_BP_DB45**	DRAM_BP_DB24	VSS	VSS	AD
	13	14	15	16	17	18	19	20	21	22	23	24	

X No Ball In Matrix

Figure 3-6 X5 FCCSP563 Ball Map (Bottom-Right Part)

3.1.3 Pin List

Table 3-1 lists the pins alphabetically by ball number.

Table 3-1 Pin List

No.	Name	No.	Name
A1	NA	B1	VSS
A2	VSS	B2	AON_TEST_MODE

No.	Name	No.	Name
A3	USB3_RX0_P	B3	USB3_RX0_M
A4	USB3_TX0_P	B4	USB3_TX0_M
A5	USB3_REF_CLK_P	B5	USB3_REF_CLK_M
A6	USB3_DP0	B6	USB3_DM0
A7	USB2_VBUS0	B7	USB3_VBUS0
A8	USB2_DP0	B8	USB2_DM0
A9	HSIO_SDIO_DAT2	B9	HSIO_SDIO_DAT3
A10	HSIO_SD_DAT2	B10	HSIO_SD_DAT3
A11	HSIO_SD_CMD	B11	HSIO_SD_DAT1
A12	HSIO_QSPI_DATA_3	B12	HSIO_SD_SDCLK
A13	HSIO_QSPI_SSN_0	B13	VSS
A14	HSIO_ENET_RXDV	B14	HSIO_QSPI_DATA_0
A15	HSIO_ENET_RXD_1	B15	HSIO_QSPI_SSN_1
A16	HSIO_ENET_RX_CLK	B16	VSS
A17	HSIO_ENET_RXD_0	B17	HSIO_ENET_TXEN
A18	HSIO_ENET_TXD_3	B18	HSIO_ENET_TX_CLK
A19	DRAM_BP_DB5	B19	DRAM_BP_DB7
A20	DRAM_BP_DB4	B20	VSS
A21	DRAM_BP_DB10	B21	DRAM_BP_DB9
A22	DRAM_BP_DB17	B22	DRAM_BP_DB19
A23	VSS	B23	DRAM_BP_DB18
A24	VSS	B24	VSS
C1	AON_XTALI_24M	D1	AON_USB3_ID
C2	AON_XTALO_24M	D2	AON_PMIC_EN
C3	VSS	D3	AON_HW_RESETN
C4	EMMC_RST_N	D4	AON_CLK_32K
C5	EMMC_DAT7	D5	EMMC_DAT6
C6	VSS	D6	EMMC_DAT5
C7	USB3_RESREF	D7	EMMC_DAT4

No.	Name	No.	Name
C8	EMMC_CMD	D8	EMMC_DAT1
C9	VSS	D9	USB2_TXRTUNE
C10	HSIO_SDIO_DAT0	D10	HSIO_SDIO_DAT1
C11	HSIO_SDIO_SDCLK	D11	HSIO_SDIO_WP
C12	HSIO_SD_DAT0	D12	VSS
C13	HSIO_SD_WP	D13	HSIO_SD_CDN
C14	HSIO_QSPI_DATA_2	D14	HSIO_QSPI_DATA_1
C15	HSIO_QSPI_SCLK	D15	VSS
C16	HSIO_ENET_RXD_2	D16	HSIO_EPHY_CLK
C17	HSIO_ENET_TXD_1	D17	HSIO_ENET_TXD_2
C18	HSIO_ENET_TXD_0	D18	HSIO_ENET_MDIO
C19	DRAM_BP_DB6	D19	VSS
C20	DRAM_BP_DB8	D20	DRAM_BP_DB3
C21	VSS	D21	DRAM_BP_DB0
C22	DRAM_BP_DB1	D22	VSS
C23	DRAM_BP_DB21	D23	DRAM_BP_DB20
C24	DRAM_BP_DB22	D24	DRAM_BP_DB15
E1	AON_USB2_ID	F1	AON_GPIO0_PIN01
E2	AON_EFUSE_PWR_EN	F2	AON_GPIO0_PIN02
E3	AON_RESETN_OUT	F3	VSS
E4	AON_IRQ_OUT	F4	AON_GPIO0_PIN03
E5	AON_GPIO0_PIN00	F5	AON_GPIO0_PIN04
E6	EMMC_DAT3	F6	VSS
E7	EMMC_DAT2	F7	VSS
E8	EMMC_DAT0	F8	AVDD33_USB3
E9	EMMC_SDCLK	F9	VSS
E10	HSIO_SDIO_CDN	F10	DVDD08_USB3_DVDD
E11	HSIO_SDIO_CMD	F11	VSS
E12	VDDPST33_EMMC	F12	VSS

No.	Name	No.	Name
E13	AVDD33_USB2_VDD330	F13	VSS
E14	VDDPST33_HS_SDIO	F14	VSS
E15	VDDPST33_SD	F15	VSS
E16	HSIO_ENET_RXD_3	F16	VSS
E17	HSIO_ENET_MDC	F17	AVDD18_TS_DDR
E18	VDDPST18_QSPI	F18	VSS
E19	VSS	F19	VDDPST33_ENET
E20	DRAM_BP_DB2	F20	VSS
E21	VDDQ_DDR	F21	VSS
E22	VDDQ_DDR	F22	DRAM_BP_AC11
E23	DRAM_BP_DB14	F23	DRAM_BP_DB16
E24	VSS	F24	DRAM_BP_DB13
G1	DSP_I2S1_WS	H1	DSP_UART0_TXD
G2	DSP_I2S1_SCLK	H2	DSP_UART0_RXD
G3	DSP_I2S1_DO	H3	DSP_SPI6_SCLK
G4	DSP_I2S1_DI	H4	DSP_SPI6_SSN
G5	DSP_I2S1_MCLK	H5	DSP_SPI6_MOSI
G6	VSS	H6	VDDPST18_AON_IO
G7	VDDPST18_AON_IO	H7	VSS
G8	VSS	H8	VDD08_AON
G9	AVDD18_PLL_DSP	H9	AVDD08_PLL_DSP
G10	DVDD08_USB3_VP	H10	AVSS_PLL_DSP
G11	VDDPST18_EMMC_D1_CAP	H11	VDD08_AON
G12	VDDPST18_EMMC_D3_CAP	H12	VDDPST18_EMMC_D2_CAP
G13	AVDD18_USB2_VDDH0	H13	VSS
G14	VDDPST18_SDIO_D1_CAP	H14	VDDPST18_SDIO_D2_CAP
G15	VDDPST18_SD_D1_CAP	H15	VSS
G16	VDDPST18_SD_D2_CAP	H16	VDD08_GPU
G17	VSS	H17	VDDPST18_ENET_D1_CAP

No.	Name	No.	Name
G18	VSS	H18	VDDPST18_ENET_D3_CAP
G19	VDDPST18_ENET_D2_CAP	H19	VSS
G20	VSS	H20	VDDQ_DDR
G21	VDDQ_DDR	H21	VSS
G22	DRAM_BP_AC8	H22	DRAM_BP_AC19
G23	DRAM_BP_AC13	H23	DRAM_BP_AC10
G24	DRAM_BP_DB12	H24	VSS
J1	DSP_I2S0_MCLK	K1	DSP_I2S0_DI
J2	DSP_SPI6_MISO	K2	DSP_I2S0_DO
J3	DSP_I2S0_WS	K3	VSS
J4	DSP_I2S0_SCLK	K4	DSP_I2C7_SDA
J5	VDDPST33_DSP_SDIO	K5	DSP_I2C7_SCL
J6	VSS	K6	VDDPST18_DSP_IO
J7	VDDPST18_DSP_CAP	K7	VSS
J8	VSS	K8	VDD08_DSP
J9	VDD08_DSP	K9	VSS
J10	VSS	K10	VDD08_DSP
J11	VSS	K11	VDD08_DSP
J12	VSS	K12	VDD08_SOC
J13	DVDD08_USB2_DVDD	K13	VSS
J14	VSS	K14	VDD08_SOC
J15	VDD08_GPU	K15	VSS
J16	VSS	K16	VDD08_GPU
J17	VDD08_DDR	K17	VSS
J18	VDD08_DDR	K18	VDDQ_DDR
J19	VSS	K19	VDDQ_DDR_LP
J20	VSS	K20	VSS
J21	VDDQ_DDR	K21	VSS
J22	VSS	K22	DRAM_BP_ZN

No.	Name	No.	Name
J23	DRAM_BP_AC5	K23	DRAM_BP_AC2
J24	DRAM_BP_AC4	K24	DRAM_BP_AC0
L1	DSP_PDM_IN1	M1	LSIO_UART7_TXD
L2	DSP_PDM_IN0	M2	LSIO_UART7_RXD
L3	DSP_PDM_IN2	M3	LSIO_UART7_CTS_N
L4	DSP_PDM_CKO	M4	LSIO_UART7_RTS_N
L5	DSP_PDM_IN3	M5	LSIO_UART1_RXD
L6	VSS	M6	VDDPST33_SDIO9
L7	VDDPST18_DSP_IO	M7	VSS
L8	VSS	M8	VDD08_CPU
L9	VDD08_CPU	M9	VSS
L10	VSS	M10	VDD08_CPU
L11	VDD08_CPU	M11	VSS
L12	VSS	M12	VQPS_EFUSE
L13	VDD08_SOC	M13	VSS
L14	VSS	M14	AVDD08_PLL_DDR
L15	VDD08_GPU	M15	AVDD18_PLL_DDR
L16	VSS	M16	VDD08_DDR
L17	VDD08_DDR	M17	NA
L18	NA	M18	NA
L19	NA	M19	VDDQ_DDR
L20	VDDQ_DDR_LP	M20	VSS
L21	VDDQ_DDR_LP	M21	VDDA18_DDR_PHY
L22	DRAM_BP_AC3	M22	DRAM_BP_MEMRESET_L
L23	DRAM_BP_AC1	M23	DRAM_BP_AC9
L24	VDDQ_DDR_LP	M24	DRAM_BP_AC12
N1	LSIO_UART1_TXD	P1	LSIO_UART2_RXD
N2	LSIO_UART1_CTS_N	P2	LSIO_UART3_RXD
N3	LSIO_UART1_RTS_N	P3	LSIO_UART3_TXD

No.	Name	No.	Name
N4	LSIO_UART2_TXD	P4	LSIO_I2C0_SCL
N5	VSS	P5	VDDPST33_SDIO8
N6	VSS	P6	VSS
N7	VDDPST18_SDIO9_CAP	P7	VDDPST18_SDIO8_CAP
N8	VSS	P8	VDD08_CPU
N9	VDD08_CPU	P9	VSS
N10	VSS	P10	VDD08_CPU
N11	AVDD18_VT	P11	AVSS_PLL
N12	AVDD18_PLL	P12	AVDD08_PLL
N13	VDD08_SOC	P13	VSS
N14	AVSS_PLL_DDR	P14	VDD08_BPU
N15	VDD08_DDR	P15	VSS
N16	VDD08_DDR	P16	VDD08_BPU
N17	NA	P17	VSS
N18	NA	P18	NA
N19	VDDQ_DDR	P19	NA
N20	VDDQ_DDR	P20	VDDQ_DDR_LP
N21	VSS	P21	VDDQ_DDR_LP
N22	DRAM_BP_VREF	P22	VSS
N23	DRAM_BP_AC31	P23	DRAM_BP_AC23
N24	DRAM_BP_AC28	P24	VSS
R1	LSIO_I2C0_SDA	T1	LSIO_I2C1_SCL
R2	LSIO_UART4_TXD	T2	LSIO_I2C1_SDA
R3	VSS	T3	LSIO_I2C2_SDA
R4	LSIO_UART4_RXD	T4	LSIO_I2C2_SCL
R5	VDDPST33_SDIO7	T5	VSS
R6	VSS	T6	VSS
R7	VDDPST18_SDIO7_CAP	T7	VDDPST18_SDIO6_CAP
R8	VSS	T8	VDD08_SOC

No.	Name	No.	Name
R9	VDD08_SOC	T9	VSS
R10	VSS	T10	VDD08_SOC
R11	VDD08_SOC	T11	VSS
R12	VSS	T12	VDD08_SOC
R13	VDD08_BPU	T13	VSS
R14	NA	T14	NA
R15	NA	T15	NA
R16	VSS	T16	VDD08_BPU
R17	VDD08_DDR	T17	VDD08_DDR
R18	VDDQ_DDR	T18	VDD08_DDR
R19	VDDQ_DDR_LP	T19	VSS
R20	VSS	T20	VDDQ_DDR
R21	VSS	T21	VDDQ_DDR
R22	DRAM_BP_AC21	T22	VSS
R23	DRAM_BP_AC20	T23	DRAM_BP_AC25
R24	DRAM_BP_AC22	T24	DRAM_BP_AC24
U1	LSIO_I2C3_SDA	V1	LSIO_SPI0_SCLK
U2	LSIO_I2C3_SCL	V2	LSIO_SPI0_MISO
U3	LSIO_I2C4_SDA	V3	LSIO_SPI0_MOSI
U4	LSIO_I2C4_SCL	V4	LSIO_SPI1_SCLK
U5	LSIO_SPI0_SSN	V5	LSIO_SPI1_SSN_1
U6	VDDPST33_SDIO6	V6	VSS
U7	VSS	V7	VSS
U8	VSS	V8	VDDPST18_GPIO1
U9	VDDPST18_GPIO1	V9	VSS
U10	VSS	V10	VSS
U11	AVDD08_VP_MIPI_RX	V11	AVDD18_VPH_MIPI_RX
U12	VDDPST18_SDIO5_CAP	V12	VSS
U13	VDD08_BPU	V13	VDDPST18_SDIO4_CAP

No.	Name	No.	Name
U14	VDDPST18_SDIO3_CAP	V14	VSS
U15	VDD08_BPU	V15	VDDPST18_SDIO2_CAP
U16	VSS	V16	VSS
U17	VSS	V17	AVDD08_VP_MIPI_TX
U18	AVDD18_ADC	V18	AVSS_ADC
U19	VDDQ_DDR	V19	VSS
U20	VSS	V20	VDDQ_DDR
U21	VDDQ_DDR	V21	VSS
U22	DRAM_BP_ALERT_N	V22	DRAM_BP_AC33
U23	DRAM_BP_AC32	V23	DRAM_BP_AC30
U24	VSS	V24	DRAM_BP_DB28
W1	CSI_PHY3_CLKN	Y1	CSI_PHY3_DATAN1
W2	CSI_PHY3_CLKP	Y2	CSI_PHY3_DATAP1
W3	VSS	Y3	LSIO_SPI1_MOSI
W4	LSIO_SPI1_SSN	Y4	LSIO_SPI3_SCLK
W5	LSIO_SPI1_MISO	Y5	LSIO_SPI4_SSN
W6	LSIO_SPI4_MOSI	Y6	LSIO_SPI5_SCLK
W7	VSS	Y7	LSIO_SPI5_MISO
W8	CSI_REXT	Y8	LSIO_SPI2_SSN
W9	VSS	Y9	LSIO_SPI2_SCLK
W10	VDDPST33_SDIO5	Y10	LSIO_SPI2_MOSI
W11	VDDPST33_BT1120	Y11	LSIO_SPI2_MISO
W12	AVDD18_TS_BPU	Y12	VSS
W13	VSS	Y13	DISP_DPHY_REXT
W14	VDDPST18_SDIO1_CAP	Y14	VSS
W15	VSS	Y15	ADC_REXT
W16	AVDD18_VPH_MIPI_TX	Y16	AVSS_ADC
W17	AVSS_ADC	Y17	ADC_VREFP
W18	AVDD18_ADC	Y18	ADC_VREFN

No.	Name	No.	Name
W19	AVSS_ADC	Y19	ADC_VINS[1]
W20	VSS	Y20	VSS
W21	VDDQ_DDR	Y21	DRAM_BP_DB41
W22	DRAM_BP_AC29	Y22	VDDQ_DDR
W23	DRAM_BP_DB29	Y23	DRAM_BP_DB30
W24	DRAM_BP_DB31	Y24	VSS
AA1	CSI_PHY3_DATAN0	AB1	CSI_PHY2_DATAN0
AA2	CSI_PHY3_DATAP0	AB2	CSI_PHY2_DATAP0
AA3	LSIO_SPI3_SSN	AB3	VSS
AA4	LSIO_SPI3_MISO	AB4	LSIO_SPI3_MOSI
AA5	LSIO_SPI4_SCLK	AB5	LSIO_SPI4_MISO
AA6	LSIO_SPI5_SSN	AB6	VSS
AA7	LSIO_SPI5_MOSI	AB7	BT1120_O_DATA0
AA8	BT1120_O_DATA2	AB8	BT1120_O_DATA1
AA9	BT1120_O_DATA3	AB9	VSS
AA10	BT1120_O_DATA4	AB10	BT1120_O_DATA5
AA11	BT1120_O_DATA6	AB11	BT1120_O_DATA7
AA12	BT1120_O_DATA10	AB12	BT1120_O_DATA11
AA13	BT1120_O_DATA14	AB13	VSS
AA14	BT1120_O_DATA15	AB14	BT1120_O_PIXELCLK
AA15	AVSS_ADC	AB15	ADC_VINS[7]
AA16	ADC_VINS[5]	AB16	ADC_VINS[6]
AA17	ADC_VINS[2]	AB17	ADC_VINS[3]
AA18	AVSS_ADC	AB18	ADC_VINS[0]
AA19	DRAM_BP_DB36	AB19	VSS
AA20	DRAM_BP_DB40	AB20	DRAM_BP_DB44
AA21	DRAM_BP_DB42	AB21	VSS
AA22	VSS	AB22	DRAM_BP_DB43
AA23	DRAM_BP_DB32	AB23	DRAM_BP_DB34

No.	Name	No.	Name
AA24	DRAM_BP_DB25	AB24	DRAM_BP_DB33
AC1	VSS	AD1	VSS
AC2	VSS	AD2	VSS
AC3	CSI_PHY2_DATAP1	AD3	CSI_PHY2_DATAN1
AC4	CSI_PHY2_CLKP	AD4	CSI_PHY2_CLKN
AC5	CSI_PHY1_CLKP	AD5	CSI_PHY1_CLKN
AC6	CSI_PHY1_DATAP1	AD6	CSI_PHY1_DATAN1
AC7	CSI_PHY1_DATAP0	AD7	CSI_PHY1_DATAN0
AC8	CSI_PHY0_DATAP0	AD8	CSI_PHY0_DATAN0
AC9	CSI_PHY0_DATAP1	AD9	CSI_PHY0_DATAN1
AC10	CSI_PHY0_CLKP	AD10	CSI_PHY0_CLKN
AC11	BT1120_O_DATA9	AD11	BT1120_O_DATA8
AC12	BT1120_O_DATA13	AD12	BT1120_O_DATA12
AC13	DISP_DPHY_CLKN	AD13	DISP_DPHY_CLKP
AC14	DISP_DPHY_DATAN2	AD14	DISP_DPHY_DATAP2
AC15	DISP_DPHY_DATAN3	AD15	DISP_DPHY_DATAP3
AC16	DISP_DPHY_DATAP1	AD16	DISP_DPHY_DATAN1
AC17	DISP_DPHY_DATAP0	AD17	DISP_DPHY_DATAN0
AC18	ADC_VINS[4]	AD18	AVSS_ADC
AC19	DRAM_BP_DB37	AD19	DRAM_BP_DB38
AC20	DRAM_BP_DB39	AD20	VSS
AC21	DRAM_BP_DB46	AD21	DRAM_BP_DB45
AC22	DRAM_BP_DB26	AD22	DRAM_BP_DB24
AC23	DRAM_BP_DB27	AD23	VSS
AC24	VSS	AD24	VSS

(1) NC_* means balls still exist but not connected
(2) NA means balls are removed

3.2 Pin Description

Table 3-2 lists the terms used for describing pin functions and features.

Table 3-2 Pin Symbol Description

Abbreviation	Description
I	Digital input
O	Digital output
IO	Digital input/output, controlled by software or function module
AI	Analog input
AO	Analog output
AIO	Analog input/output
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground
PD	With internal pull-down resistor
PU	With internal pull-up resistor

3.2.1 Power/Ground Pins

Table 3-3 Power/Ground Pin List

Pin Name	Number	Ball	Description
Digital Core Power			
VDD08_AON	2	H8,H11	Always on domain core power 0.8V +/- 10%
VDD08_BPU	6	P14, P16, R13, T16, U13, U15	BPU domain core power 0.8V +10%, - 7%
VDD08_CPU	7	L9, L11, M8, M10, N9, P8, P10	CPU domain core power 1.0V +5%, -10% for X5H 0.85V +/- 10% for X5M
VDD08_DDR	9	J17, J18, L17, M16, N15, N16, R17, T17, T18	DDR domain core power 0.8V +10%, - 7%
VDD08_DSP	4	J9, K8, K10, K11	DSP domain core power 0.8V +/- 10%
VDD08_GPU	4	H16, J15, K16, L15	GPU domain core power 0.8V +10%, - 7%
VDD08_SOC	9	K12, K14, L13,	TOP domain core power

Pin Name	Number	Ball	Description
		N13, R9, R11, T8, T10, T12	0.8V +10%, - 7%
Digital IO Power			
VDDPST18_AON_IO	2	G7,H6	General digital IO power in the AON subsystem
VDDPST18_DSP_IO	2	K6,L7	General digital IO power in the DSP subsystem
VDDPST18_QSPI	1	E18	QSPI digital IO power in the HSIO subsystem
VDDPST18_GPIO1	2	U9,V8	SPI0/SPI1/SPI3/SPI4/SPI5 digital IO power in the LSIO subsystem
VDDPST33_EMMC	1	E12	EMMC digital IO power in the HSIO subsystem
VDDPST33_HS_SDIO	1	E14	SDIO digital IO power in the HSIO subsystem
VDDPST33_SD	1	E15	SD card digital IO power in the HSIO subsystem
VDDPST33_ENET	1	F19	ENET digital IO power in the HSIO subsystem
VDDPST33_DSP_SDIO	1	J5	I2S1 digital IO power in the LSIO subsystem
VDDPST33_SDIO9	1	M6	UART0 digital IO power in the LSIO subsystem
VDDPST33_SDIO8	1	P5	UART1 digital IO power in the LSIO subsystem
VDDPST33_SDIO7	1	R5	UART2/UART3/UART4 digital IO power in the LSIO subsystem
VDDPST33_SDIO6	1	U6	I2C0/I2C1 digital IO power in the LSIO subsystem
VDDPST33_SDIO5	1	W10	SPI2 digital IO power in the LSIO subsystem
VDDPST33_BT1120	1	W11	BT1120 digital IO power
Analog Power			
AVDD33_USB2_VDD330	1	F13	USB2 PHY 3.3v Analog power
AVDD18_USB2_VDDH0	1	G13	USB2 PHY regulator power
DVDD08_USB2_DVDD	1	J13	USB2 PHY digital power

Pin Name	Number	Ball	Description
AVDD33_USB3	1	F8	USB3 PHY high-voltage power
DVDD08_USB3_DVDD	1	F10	USB3 PHY analog and digital low-voltage power
DVDD08_USB3_VP	1	J10	USB3 PHY analog and digital low-voltage power
AVDD18_PLL_DSP	1	G9	PLL 1.8V analog power in the DSP subsystem
AVDD08_PLL_DSP	1	H9	PLL 0.8V analog power in the DSP subsystem
AVDD18_PLL_DDR	1	M14	PLL 1.8V analog power in the DDR subsystem
AVDD08_PLL_DDR	1	M15	PLL 0.8V analog power in the DDR subsystem
AVDD18_PLL	1	N12	PLL 1.8V analog power in the TOP subsystem
AVDD08_PLL	1	P12	PLL 0.8V analog power in the TOP subsystem
AVDD08_VP_MIPI_RX	1	U11	MIPI RX PHY 0.8V Analog power
AVDD18_VPH_MIPI_RX	1	V11	MIPI RX PHY 1.8V Analog power
AVDD08_VP_MIPI_TX	1	V17	MIPI TX PHY 0.8V Analog power
AVDD18_VPH_MIPI_TX	1	W16	MIPI TX PHY 1.8V Analog power
VDDA18_DDR_PHY	1	M21	DDR PHY 1.8V Analog power
VDDQ_DDR	17	E21, E22, G21, H20, J21, K18, M19, N19, N20, R18, T20, T21, U19, U21, V20, W21, Y22	DDR PHY VDDQ I/O power
VDDQ_DDR_LP	7	K19, L20, L21, L24, P20, P21, R19	DDR PHY VDDQLP I/O power
AVDD18_VT	1	N11	Voltage sensor 1.8V analog power
AVDD18_TS_BPU	1	W12	BPU TS 1.8V analog power
AVDD18_TS_DDR	1	F17	DDR TS 1.8V analog power
AVDD18_ADC	2	U18,W18	ADC 1.8V analog power
VQPS_EFUSE	1	M12	EFUSE programming power

Pin Name	Number	Ball	Description
Ground			
VSS	139	refer to ball map	Digital ground
AVSS_PLL_DSP	1	H10	Analog ground of PLL in the DSP subsystem
AVSS_PLL_DDR	1	N14	Analog ground of PLL in the DDR subsystem
AVSS_PLL	1	P11	Analog ground of PLL in the TOP subsystem
AVSS_ADC	7	V18, W17, W19, Y16, AA15, AA18, AD18	Analog ground of ADC

3.2.2 Digital Pins

3.2.2.1 Digital Pin List

Table 3-4 Digital Pin List

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
Common					
AON_TEST_MODE	B2	I	PD	-	VDDPST18_AON_IO
AON_XTALI_24M	C1	CIN	CIN	-	
AON_XTALO_24M	C2	COUT	COUT	config	
AON_CLK_32K	D4	CIN	CIN	-	
AON_HW_RESETN	D3	I	-	-	
AON_PMIC_EN	D2	O	-	config	
AON_USB3_ID	D1	IO	-	config	
AON_USB2_ID	E1	IO	-	config	
AON_EFUSE_PWR_EN	E2	IO	-	config	
AON_RESETN_OUT	E3	O	-	config	
AON_IRQ_OUT	E4	O	-	config	
AON_GPIO0_PIN00	E5	IO	-	config	
AON_GPIO0_PIN01	F1	IO	-	config	
AON_GPIO0_PIN02	F2	IO	-	config	
AON_GPIO0_PIN03	F4	IO	-	config	

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
AON_GPIO0_PIN04	F5	IO	-	config	
UART0					
DSP_UART0_TXD	H1	IO	PU	config	VDDPST18_DSP_IO
DSP_UART0_RXD	H2	IO	PU	config	
SPI6					
DSP_SPI6_SSN	H4	IO	PD	config	VDDPST18_DSP_IO
DSP_SPI6_SCLK	H3	IO	PD	config	
DSP_SPI6_MOSI	H5	IO	PD	config	
DSP_SPI6_MISO	J2	IO	PD	config	
I2S1					
DSP_I2S1_MCLK	G5	IO	-	config	VDDPST33_DSP_SDIO
DSP_I2S1_WS	G1	IO	-	config	
DSP_I2S1_SCLK	G2	IO	-	config	
DSP_I2S1_DO	G3	IO	-	config	
DSP_I2S1_DI	G4	IO	-	config	
I2S0					
DSP_I2S0_MCLK	J1	IO	PD	config	VDDPST18_DSP_IO
DSP_I2S0_WS	J3	IO	PD	config	
DSP_I2S0_SCLK	J4	IO	PD	config	
DSP_I2S0_DO	K2	IO	PD	config	
DSP_I2S0_DI	K1	IO	PD	config	
I2C7					
DSP_I2C7_SDA	K4	IO	PD	config	VDDPST18_DSP_IO
DSP_I2C7_SCL	K5	IO	PD	config	
PDM					
DSP_PDM_IN0	L2	IO	PD	config	VDDPST18_DSP_IO
DSP_PDM_IN1	L1	IO	PD	config	
DSP_PDM_IN2	L3	IO	PD	config	
DSP_PDM_IN3	L5	IO	PD	config	
DSP_PDM_CKO	L4	IO	PD	config	
UART7					
LSIO_UART7_RXD	M2	IO	-	config	VDDPST33_SDIO9

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
LSIO_UART7_TXD	M1	IO	-	config	
LSIO_UART7_CTS_N	M3	IO	-	config	
LSIO_UART7_RTS_N	M4	IO	-	config	
UART1					
LSIO_UART1_RXD	M5	IO	-	config	VDDPST33_SDIO8
LSIO_UART1_TXD	N1	IO	-	config	
LSIO_UART1_CTS_N	N2	IO	-	config	
LSIO_UART1_RTS_N	N3	IO	-	config	
UART2					
LSIO_UART2_RXD	P1	IO	-	config	VDDPST33_SDIO7
LSIO_UART2_TXD	N4	IO	-	config	
UART3					
LSIO_UART3_RXD	P2	IO	-	config	VDDPST33_SDIO7
LSIO_UART3_TXD	P3	IO	-	config	
UART4					
LSIO_UART4_RXD	R4	IO	-	config	VDDPST33_SDIO7
LSIO_UART4_TXD	R2	IO	-	config	
SPI0					
LSIO_SPI0_SCLK	V1	IO	-	config	VDDPST18_GPIO1
LSIO_SPI0_SSN	U5	IO	-	config	
LSIO_SPI0_MISO	V2	IO	-	config	
LSIO_SPI0_MOSI	V3	IO	-	config	
SPI1					
LSIO_SPI1_SCLK	V4	IO	-	config	VDDPST18_GPIO1
LSIO_SPI1_SSN	W4	IO	-	config	
LSIO_SPI1_SSN_1	V5	IO	-	config	
LSIO_SPI1_MISO	W5	IO	-	config	
LSIO_SPI1_MOSI	Y3	IO	-	config	
SPI2					
LSIO_SPI2_SCLK	Y9	IO	-	config	VDDPST33_SDIO5
LSIO_SPI2_SSN	Y8	IO	-	config	
LSIO_SPI2_MISO	Y11	IO	-	config	

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
LSIO_SPI2_MOSI	Y10	IO	-	config	
SPI3					
LSIO_SPI3_SCLK	Y4	IO	-	config	VDDPST18_GPIO1
LSIO_SPI3_SSN	AA3	IO	-	config	
LSIO_SPI3_MISO	AA4	IO	-	config	
LSIO_SPI3_MOSI	AB4	IO	-	config	
SPI4					
LSIO_SPI4_SCLK	AA5	IO	-	config	VDDPST18_GPIO1
LSIO_SPI4_SSN	Y5	IO	-	config	
LSIO_SPI4_MISO	AB5	IO	-	config	
LSIO_SPI4_MOSI	W6	IO	-	config	
SPI5					
LSIO_SPI5_SCLK	Y6	IO	-	config	VDDPST18_GPIO1
LSIO_SPI5_SSN	AA6	IO	-	config	
LSIO_SPI5_MISO	Y7	IO	-	config	
LSIO_SPI5_MOSI	AA7	IO	-	config	
I2C0					
LSIO_I2C0_SCL	P4	IO	-	config	VDDPST33_SDIO6
LSIO_I2C0_SDA	R1	IO	-	config	
I2C1					
LSIO_I2C1_SCL	T1	IO	-	config	VDDPST33_SDIO6
LSIO_I2C1_SDA	T2	IO	-	config	
I2C2					
LSIO_I2C2_SCL	T4	IO	-	config	VDDPST18_GPIO1
LSIO_I2C2_SDA	T3	IO	-	config	
I2C3					
LSIO_I2C3_SCL	U2	IO	-	config	VDDPST18_GPIO1
LSIO_I2C3_SDA	U1	IO	-	config	
I2C4					
LSIO_I2C4_SCL	U4	IO	-	config	VDDPST18_GPIO1
LSIO_I2C4_SDA	U3	IO	-	config	
BT1120 OUT					

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
BT1120_O_DATA0	AB7	IO	-	config	VDDPST33_BT1120
BT1120_O_DATA1	AB8	IO	-	config	
BT1120_O_DATA2	AA8	IO	-	config	
BT1120_O_DATA3	AA9	IO	-	config	
BT1120_O_DATA4	AA10	IO	-	config	
BT1120_O_DATA5	AB10	IO	-	config	
BT1120_O_DATA6	AA11	IO	-	config	
BT1120_O_DATA7	AB11	IO	-	config	
BT1120_O_DATA8	AD11	IO	-	config	
BT1120_O_DATA9	AC11	IO	-	config	
BT1120_O_DATA10	AA12	IO	-	config	
BT1120_O_DATA11	AB12	IO	-	config	
BT1120_O_DATA12	AD12	IO	-	config	
BT1120_O_DATA13	AC12	IO	-	config	
BT1120_O_DATA14	AA13	IO	-	config	
BT1120_O_DATA15	AA14	IO	-	config	
BT1120_O_PIXELCLK	AB14	IO	-	config	
EMAC					
HSIO_ENET_MDC	E17	IO	-	config	VDDPST33_ENET
HSIO_ENET_MDIO	D18	IO	-	config	
HSIO_ENET_TXD_0	C18	IO	-	config	
HSIO_ENET_TXD_1	C17	IO	-	config	
HSIO_ENET_TXD_2	D17	IO	-	config	
HSIO_ENET_TXD_3	A18	IO	-	config	
HSIO_ENET_TXEN	B17	IO	-	config	
HSIO_ENET_TX_CLK	B18	IO	-	config	
HSIO_ENET_RX_CLK	A16	IO	-	config	
HSIO_ENET_RXD_0	A17	IO	-	config	
HSIO_ENET_RXD_1	A15	IO	-	config	
HSIO_ENET_RXD_2	C16	IO	-	config	
HSIO_ENET_RXD_3	E16	IO	-	config	
HSIO_ENET_RXDV	A14	IO	-	config	

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
HSIO_EPHY_CLK	D16	IO	-	config	
SDIO0					
HSIO_SD_WP	C13	IO	-	config	VDDPST33_SD
HSIO_SD_SDCLK	B12	IO	-	config	
HSIO_SD_CMD	A11	IO	-	config	
HSIO_SD_CDN	D13	IO	-	config	
HSIO_SD_DAT0	C12	IO	-	config	
HSIO_SD_DAT1	B11	IO	-	config	
HSIO_SD_DAT2	A10	IO	-	config	
HSIO_SD_DAT3	B10	IO	-	config	
SDIO1					
HSIO_SDIO_WP	D11	IO	-	config	VDDPST33_SDIO
HSIO_SDIO_SDCLK	C11	IO	-	config	
HSIO_SDIO_CMD	E11	IO	-	config	
HSIO_SDIO_CDN	E10	IO	-	config	
HSIO_SDIO_DAT0	C10	IO	-	config	
HSIO_SDIO_DAT1	D10	IO	-	config	
HSIO_SDIO_DAT2	A9	IO	-	config	
HSIO_SDIO_DAT3	B9	IO	-	config	
QSPI					
HSIO_QSPI_SSN_0	A13	IO	-	config	VDDPST18_QSPI
HSIO_QSPI_SSN_1	B15	IO	-	config	
HSIO_QSPI_SCLK	C15	IO	-	config	
HSIO_QSPI_DATA_0	B14	IO	-	config	
HSIO_QSPI_DATA_1	D14	IO	-	config	
HSIO_QSPI_DATA_2	C14	IO	-	config	
HSIO_QSPI_DATA_3	A12	IO	-	config	
EMMC					
EMMC_SDCLK	E9	IO	-	config	VDDPST33_EMMC
EMMC_CMD	C8	IO	-	config	
EMMC_DAT0	E8	IO	-	config	
EMMC_DAT1	D8	IO	-	config	

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
EMMC_DAT2	E7	IO	-	config	
EMMC_DAT3	E6	IO	-	config	
EMMC_DAT4	D7	IO	-	config	
EMMC_DAT5	D6	IO	-	config	
EMMC_DAT6	D5	IO	-	config	
EMMC_DAT7	C5	IO	-	config	
EMMC_RST_n	C4	IO	-	config	

3.2.2.2 Digital Pin Multiplexing

The X5 SoC has a lot of functionalities but a limited number of pins. Even though a single pin can only perform one function at a time, they can be configured internally to perform different functions. Table 3-5 details the pin multiplexing configuration for each pin.

Table 3-5 Digital Pin Multiplexing

Pin Name	Mux	Functions	Default Dir	Dir	Description
AON_TEST_MODE	NA	AON_TEST_MODE	I	I	Chip mode selection: 0: function mode 1: test mode for ATE
AON_XTALI_24M	NA	AON_XTALI_24M	I	I	24 M crystal input
AON_XTALO_24M	NA	AON_XTALO_24M	O	O	24 M crystal output
AON_CLK_32K	NA	AON_CLK_32K	I	I	32 K clock external input
AON_HW_RESETN	NA	AON_HW_RESETN	I	I	External Hardware reset
AON_PMIC_EN	NA	AON_PMIC_EN	O	O	Output control to enable/disable PMIC
AON_USB3_ID	0	AON_USB3_ID	IO	IO	Output control to enable/disable shutdown domain powers
	1	AON_GPIO0_PIN05	-	IO	GPIO
AON_USB2_ID	0	AON_USB2_ID	IO	IO	Output control to enable/disable shutdown domain powers
	1	AON_GPIO0_PIN06	-	IO	GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
AON_EFUSE_PWR_EN	0	AON_EFUSE_PWR_EN	IO	IO	Output control to enable/disable shutdown domain powers
	1	AON_GPIO0_PIN07	-	IO	GPIO
AON_RESETN_OUT	NA	AON_RESETN_OUT	O	O	System reset out
AON_IRQ_OUT	NA	AON_IRQ_OUT	O	O	Watch dog reset out
AON_GPIO0_PIN00	NA	AON_GPIO0_PIN00	IO	IO	GPIO
AON_GPIO0_PIN01	NA	AON_GPIO0_PIN01	IO	IO	GPIO
AON_GPIO0_PIN02	NA	AON_GPIO0_PIN02	IO	IO	GPIO
AON_GPIO0_PIN03	NA	AON_GPIO0_PIN03	IO	IO	GPIO
AON_GPIO0_PIN04	NA	AON_GPIO0_PIN04	IO	IO	GPIO
DSP_UART0_TXD	0	DSP_UART0_TXD	IO	IO	UART5 TX data output
	1	DSP_GPIO0_PIN03	-	IO	GPIO
DSP_UART0_RXD	0	DSP_UART0_RXD	IO	IO	UART5 RX data input
	1	DSP_GPIO0_PIN02	-	IO	GPIO
DSP_SPI6_SSN	0	DSP_SPI6_SSN	-	IO	SPI6 master chip select output SPI6 slave chip select input
	1	DSP_GPIO0_PIN20	IO	IO	GPIO
DSP_SPI6_SCLK	0	DSP_SPI6_SCLK	-	IO	SPI6 master clock output SPI6 slave clock input
	1	DSP_GPIO0_PIN19	IO	IO	GPIO
DSP_SPI6_MOSI	0	DSP_SPI6_MOSI	-	IO	SPI6 master data output SPI6 slave data input
	1	DSP_GPIO0_PIN22	IO	IO	GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
DSP_SPI6_MISO	0	DSP_SPI6_MISO	-	IO	SPI6 master data input SPI6 slave data output
	1	DSP_GPIO0_PIN21	IO	IO	GPIO
DSP_I2S1_MCLK	0	DSP_I2S1_MCLK	-	IO	I2S1 master clock out I2S1 slave clock in
	1	DSP_GPIO0_PIN09	IO	IO	GPIO
DSP_I2S1_WS	0	DSP_I2S1_WS	-	IO	I2S1 master Word Select line output I2S1 slave Word Select line input
	1	DSP_GPIO0_PIN11	IO	IO	GPIO
DSP_I2S1_SCLK	0	DSP_I2S1_SCLK	-	IO	I2S1 master clock output I2S1 slave clock input
	1	DSP_GPIO0_PIN10	IO	IO	GPIO
DSP_I2S1_DO	0	DSP_I2S1_DO	-	IO	I2S1 master data output I2S1 slave data input
	1	DSP_GPIO0_PIN13	IO	IO	GPIO
DSP_I2S1_DI	0	DSP_I2S1_DI	-	IO	I2S1 master data input I2S1 slave data output
	1	DSP_GPIO0_PIN12	IO	IO	GPIO
DSP_I2S0_MCLK	0	DSP_I2S0_MCLK	-	IO	I2S0 master clock out I2S0 slave clock in
	1	DSP_GPIO0_PIN04	IO	IO	GPIO
DSP_I2S0_WS	0	DSP_I2S0_WS	-	IO	I2S0 master Word Select line output I2S0 slave Word Select line input
	1	DSP_GPIO0_PIN06	IO	IO	GPIO
DSP_I2S0_SCLK	0	DSP_I2S0_SCLK	-	IO	I2S0 master clock output I2S0 slave clock input

Pin Name	Mux	Functions	Default Dir	Dir	Description
	1	DSP_GPIO0_PIN05	IO	IO	GPIO
DSP_I2S0_DO	0	DSP_I2S0_DO	-	IO	I2S0 master data output I2S0 slave data input
	1	DSP_GPIO0_PIN08	IO	IO	GPIO
DSP_I2S0_DI	0	DSP_I2S0_DI	-	IO	I2S0 master data input I2S0 slave data output
	1	DSP_GPIO0_PIN07	IO	IO	GPIO
DSP_I2C7_SDA	0	DSP_I2C7_SDA	-	IO	I2C7 SDA
	1	DSP_GPIO0_PIN01	IO	IO	GPIO
DSP_I2C7_SCL	0	DSP_I2C7_SCL	-	IO	I2C7 SCL
	1	DSP_GPIO0_PIN00	IO	IO	GPIO
DSP_PDM_IN0	0	DSP_PDM_IN0	-	IO	Digital Microphone PDM[0] data input
	1	DSP_GPIO0_PIN15	IO	IO	GPIO
DSP_PDM_IN1	0	DSP_PDM_IN1	-	IO	Digital Microphone PDM[1] data input
	1	DSP_GPIO0_PIN16	IO	IO	GPIO
DSP_PDM_IN2	0	DSP_PDM_IN2	-	IO	Digital Microphone PDM[2] data input
	1	DSP_GPIO0_PIN17	IO	IO	GPIO
DSP_PDM_IN3	0	DSP_PDM_IN3	-	IO	Digital Microphone PDM[3] data input
	1	DSP_GPIO0_PIN18	IO	IO	GPIO
DSP_PDM_CKO	0	DSP_PDM_CKO	-	IO	Digital Microphone PDM clock output
	1	DSP_GPIO0_PIN14	IO	IO	GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
LSIO_UART7_RXD	0	LSIO_UART7_RXD	-	IO	UART7 RX data input
	2	LSIO_GPIO0_PIN00	IO	IO	GPIO
LSIO_UART7_TXD	0	LSIO_UART7_TXD	-	IO	UART7 TX data output
	2	LSIO_GPIO0_PIN01	IO	IO	GPIO
LSIO_UART7_CTS_N	0	LSIO_UART7_CTS_N	-		UART7 Modem control line CTS_N
	1	UART6_RXD	-		UART6 RX data input
	2	LSIO_GPIO0_PIN02	IO	IO	GPIO
LSIO_UART7_RTS_N	0	LSIO_UART7_RTS_N	-		UART7 Modem control line RTS_N
	1	UART6_TXD	-		UART6 TX data output
	2	LSIO_GPIO0_PIN03	IO	IO	GPIO
LSIO_UART1_RXD	0	LSIO_UART1_RXD	-		UART1 RX data input
	2	LSIO_GPIO0_PIN04	IO	IO	GPIO
LSIO_UART1_TXD	0	LSIO_UART1_TXD	-		UART1 TX data output
	2	LSIO_GPIO0_PIN05	IO	IO	GPIO
LSIO_UART1_CTS_N	0	LSIO_UART1_CTS_N	-		UART0 Modem control line CTS_N
	2	LSIO_GPIO0_PIN06	IO	IO	GPIO
LSIO_UART1_RTS_N	0	LSIO_UART1_RTS_N	-		UART0 Modem control line RTS_N
	2	LSIO_GPIO0_PIN07	IO	IO	GPIO
LSIO_UART2_RXD	0	LSIO_UART2_RXD	-		UART2 RX data input
	2	LSIO_GPIO0_PIN08	IO	IO	GPIO
LSIO_UART2_TXD	0	LSIO_UART2_TXD	-		UART2 TX data output
	2	LSIO_GPIO0_PIN09	IO	IO	GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
LSIO_UART3_RXD	0	LSIO_UART3_RXD	-		UART3 RX data input
	1	LSIO_I2C5_SCL	-		I2C5 SCL
	2	LSIO_GPIO0_PIN10	IO	IO	GPIO
LSIO_UART3_TXD	0	LSIO_UART3_TXD	-		UART3 TX data output
	1	LSIO_I2C5_SDA	-		I2C5 SDA
	2	LSIO_GPIO0_PIN11	IO	IO	GPIO
LSIO_UART4_RXD	0	LSIO_UART4_RXD	-		UART4 RX data input
	2	LSIO_GPIO0_PIN12	IO	IO	GPIO
LSIO_UART4_TXD	0	LSIO_UART4_TXD	-		UART4 TX data output
	2	LSIO_GPIO0_PIN13	IO	IO	GPIO
LSIO_SPI0_SCLK	0	LSIO_SPI0_SCLK	-		SPI0 master clock output SPI0 slave clock input
	2	LSIO_GPIO0_PIN14	IO	IO	GPIO
LSIO_SPI0_SSN	0	LSIO_SPI0_SSN	-		SPI6 master chip select output SPI6 slave chip select input
	2	LSIO_GPIO1_PIN04	IO	IO	GPIO
LSIO_SPI0_MISO	0	LSIO_SPI0_MISO	-		SPI0 master data input SPI0 slave data output
	2	LSIO_GPIO1_PIN05	IO	IO	GPIO
LSIO_SPI0_MOSI	0	LSIO_SPI0_MOSI	-		SPI0 master data output SPI0 slave data input
	2	LSIO_GPIO1_PIN06	IO	IO	GPIO
LSIO_SPI1_SCLK	0	LSIO_SPI1_SCLK	-		SPI1 master clock output SPI1 slave clock input
	1	LSIO_GPIO0_PIN16	-		GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
	2	JTG_TCK	IO	IO	JTAG clok input
LSIO_SPI1_SSN	0	LSIO_SPI1_SSN	-		SPI1 master chip select 0 output SPI1 slave chip select 0 input
	1	LSIO_GPIO0_PIN17	-		GPIO
	2	JTG_TRSTN	IO	IO	JTAG reset input, active low
LSIO_SPI1_SSN_1	0	LSIO_SPI1_SSN_1	-		SPI1 master chip select 1 output SPI1 slave chip select 1 input
	1	LSIO_GPIO0_PIN15	-		GPIO
	2	JTG_TMS	IO	IO	JTAG mode selection
LSIO_SPI1_MISO	0	LSIO_SPI1_MISO	-		SPI1 master data input SPI1 slave data output
	1	LSIO_GPIO0_PIN18	-		GPIO
	2	JTG_TDI	IO	IO	JTAG data input
LSIO_SPI1_MOSI	0	LSIO_SPI1_MOSI	-		SPI1 master data output SPI1 slave data input
	1	LSIO_GPIO0_PIN19	-		GPIO
	2	JTG_TDO	IO	IO	JTAG data output
LSIO_SPI2_SCLK	0	LSIO_SPI2_SCLK	-		SPI2 master clock output SPI2 slave clock input
	1	LSIO_GPIO0_PIN20	IO	IO	GPIO
	3	LSIO_PWM_OUT0	-		PWM0 output
LSIO_SPI2_SSN	0	LSIO_SPI2_SSN	-		SPI2 master chip select output SPI2 slave chip select input
	1	LSIO_GPIO0_PIN21	IO	IO	GPIO
	3	LSIO_PWM_OUT1	-		PMW1 output
LSIO_SPI2_MISO	0	LSIO_SPI2_MISO	-		SPI2 master data input SPI2 slave data output
	1	LSIO_GPIO0_PIN2	IO	IO	GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
		2			
	3	LSIO_PWM_OUT2	-		PWM2 output
LSIO_SPI2_MOSI	0	LSIO_SPI2_MOSI	-		SPI2 master data output SPI2 slave data input
	1	LSIO_GPIO0_PIN23	IO	IO	GPIO
	3	LSIO_PWM_OUT3	-		PWM3 output
LSIO_SPI3_SCLK	0	LSIO_SPI3_SCLK	-		SPI3 master clock output SPI3 slave clock input
	1	LSIO_GPIO0_PIN24	IO	IO	GPIO
	2	LSIO_LPWM_IO4	-		PMW4 output
	3	LSIO_SENSOR0_MCLK	-		Sensor0 MCLK output
LSIO_SPI3_SSN	0	LSIO_SPI3_SSN	-		SPI3 master clock output SPI3 slave clock input
	1	LSIO_GPIO0_PIN25	IO	IO	GPIO
	2	LSIO_LPWM_IO5	-		Lite PWM5 output
	3	LSIO_SENSOR1_MCLK	-		Sensor1 MCLK output
LSIO_SPI3_MISO	0	LSIO_SPI3_MISO	-		SPI3 master data input SPI3 slave data output
	1	LSIO_GPIO0_PIN26	IO	IO	GPIO
	2	LSIO_LPWM_IO6	-		Lite PWM6 output
	3	LSIO_SENSOR2_MCLK	-		Sensor2 MCLK output
LSIO_SPI3_MOSI	0	LSIO_SPI3_MOSI	-		SPI3 master data output SPI3 slave data input
	1	LSIO_GPIO0_PIN27	IO	IO	GPIO
	2	LSIO_LPWM_IO7	-		Lite PWM7 output
	3	LSIO_SENSOR3_	-		Sensor3 MCLK output

Pin Name	Mux	Functions	Default Dir	Dir	Description
		MCLK			
LSIO_SPI4_SCLK	0	LSIO_SPI4_SCLK	-		SPI4 master clock output SPI4 slave clock input
	1	LSIO_GPIO0_PIN28	IO	IO	GPIO
	2	UART5_RXD	-		UART5 RX data input
LSIO_SPI4_SSN	0	LSIO_SPI4_SSN	-		SPI4 master chip select output SPI4 slave chip select input
	1	LSIO_GPIO0_PIN29	IO	IO	GPIO
	2	UART5_TXD	-		UART5 TX data output
LSIO_SPI4_MISO	0	LSIO_SPI4_MISO	-		SPI4 master data input SPI4 slave data output
	1	LSIO_GPIO0_PIN30	IO	IO	GPIO
	2	I2C6_SCL	-		I2C6 SCL
LSIO_SPI4_MOSI	0	LSIO_SPI4_MOSI	-		SPI4 master data output SPI4 slave data input
	1	LSIO_GPIO0_PIN31	IO	IO	GPIO
	2	I2C6_SDA	-		I2C6 SDA
LSIO_SPI5_SCLK	0	LSIO_SPI5_SCLK	-		SPI5 master clock output SPI5 slave clock input
	1	LSIO_GPIO1_PIN00	IO	IO	GPIO
	2	LSIO_LPWM_IO0	-		Lite PWM0 output
LSIO_SPI5_SSN	0	LSIO_SPI5_SSN	-		SPI5 master chip select output SPI5 slave chip select input
	1	LSIO_GPIO1_PIN01	IO	IO	GPIO
	2	LSIO_LPWM_IO1	-		Lite PWM1 output
LSIO_SPI5_MISO	0	LSIO_SPI5_MISO	-		SPI5 master data input SPI5 slave data output
	1	LSIO_GPIO1_PIN0	IO	IO	GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
		2			
	2	LSIO_LPWM_IO2	-		Lite PWM2 output
LSIO_SPI5_MOSI	0	LSIO_SPI5_MOSI	-		SPI5 master data output SPI5 slave data input
	1	LSIO_GPIO1_PIN03	IO	IO	GPIO
	2	LSIO_LPWM_IO3	-		Lite PWM3 output
LSIO_I2C0_SCL	0	LSIO_I2C0_SCL	-		I2C0 SCL
	1	LSIO_GPIO1_PIN07	IO	IO	GPIO
	3	LSIO_PWM_OUT4	-		Lite PWM4 output
LSIO_I2C0_SDA	0	LSIO_I2C0_SDA	-		I2C0 SDA
	1	LSIO_GPIO1_PIN08	IO	IO	GPIO
	3	LSIO_PWM_OUT5	-		Lite PWM5 output
LSIO_I2C1_SCL	0	LSIO_I2C1_SCL	-		I2C1 SCL
	1	LSIO_GPIO1_PIN09	IO	IO	GPIO
	2	TIME_SYNC1	-		Time sync1 for LPWM or SIF
	3	LSIO_PWM_OUT6	-		PWM6 output
LSIO_I2C1_SDA	0	LSIO_I2C1_SDA	-		I2C1 SDA
	1	LSIO_GPIO1_PIN10	IO	IO	GPIO
	2	TIME_SYNC2	-		Time sync2 for LPWM or SIF
	3	LSIO_PWM_OUT7	-		PWM7 output
LSIO_I2C2_SCL	0	LSIO_I2C2_SCL	-		I2C2 SCL
	1	LSIO_GPIO1_PIN11	IO	IO	GPIO
LSIO_I2C2_SDA	0	LSIO_I2C2_SDA	-		I2C2 SDA
	1	LSIO_GPIO1_PIN12	IO	IO	GPIO
LSIO_I2C3_SCL	0	LSIO_I2C3_SCL	-		I2C3 SCL
	1	LSIO_GPIO1_PIN13	IO	IO	GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
LSIO_I2C3_SDA	0	LSIO_I2C3_SDA	-		I2C3 SDA
	1	LSIO_GPIO1_PIN14	IO	IO	GPIO
LSIO_I2C4_SCL	0	LSIO_I2C4_SCL	-		I2C4 SCL
	1	LSIO_GPIO1_PIN15	IO	IO	GPIO
	2	TIME_SYNC3	-		Time sync3 for LPWM or SIF
	3	DISP_TE	-		MIPI DSI Tearing Effect
LSIO_I2C4_SDA	0	LSIO_I2C4_SDA	-		I2C4 SDA
	1	LSIO_GPIO1_PIN16	IO	IO	GPIO
	2	TIME_SYNC4	-		Time sync4 for LPWM or SIF
BT1120_O_DATA0	0	BOOT_STRAP_PIN0	IO	IO	BOOT STAP PIN0
	1	BT1120_O_DATA0	-		BT1120 data0
BT1120_O_DATA1	0	BOOT_STRAP_PIN1	IO	IO	BOOT STAP PIN1
	1	BT1120_O_DATA1	-		BT1120 DATA1
BT1120_O_DATA2	0	BOOT_STRAP_PIN2	IO	IO	BOOT STAP PIN2
	1	BT1120_O_DATA2	-		BT1120 DATA2
BT1120_O_DATA3	0	BOOT_STRAP_PIN3	IO	IO	BOOT STAP PIN3
	1	BT1120_O_DATA3	-		BT1120 DATA3
BT1120_O_DATA4	0	BOOT_STRAP_PIN4	IO	IO	BOOT STAP PIN4
	1	BT1120_O_DATA0	-		BT1120 DATA0
BT1120_O_DATA5	0	BOOT_STRAP_PIN5	IO	IO	BOOT STAP PIN5
	1	BT1120_O_DATA5	-		BT1120 DATA5
BT1120_O_DATA6	0	BOOT_STRAP_PIN6	IO	IO	BOOT STAP PIN6
	1	BT1120_O_DATA6	-		BT1120 DATA6
BT1120_O_DATA7	0	BOOT_STRAP_PIN7	IO	IO	BOOT STAP PIN7

Pin Name	Mux	Functions	Default Dir	Dir	Description
	1	BT1120_O_DATA7	-		BT1120 DATA7
BT1120_O_DATA8	0	BOOT_STRAP_PIN8	IO	IO	BOOT STAP PIN8
	1	BT1120_O_DATA8	-		BT1120 DATA8
BT1120_O_DATA9	0	BOOT_STRAP_PIN9	IO	IO	BOOT STAP PIN9
	1	BT1120_O_DATA9	-		BT1120 DATA9
BT1120_O_DATA10	0	BOOT_STRAP_PIN10	IO	IO	BOOT STAP PIN10
	1	BT1120_O_DATA10	-		BT1120 DATA10
BT1120_O_DATA11	0	BOOT_STRAP_PIN11	IO	IO	BOOT STAP PIN11
	1	BT1120_O_DATA11	-		BT1120 DATA11
BT1120_O_DATA12	0	BOOT_STRAP_PIN12	IO	IO	BOOT STAP PIN12
	1	BT1120_O_DATA12	-		BT1120 DATA12
BT1120_O_DATA13	0	BOOT_STRAP_PIN13	IO	IO	BOOT STAP PIN13
	1	BT1120_O_DATA13	-		BT1120 DATA13
BT1120_O_DATA14	0	BOOT_STRAP_PIN14	IO	IO	BOOT STAP PIN14
	1	BT1120_O_DATA14	-		BT1120 DATA14
BT1120_O_DATA15	0	BOOT_STRAP_PIN15	IO	IO	BOOT STAP PIN15
	1	BT1120_O_DATA15	-		BT1120 DATA15
BT1120_O_PIXELCLK	0	BOOT_STRAP_PIN16	IO	IO	BOOT STAP PIN16
	1	BT1120_O_DATA16	-		BT1120 DATA16
HSIO_ENET_MD	0	HSIO_ENET_MDC	-		ENET MDC

Pin Name	Mux	Functions	Default Dir	Dir	Description
C	2	HSIO_GPIO0_PIN00	IO	IO	GPIO
HSIO_ENET_MDIO	0	HSIO_ENET_MDIO	-		ENET MDIO
	2	HSIO_GPIO0_PIN01	IO	IO	GPIO
HSIO_ENET_TXD_0	0	HSIO_ENET_TXD_0	-		ENET TX data0
	2	HSIO_GPIO0_PIN02	IO	IO	GPIO
HSIO_ENET_TXD_1	0	HSIO_ENET_TXD_1	-		ENET TX data1
	2	HSIO_GPIO0_PIN03	IO	IO	GPIO
HSIO_ENET_TXD_2	0	HSIO_ENET_TXD_2	-		ENET TX data2
	2	HSIO_GPIO0_PIN04	IO	IO	GPIO
HSIO_ENET_TXD_3	0	HSIO_ENET_TXD_3	-		ENET TX data3
	2	HSIO_GPIO0_PIN05	IO	IO	GPIO
HSIO_ENET_TXEN	0	HSIO_ENET_TXEN	-		ENET TXEN
	2	HSIO_GPIO0_PIN06	IO	IO	GPIO
HSIO_ENET_TX_CLK	0	HSIO_ENET_TX_CLK	-		ENET TX clock
	1	ENET_REF_CLK	-		ENET Reference clock
	2	HSIO_GPIO0_PIN07	IO	IO	GPIO
HSIO_ENET_RX_CLK	0	HSIO_ENET_RX_CLK	-	-	ENET RX clock
	2	HSIO_GPIO0_PIN08	IO	IO	GPIO
HSIO_ENET_RXD_0	0	HSIO_ENET_RXD_0	-		ENET RX data0

Pin Name	Mux	Functions	Default Dir	Dir	Description
	2	HSIO_GPIO0_PIN09	IO	IO	GPIO
HSIO_ENET_RXD_1	0	HSIO_ENET_RXD_1	-		ENET RX data1
	2	HSIO_GPIO0_PIN10	IO	IO	GPIO
HSIO_ENET_RXD_2	0	HSIO_ENET_RXD_2	-		ENET RX data2
	2	HSIO_GPIO0_PIN11	IO	IO	GPIO
HSIO_ENET_RXD_3	0	HSIO_ENET_RXD_3	-		ENET RX data3
	2	HSIO_GPIO0_PIN12	IO	IO	GPIO
HSIO_ENET_RXDV	0	HSIO_ENET_RXDV	-		ENET RX DV
	2	HSIO_GPIO0_PIN13	IO	IO	GPIO
HSIO_EPHY_CLK	0	HSIO_EPHY_CLK	-		ENET PHY clock
	1	HSIO_ENET_AUX_TRIG_0	-		ENET AUX trigger 0
	2	HSIO_GPIO0_PIN14	IO	IO	GPIO
HSIO_SD_WP	0	HSIO_SD_WP	IO	IO	SD Write Protect
	2	HSIO_GPIO0_PIN15	-		GPIO
HSIO_SD_SDCLK	0	HSIO_SD_SDCLK	IO	IO	SD Clock
	2	HSIO_GPIO0_PIN16	-		GPIO
HSIO_SD_CMD	0	HSIO_SD_CMD	IO	IO	SD Command
	2	HSIO_GPIO0_PIN17	-		GPIO
HSIO_SD_CDN	0	HSIO_SD_CDN	IO	IO	SD CDN
	2	HSIO_GPIO0_PIN18	-		GPIO
HSIO_SD_DAT0	0	HSIO_SD_DAT0	IO	IO	SD DATA0

Pin Name	Mux	Functions	Default Dir	Dir	Description
	2	HSIO_GPIO0_PIN 19	-		GPIO
HSIO_SD_DAT1	0	HSIO_SD_DAT1	IO	IO	SD DATA1
	2	HSIO_GPIO0_PIN 20	-		GPIO
HSIO_SD_DAT2	0	HSIO_SD_DAT2	IO	IO	SD DATA2
	2	HSIO_GPIO0_PIN 21	-		GPIO
HSIO_SD_DAT3	0	HSIO_SD_DAT3	IO	IO	SD DATA3
	2	HSIO_GPIO0_PIN 22	-		GPIO
HSIO_SDIO_WP	0	HSIO_SDIO_WP	-		SDIO Write Protect
	2	HSIO_GPIO0_PIN 23	IO	IO	GPIO
HSIO_SDIO_SDCLK	0	HSIO_SDIO_SDCLK	-		SDIO clock
	2	HSIO_GPIO0_PIN 24	IO	IO	GPIO
HSIO_SDIO_CMD	0	HSIO_SDIO_CMD	-		SDIO Command
	2	HSIO_GPIO0_PIN 25	IO	IO	GPIO
HSIO_SDIO_CDN	0	HSIO_SDIO_CDN	-		SDIO CDN
	2	HSIO_GPIO0_PIN 26	IO	IO	GPIO
HSIO_SDIO_DAT0	0	HSIO_SDIO_DAT0	-		SDIO DATA0
	2	HSIO_GPIO0_PIN 27	IO	IO	GPIO
HSIO_SDIO_DAT1	0	HSIO_SDIO_DAT1	-		SDIO DATA1
	1	HSIO_ENET_AUX_TRIG_1	-		Enet Aux Trig 1
	2	HSIO_GPIO0_PIN 28	IO	IO	GPIO
HSIO_SDIO_DAT2	0	HSIO_SDIO_DAT2	-		SDIO DATA2
	1	HSIO_ENET_AUX_TRIG_2	-		ENET AUX Trigger 2

Pin Name	Mux	Functions	Default Dir	Dir	Description
	2	HSIO_GPIO0_PIN29	IO	IO	GPIO
HSIO_SDIO_DAT3	0	HSIO_SDIO_DAT3	-		SDIO DATA3
	1	HSIO_ENET_AUX_TRIG_3	-		ENET AUX Trigger 3
	2	HSIO_GPIO0_PIN30	IO	IO	GPIO
HSIO_QSPI_SSN_0	0	HSIO_QSPI_SSN_0	IO	IO	QSPI SSN 0
	1	HSIO_GPIO1_PIN00	-		GPIO
HSIO_QSPI_SSN_1	0	HSIO_QSPI_SSN_1	IO	IO	QSPI SSN 1
	1	HSIO_GPIO1_PIN01	-		GPIO
HSIO_QSPI_SCLK	0	HSIO_QSPI_SCLK	IO	IO	QSPI clock
	1	HSIO_GPIO1_PIN02	-		GPIO
HSIO_QSPI_DATA_0	0	HSIO_QSPI_DATA_0	IO	IO	QSPI DATA 0
	1	HSIO_GPIO1_PIN03	-		GPIO
HSIO_QSPI_DATA_1	0	HSIO_QSPI_DATA_1	IO	IO	QSPI DATA 1
	1	HSIO_GPIO1_PIN04	-		GPIO
HSIO_QSPI_DATA_2	0	HSIO_QSPI_DATA_2	IO	IO	QSPI DATA 2
	1	HSIO_GPIO1_PIN05	-		GPIO
HSIO_QSPI_DATA_3	0	HSIO_QSPI_DATA_3	IO	IO	QSPI DATA 3
	1	HSIO_GPIO1_PIN06	-		GPIO
EMMC_SDCLK	0	EMMC_SDCLK	IO	IO	EMMC clock
	1	HSIO_GPIO1_PIN	-		GPIO

Pin Name	Mux	Functions	Default Dir	Dir	Description
		07			
EMMC_CMD	0	EMMC_CMD	IO	IO	EMMC Command
	1	HSIO_GPIO1_PIN 08	-		GPIO
EMMC_DAT0	0	EMMC_DAT0	IO	IO	EMMC DATA 0
	1	HSIO_GPIO1_PIN 09	-		GPIO
EMMC_DAT1	0	EMMC_DAT1	IO	IO	EMMC DATA 1
	1	HSIO_GPIO1_PIN 10	-		GPIO
EMMC_DAT2	0	EMMC_DAT2	IO	IO	EMMC DATA 2
	1	HSIO_GPIO1_PIN 11	-		GPIO
EMMC_DAT3	0	EMMC_DAT3	IO	IO	EMMC DATA 3
	1	HSIO_GPIO1_PIN 12	-		GPIO
EMMC_DAT4	0	EMMC_DAT4	IO	IO	EMMC DATA 4
	1	HSIO_GPIO1_PIN 13	-		GPIO
EMMC_DAT5	0	EMMC_DAT5	IO	IO	EMMC DATA 5
	1	HSIO_GPIO1_PIN 14	-		GPIO
EMMC_DAT6	0	EMMC_DAT6	IO	IO	EMMC DATA 6
	1	HSIO_GPIO1_PIN 15	-		GPIO
EMMC_DAT7	0	EMMC_DAT7	IO	IO	EMMC DATA 7
	1	HSIO_GPIO1_PIN 16	-		GPIO
EMMC_RST_n	0	EMMC_RST_n	IO	IO	EMMC Reset_n
	1	HSIO_GPIO1_PIN 17	-		GPIO

(1) Mux = NA means no function mux for this pin.

(2) Mux = 0/1/2/3 means this pin function can be configured by PIN registers. The value is the function selection. Only listed values are legal.

(3) If GPIO is the default function, it is in input state.

3.2.3 Analog Pins

Table 3-6 Analog Pin List

Pin Name	Ball	Type	Description
MIPI CSI Host RX			
CSI_PHY0_CLKP	AC10	AI	MIPI CSI0 Positive D-PHY Differential Clock Line.
CSI_PHY0_CLKN	AD10	AI	MIPI CSI0 Negative D-PHY Differential Clock Line.
CSI_PHY0_DATAP0	AC8	AI	MIPI CSI0 Positive D-PHY Differential Data Line
CSI_PHY0_DATAP1	AC9	AI	MIPI CSI0 Positive D-PHY Differential Data Line
CSI_PHY0_DATAN0	AD8	AI	MIPI CSI0 Negative D-PHY Differential Data Line
CSI_PHY0_DATAN1	AD9	AI	MIPI CSI0 Negative D-PHY Differential Data Line
CSI_PHY1_CLKP	AC5	AI	MIPI CSI1 Positive D-PHY Differential Clock Line.
CSI_PHY1_CLKN	AD5	AI	MIPI CSI1 Negative D-PHY Differential Clock Line.
CSI_PHY1_DATAP0	AC7	AI	MIPI CSI1 Positive D-PHY Differential Data Line
CSI_PHY1_DATAP1	AC6	AI	MIPI CSI1 Positive D-PHY Differential Data Line
CSI_PHY1_DATAN0	AD7	AI	MIPI CSI1 Negative D-PHY Differential Data Line
CSI_PHY1_DATAN1	AD6	AI	MIPI CSI1 Negative D-PHY Differential Data Line
CSI_PHY2_CLKP	AC4	AI	MIPI CSI2 Positive D-PHY Differential Clock Line.
CSI_PHY2_CLKN	AD4	AI	MIPI CSI2 Negative D-PHY Differential Clock Line.
CSI_PHY2_DATAP0	AB2	AI	MIPI CSI2 Positive D-PHY Differential Data Line
CSI_PHY2_DATAP1	AC3	AI	MIPI CSI2 Positive D-PHY Differential Data Line

Pin Name	Ball	Type	Description
CSI_PHY2_DATAN0	AB1	AI	MIPI CSI2 Negative D-PHY Differential Data Line
CSI_PHY2_DATAN1	AD3	AI	MIPI CSI2 Negative D-PHY Differential Data Line
CSI_PHY3_CLKP	W2	AI	MIPI CSI3 Positive D-PHY Differential Clock Line.
CSI_PHY3_CLKN	W1	AI	MIPI CSI3 Negative D-PHY Differential Clock Line.
CSI_PHY3_DATAP0	AA2	AI	MIPI CSI3 Positive D-PHY Differential Data Line
CSI_PHY3_DATAP1	Y2	AI	MIPI CSI3 Positive D-PHY Differential Data Line
CSI_PHY3_DATAN0	AA1	AI	MIPI CSI3 Negative D-PHY Differential Data Line
CSI_PHY3_DATAN1	Y1	AI	MIPI CSI3 Negative D-PHY Differential Data Line
MIPI CSI Device TX			
DISP_DPHY_REXT	Y13	AIO	External Resistor Connection.
DISP_DPHY_DATAP0	AC17	AO	Positive D-PHY Differential Data Line.
DISP_DPHY_DATAP1	AC16	AO	Positive D-PHY Differential Data Line.
DISP_DPHY_DATAP2	AD14	AO	Positive D-PHY Differential Data Line.
DISP_DPHY_DATAP3	AD15	AO	Positive D-PHY Differential Data Line.
DISP_DPHY_DATAN0	AD17	AO	Negative D-PHY Differential Data Line.
DISP_DPHY_DATAN1	AD16	AO	Negative D-PHY Differential Data Line.
DISP_DPHY_DATAN2	AC14	AO	Negative D-PHY Differential Data Line.
DISP_DPHY_DATAN3	AC15	AO	Negative D-PHY Differential Data Line.
DISP_DPHY_CLKP	AD13	AO	Positive D-PHY Differential Clock Line.
DISP_DPHY_CLKN	AC13	AO	Negative D-PHY Differential Clock Line.
USB3.0			
USB3_RX0_P	A3	AI	USB 3.0 receive signal DP
USB3_RX0_M	B3	AI	USB 3.0 receive signal DM.
USB3_REF_CLK_P	A5	AI	Low-Swing Differential Input Clock Pair With Pad.
USB3_REF_CLK_M	B5	AI	Low-Swing Differential Input Clock Pair With Pad.

Pin Name	Ball	Type	Description
USB3_TX0_P	A4	AO	USB 3.0 transmission signal DP
USB3_TX0_M	B4	AO	USB 3.0 transmission signal DM
USB3_RESREF	C7	AIO	Reference Resistor Connection
USB3_VBUS0	B7	P	USB 5-V Power Supply Pin.
USB3_DP0	A6	AIO	USB2.0 data line DP
USB3_DM0	B6	AIO	USB2.0 data line DM
USB2.0			
USB2_VBUS0	A7	AI	USB 5-V Signal
USB2_TXRTUNE	D9	AI	Transmitter Resistor Tune Pin
USB2_DP0	A8	AI	USB2 D+ Signal
USB2_DM0	B8	AI	USB2 D- Signal
LPDDR4/LPDDR4x			
DRAM_BP_VREF	N22	AI	Voltage reference for receivers and analog test point for debug
DRAM_BP_DB0	D21	AI	LPDDR4/LPDDR4x DQA[0]
DRAM_BP_DB1	C22	AI	LPDDR4/LPDDR4X DQA[1]
DRAM_BP_DB2	E20	AI	LPDDR4/LPDDR4X DQA[2]
DRAM_BP_DB3	D20	AI	LPDDR4/LPDDR4X DQA[3]
DRAM_BP_DB4	A20	AI	LPDDR4/LPDDR4X DQA[4]
DRAM_BP_DB5	A19	AI	LPDDR4/LPDDR4X DQA[5]
DRAM_BP_DB6	C19	AI	LPDDR4/LPDDR4X DQA[6]
DRAM_BP_DB7	B19	AI	LPDDR4/LPDDR4X DQA[7]
DRAM_BP_DB8	C20	AI	DM/DBIA[0]
DRAM_BP_DB9	B21	AI	DQSA_T[0]
DRAM_BP_DB10	A21	AI	DQSA_C[0]
DRAM_BP_DB12	G24	AI	LPDDR4/LPDDR4X DQA[8]
DRAM_BP_DB13	F24	AI	LPDDR4/LPDDR4X DQA[9]
DRAM_BP_DB14	E23	AI	LPDDR4/LPDDR4X DQA[10]
DRAM_BP_DB15	D24	AI	LPDDR4/LPDDR4X DQA[11]
DRAM_BP_DB16	F23	AI	LPDDR4/LPDDR4X DQA[12]
DRAM_BP_DB17	A22	AI	LPDDR4/LPDDR4X DQA[13]
DRAM_BP_DB18	B23	AI	LPDDR4/LPDDR4X DQA[14]

Pin Name	Ball	Type	Description
DRAM_BP_DB19	B22	AI	LPDDR4/LPDDR4X DQA[15]
DRAM_BP_DB20	D23	AI	DM/DBIA[1]
DRAM_BP_DB21	C23	AI	DQSA_T[1]
DRAM_BP_DB22	C24	AI	DQSA_C[1]
DRAM_BP_DB24	AD22	AI	LPDDR4/LPDDR4X DQB[0]
DRAM_BP_DB25	AA24	AI	LPDDR4/LPDDR4X DQB[1]
DRAM_BP_DB26	AC22	AI	LPDDR4/LPDDR4X DQB[2]
DRAM_BP_DB27	AC23	AI	LPDDR4/LPDDR4X DQB[3]
DRAM_BP_DB28	V24	AI	LPDDR4/LPDDR4X DQB[4]
DRAM_BP_DB29	W23	AI	LPDDR4/LPDDR4X DQB[5]
DRAM_BP_DB30	Y23	AI	LPDDR4/LPDDR4X DQB[6]
DRAM_BP_DB31	W24	AI	LPDDR4/LPDDR4X DQB[7]
DRAM_BP_DB32	AA23	AI	LPDDR4/LPDDR4X DM/DBIB[0]
DRAM_BP_DB33	AB24	AI	LPDDR4/LPDDR4X DQSB_T[0]
DRAM_BP_DB34	AB23	AI	LPDDR4/LPDDR4X DQSB_C[0]
DRAM_BP_DB36	AA19	AI	LPDDR4/LPDDR4X DQB[8]
DRAM_BP_DB37	AC19	AI	LPDDR4/LPDDR4X DQB[9]
DRAM_BP_DB38	AD19	AI	LPDDR4/LPDDR4X DQB[10]
DRAM_BP_DB39	AC20	AI	LPDDR4/LPDDR4X DQB[11]
DRAM_BP_DB40	AA20	AI	LPDDR4/LPDDR4X DQB[12]
DRAM_BP_DB41	Y21	AI	LPDDR4/LPDDR4X DQB[13]
DRAM_BP_DB42	AA21	AI	LPDDR4/LPDDR4X DQB[14]
DRAM_BP_DB43	AB22	AI	LPDDR4/LPDDR4X DQB[15]
DRAM_BP_DB44	AB20	AI	LPDDR4/LPDDR4X DM/DBIB[1]
DRAM_BP_DB45	AD21	AI	LPDDR4/LPDDR4X DQSB_T[1]
DRAM_BP_DB46	AC21	AI	LPDDR4/LPDDR4X DQSB_C[1]
DRAM_BP_MEMRESET_L	M22	AI	LPDDR4/LPDDR4X DRAM reset
DRAM_BP_AC0	K24	AI	LPDDR4/LPDDR4X CKEA0
DRAM_BP_AC1	L23	AI	LPDDR4/LPDDR4X CKEA1
DRAM_BP_AC2	K23	AI	LPDDR4/LPDDR4X CSA0
DRAM_BP_AC3	L22	AI	LPDDR4/LPDDR4X CSA1
DRAM_BP_AC4	J24	AI	LPDDR4/LPDDR4X CLKA_T

Pin Name	Ball	Type	Description
DRAM_BP_AC5	J23	AI	LPDDR4/LPDDR4X CLKA_C
DRAM_BP_AC8	G22	AI	LPDDR4/LPDDR4X CAA0
DRAM_BP_AC9	M23	AI	LPDDR4/LPDDR4X CAA1
DRAM_BP_AC10	H23	AI	LPDDR4/LPDDR4X CAA2
DRAM_BP_AC11	F22	AI	LPDDR4/LPDDR4X CAA3
DRAM_BP_AC12	M24	AI	LPDDR4/LPDDR4X CAA4
DRAM_BP_AC13	G23	AI	LPDDR4/LPDDR4X CAA5
DRAM_BP_AC19	H22	AI	Primary Digital Observation Pin
DRAM_BP_AC20	R23	AI	LPDDR4/LPDDR4X CKEB0
DRAM_BP_AC21	R22	AI	LPDDR4/LPDDR4X CKEB1
DRAM_BP_AC22	R24	AI	LPDDR4/LPDDR4X CSB0
DRAM_BP_AC23	P23	AI	LPDDR4/LPDDR4X CSB1
DRAM_BP_AC24	T24	AI	LPDDR4/LPDDR4X CLKB_T
DRAM_BP_AC25	T23	AI	LPDDR4/LPDDR4X CLKB_C
DRAM_BP_AC28	N24	AI	LPDDR4/LPDDR4X CAB0
DRAM_BP_AC29	W22	AI	LPDDR4/LPDDR4X CAB1
DRAM_BP_AC30	V23	AI	LPDDR4/LPDDR4X CAB2
DRAM_BP_AC31	N23	AI	LPDDR4/LPDDR4X CAB3
DRAM_BP_AC32	U23	AI	LPDDR4/LPDDR4X CAB4
DRAM_BP_AC33	V22	AI	LPDDR4/LPDDR4X CAB5
DRAM_BP_ZN	K22	AI	Calibration Resistor Connection Bump
ADC			
ADC_VINS[0]	AB18	AI	Single-end analog input signal[0]
ADC_VINS[1]	Y19	AI	Single-end analog input signal[1]
ADC_VINS[2]	AA17	AI	Single-end analog input signal[2]
ADC_VINS[3]	AB17	AI	Single-end analog input signal[3]
ADC_VINS[4]	AC18	AI	Single-end analog input signal[4]
ADC_VINS[5]	AA16	AI	Single-end analog input signal[5]
ADC_VINS[6]	AB16	AI	Single-end analog input signal[6]
ADC_VINS[7]	AB15	AI	Single-end analog input signal[7]
ADC_VREFN	Y18	AI	Negative reference voltage
ADC_VREFP	Y17	AI	Positive reference voltage

Pin Name	Ball	Type	Description
ADC_ATSTP(ADC_REXT)	Y15	AI	External resistor connection pin

4 Electrical Specification

4.1 Recommended Operating Condition

Table 4-1 summarizes the recommended operating conditions for the power supply under normal voltage.

Table 4-1 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
Digital Core Power					
VDD08_AON	Always on domain core power	0.72	0.8	0.88	V
VDD08_BPU	BPU domain core power	0.75	0.8	0.88	V
VDD08_CPU	CPU domain core power*	0.90 0.77	1.0 0.85	1.05 0.94	V
VDD08_DDR	DDR domain core power	0.75	0.8	0.88	V
VDD08_DSP	DSP domain core power	0.72	0.8	0.88	V
VDD08_GPU	GPU domain core power	0.75	0.8	0.88	V
VDD08_SOC	TOP domain core power	0.75	0.8	0.88	V
Digital IO Power					
VDDPST18_AON_IO	AON subsystem IO power domain	1.62	1.8	1.98	V
VDDPST18_DSP_IO	DSP subsystem IO power domain	1.62	1.8	1.98	V
VDDPST18_QSPI	QSPI IO power domain	1.62	1.8	1.98	V
VDDPST18_GPIO1	SPI0/SPI1/SPI3/SPI4/SPI5 IO power domain	1.62	1.8	1.98	V
VDDPST33_EMMC	EMMC IO power domain	1.62	1.8	1.98	V
VDDPST33_HS_SDIO	SDIO IO power domain in 1.8V mode	1.62	1.8	1.98	V
	SDIO IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_SD	SD card IO power domain in 1.8V mode	1.62	1.8	1.98	V
	SD card IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_ENET	Ethernet IO power domain in 1.8V mode	1.62	1.8	1.98	V
	Ethernet IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_DSP_SDIO	DSP subsystem IO power domain	1.62	1.8	1.98	V

Symbol	Description	Min	Typ	Max	Unit
	in 1.8V mode				
	DSP subsystem IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_SDIO9	UART0(4-wire) IO power domain in 1.8V mode	1.62	1.8	1.98	V
	UART0(4-wire) IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_SDIO8	UART1(4-wire) IO power domain in 1.8V mode	1.62	1.8	1.98	V
	UART1(4-wire) IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_SDIO7	UART2/UART3/UART4 IO power domain in 1.8V mode	1.62	1.8	1.98	V
	UART2/UART3/UART4 IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_SDIO6	I2C0/I2C1 IO power domain in 1.8V mode	1.62	1.8	1.98	V
	I2C0/I2C1 IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_SDIO5	SPI2 IO power domain in 1.8V mode	1.62	1.8	1.98	V
	SPI2 IO power domain in 3.3V mode	2.7	3.3	3.465	V
VDDPST33_BT1120	BT1120 IO power domain in 1.8V mode	1.62	1.8	1.98	V
	BT1120 IO power domain in 3.3V mode	2.7	3.3	3.465	V
Analog Power					
AVDD33_USB2_VDD330	USB2 PHY 3.3V Analog power	3.07	3.3	3.63	V
AVDD18_USB2_VDDH0	USB2 PHY regulator power	1.68	1.8	1.98	V
		3.07	3.3	3.63	V
DVDD08_USB2_DVDD	USB2 PHY digital power	0.75	0.8	0.88	V
AVDD33_USB3	USB3 PHY high-voltage power	3.07	3.3	3.63	V
DVDD08_USB3_DVDD	USB3 PHY analog and digital low-voltage power	0.75	0.8	0.88	V
DVDD08_USB3_VP	USB3 PHY analog and digital low-voltage power	0.75	0.8	0.88	V

Symbol	Description	Min	Typ	Max	Unit
AVDD18_PLL_DSP	PLL 1.8V analog power in the DSP subsystem	1.62	1.8	1.98	V
AVDD08_PLL_DSP	PLL 0.8V analog power in the DSP subsystem	0.72	0.8	0.88	V
AVDD18_PLL_DDR	PLL 1.8V analog power in the DDR subsystem	1.62	1.8	1.98	V
AVDD08_PLL_DDR	PLL 0.8V analog power in the DDR subsystem	0.72	0.8	0.88	V
AVDD18_PLL	PLL 1.8V analog power in the TOP subsystem	1.62	1.8	1.98	V
AVDD08_PLL	PLL 0.8V analog power in the TOP subsystem	0.72	0.8	0.88	V
AVDD08_VP_MIPI_RX	MIPI RX PHY 0.8V Analog power	0.75	0.8	0.88	V
AVDD18_VPH_MIPI_RX	MIPI RX PHY 1.8V Analog power	1.68	1.8	1.98	V
AVDD08_VP_MIPI_TX	MIPI TX PHY 0.8V Analog power	0.75	0.8	0.88	V
AVDD18_VPH_MIPI_TX	MIPI TX PHY 1.8V Analog power	1.68	1.8	1.98	V
VDDA18_DDR_PHY	DDR PHY 1.8V Analog power	1.68	1.8	1.98	V
VDDQ_DDR	DDR PHY VDDQ I/O power (LPDDR4)	1.06	1.1	1.17	V
	DDR PHY VDDQ I/O power (LPDDR4x)	1.06	1.1	1.17	V
VDDQ_DDR_LP	DDR PHY VDDQLP I/O power (LPDDR4)	1.06	1.1	1.17	V
	DDR PHY VDDQLP I/O power (LPDDR4x)	0.57	0.6	0.65	V
AVDD18_VT	Voltage sensor 1.8V analog power	1.62	1.8	1.98	V
AVDD18_TS_BPU	BPU TS 1.8V analog power	1.62	1.8	1.98	V
AVDD18_TS_DDR	DDR TS 1.8V analog power	1.62	1.8	1.98	V
AVDD18_ADC	ADC 1.8V analog power	1.62	1.8	1.98	V
VQPS_EFUSE	EFUSE programming power	1.71	1.8	1.89	V
Ground					
VSS	Digital ground	-	0	-	V
AVSS_PLL_DSP	Analog ground of PLL in the DSP subsystem	-	0	-	V
AVSS_PLL_DDR	Analog ground of PLL in the DDR subsystem	-	0	-	V
AVSS_PLL	Analog ground of PLLs	-	0	-	V

Symbol	Description	Min	Typ	Max	Unit
AVSS_ADC	Analog ground of ADC	-	0	-	V

Note: The typical voltage of X5H VDD08_CPU is 1.0V, and then the typical voltage of X5M VDD08_CPU is 0.85V.

4.2 Electrostatic Discharge (ESD) Ratings

Table 4-2 summarizes the ESD ratings of the X5.

Table 4-2 ESD Ratings

Symbol	Description	Value	Unit
HBM	Human-Body model (HBM)	2000	V
CDM	Charged-device model (CDM)	250	V

4.3 Digital General IO Electrical Parameters

Table 4-3 summarizes the digital general IO electrical characteristics.

Table 4-3 Digital General IO Electrical Parameters

Symbol	Description	Drive Strength	Min	Typ	Max	Unit
VDDIO	Interface voltage	-	1.62	1.8	1.98	V
V_{IL}	Input Low Voltage	-	-0.3	-	0.35*VDDIO	V
V_{IH}	Input High Voltage	-	0.65*VDDIO	-	VDDIO+0.3	V
V_T	Threshold Point	-	0.83	0.91	1.01	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	-	0.99	1.09	1.21	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	-	0.74	0.82	0.9	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	-	0.82	0.91	1	V
V_{TPU+}	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	0.98	1.08	1.2	V
V_{TPU-}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	0.73	0.81	0.89	V

Symbol	Description	Drive Strength	Min	Typ	Max	Unit
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	-	0.84	0.92	1.02	V
V_{TPD+}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	1	1.1	1.22	V
V_{TPD-}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	0.75	0.83	0.91	V
V_{TSPU}	Threshold Point with Strong Pull-up Resistor Enabled	-	0.78	0.86	0.94	V
V_{TSPU+}	Schmitt Trigger Low to High Threshold Point with Strong Pull-up Resistor Enabled	-	0.95	1.04	1.15	V
V_{TSPU-}	Schmitt Trigger High to Low Threshold Point with Strong Pull-up Resistor Enabled	-	0.68	0.76	0.83	V
I	Input Leakage Current@ V_I=1.8V or 0V	-	-	-	±10μ	A
I_{OZ}	Tri-state Output Leakage Current @V_O=1.8V or 0V		-	-	±10μ	A
R_{SPU}	Strong Pull-up Resistor	-	2.8k	3.7k	4.5k	Ω
R_{PU}	Pull-up Resistor	-	18k	28k	38k	Ω
R_{PD}	Pull-down Resistor	-	17k	25k	33k	Ω
V_{OL}	Output Low Voltage	-	-	-	0.45	V
V_{OH}	Output High Voltage	-	1.35	-	-	V
I_{OL}	I_{OL} Low Level Output Current @V_{OL}(max)	02	6.6	8.7	12.8	mA
		04	12.2	16.1	24	mA
		06	15.7	20.7	31.1	mA
		08	23.1	30.4	46.2	mA
I_{OH}	I_{OH} High Level Output Current @V_{OH}(max)	02	5.5	7.4	11.6	mA
		04	10.2	13.7	21.6	mA
		06	13.1	17.6	27.9	mA
		08	19.2	25.8	41.4	mA

4.4 24M OSC IO Electrical Parameters

Table 4-4 lists the 24M oscillator (OSC) IO electrical parameters.

Table 4-4 24M OSC IO Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Freq	Frequency	-	24	-	MHz
Duty	Duty cycle	40	50	60	%
ESR	Crystal maximum ESR			40	Ω

4.5 32K Input Electrical Parameters

Table 4-5 lists the 32K input electrical parameters.

Table 4-5 32K Input Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Freq	Frequency	-	32768	-	Hz
Duty	Duty cycle	40	50	60	%

4.6 SDIO Electrical Parameters

Table 4-6 summarize the SD special IO electrical characteristics (1.8V).

Table 4-6 SDIO Electrical Parameters (1.8V)

Symbol	Description	Drive Strength	Min	Typ	Max	Unit
VDDIO	Interface voltage	-	1.62	1.8	1.98	V
V_{IL}	Input Low Voltage	-	-0.3		0.58	V
V_{IH}	Input High Voltage	-	1.27		1.98	V
V_T	Threshold Point	-	0.84	0.93	1.02	V
V_{T+}	Schmitt Trigger Low to High Threshold Point		0.98	1.08	1.19	V
V_{T-}	Schmitt Trigger High to Low Threshold Point		0.71	0.8	0.88	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled		0.84	0.92	1.01	V
V_{TPU+}	Schmitt Trigger Low to High		0.98	1.08	1.18	V

Symbol	Description	Drive Strength	Min	Typ	Max	Unit
	Threshold Point with Pull-up Resistor Enabled					
V_{TPU-}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled		0.7	0.79	0.87	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled		0.85	0.94	1.03	V
V_{TPD+}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled		0.99	1.1	1.2	V
V_{TPD-}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled		0.72	0.8	0.89	V
I_I	Input Leakage Current@ V_I=1.8V or 0V				±10μ	A
I_{OZ}	Tri-state Output Leakage Current @V_O=1.8V or 0V				±10μ	A
R_{SPU}	Strong Pull-up Resistor			-		Ω
R_{PU}	Pull-up Resistor		29k	35k	45k	Ω
R_{PD}	Pull-down Resistor		24k	28k	33k	Ω
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		1.4			V
I_{OL}	I_{OL} Low Level Output Current @V_{OL}(max)	02	8.1	12.5	17.1	mA
		04	12.1	18.7	25.7	mA
		06	16.1	24.9	34.2	mA
		08	20.1	31	42.7	mA
I_{OH}	I_{OH} High Level Output Current @V_{OH}(max)	02	3.7	10.1	19.8	mA
		04	5.6	15.2	29.7	mA
		06	7.4	20.2	39.5	mA
		08	9.3	25.2	49.3	mA

Table 4-7 summarizes the SD special IO electrical characteristics (3.3V).

Table 4-7 SDIO Electrical Parameters (3.3V)

Symbol	Description	Drive Strength	Min	Typ	Max	Unit
VDDIO	Interface voltage	-	3.135	3.3	3.465	V
V_{IL}	Input Low Voltage	-	-0.3		0.25*VDDIO	V
V_{IH}	Input High Voltage	-	0.625*VDDIO		3.465	V
V_T	Threshold Point	-	0.88	1.05	1.31	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	-	1	1.16	1.41	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	-	0.73	0.89	1.14	V
V_{TPU}	Threshold Point with Pull-up Resistor Enabled	-	0.87	1.03	1.29	V
V_{TPU+}	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	0.99	1.14	1.39	V
V_{TPU-}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	0.71	0.88	1.12	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	-	0.89	1.14	1.39	V
V_{TPD+}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	1.01	1.17	1.42	V
V_{TPD-}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	0.73	0.9	1.15	V
I_I	Input Leakage Current@ V_I=1.8V or 0V	-			±10μ	A
I_{OZ}	Tri-state Output Leakage Current @V_O=1.8V or 0V	-			±10μ	A
R_{PU}	Pull-up Resistor	-	31k	42k	66k	Ω
R_{PD}	Pull-down Resistor	-	24k	29k	33k	Ω
V_{OL}	Output Low Voltage	-	-	-	0.125*VDDIO	V
V_{OH}	Output High Voltage	-	0.75*VDDIO	-	-	V
I_{OL}	I_{OL} Low Level Output Current @V_{OL}(max)	02	5.0	8.7	14.7	mA
		04	7.5	13	22.1	mA

Symbol	Description	Drive Strength	Min	Typ	Max	Unit
		06	10.0	17.4	29.4	mA
		08	12.5	21.7	36.7	mA
I_{OH}	I_{OH} High Level Output Current @V_{OH}(max)	02	6.9	12.3	21.5	mA
		04	10.3	18.5	32.2	mA
		06	13.8	24.7	42.9	mA
		08	17.2	30.8	53.6	mA

4.7 DDR Electrical Parameters

Table 4-8 summarizes the DDR IO DC/AC electrical characteristics in LPDDR4/LPDDR4x mode.

Table 4-8 LPDDR4/LPDDR4x Mode DDR DC/AC Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
V_{ref}	Reference voltage	-	Variable	-	V
$V_{refDC-err}$	DC reference voltage error	-0.75%	-	0.75%	VDDQ
$V_{refAC-err}$	AC Reference voltage error	-0.25%	-	0.25%	VDDQ
I_{IZ}	V_{ref} input leakage current	-	-	50	uA
I_{IZ}	BP_DAT input leakage current	-	-	50	uA
V_{IH-DC}	Input high voltage for BP_DAT*	V_{ref} + 0.02	-	-	V
V_{IL-DC}	Input low voltage for BP_DAT*	-	-	V_{ref} - 0.02	V
$V_{IH-ACLS}$	Low-speed Input high voltage for BP_DAT (logic 1)	V_{ref} + 0.070	-	VDDQ + 0.15	V
$V_{IL-ACLS}$	Low-speed Input low voltage for BP_DAT (logic 0)	–0.15	-	V_{ref} - 0.070	V
$V_{IH-ACHS}$	High-speed input high voltage for BP_DAT (logic 1)	V_{ref} + 0.070	-	V_{ref} + 0.440	V
$V_{IL-ACHS}$	High-speed input low voltage for BP_DAT (logic 0)	V_{ref} – 0.440	-	V_{ref} - 0.070	V
V_{ID-DC}	Differential input voltage for abs(DQS_t – DQS_c)	0.1	-	-	V
V_{IH_DC}	Input high voltage for all BP_*	0.7 * VDDQ	-	-	V
V_{IL_DC}	Input low voltage for all BP_*	-	-	0.3* VDDQ	V
V_{OH_DC}	Output high voltage for all BP_*	0.8 * VDDQ	-	-	V

Symbol	Description	Min	Typ	Max	Unit
V_{OL_DC}	Output low voltage for all BP_*	-	-	0.2 * VDDQ	V
V_{OH_DC}	Output high voltage for BP_MEMRESET_L	0.8 * VDDQ	-	VDDQ	V
V_{OL_DC}	Output low voltage for BP_MEMRESET_L	VSS	-	0.2* VDDQ	V
RTT	On-die termination (ODT) programmable resistances	-	open, 120, 60, 40	-	Ohm
ROnPu	Output driver pull-up impedance: DQ, DQS outputs	-	120, 60, 40	-	Ohm
ROnPd	Output driver pull-down impedance: DQ, DQS outputs	-	120, 60, 40	-	Ohm
ROnPu	Output driver pull-up impedance: address, command, CLK outputs	-	120, 60, 40	-	Ohm
ROnPd	Output driver pull-down impedance: address, command, CLK outputs	-	120, 60, 40	-	Ohm
ROnPu	Output driver pull-up impedance: BP_CKE	-	24 - 40	-	Ohm
ROnPd	Output driver pull-down impedance: BP_CKE	-	24 - 40	-	Ohm
ROnPu	Output driver pull-up impedance: BP_MEMRESET_L	-	24 - 40	-	Ohm
ROnPd	Output driver pull-down impedance: BP_MEMRESET_L	-	24 - 40	-	Ohm

4.8 MIPI CSI RX Electrical Parameters

Table 4-9 summarizes the MIPI CSI high-speed receiver (RX) electrical characteristics.

Table 4-9 MIPI CSI RX Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Apply to CLKP/N and DATAP/N Inputs					
V_{PIN}	Pin signal voltage range	-50	-	1350	mV
I_{LEAK}	Pin leakage current	-10	-	10	μA
V_{GNDSH}	Ground shift	-50	-	50	mV
$V_{PIN(absmax)}$	Maximum transient output voltage level	-0.15	-	1.45	V
T_{Voh}	Maximum transient time above $V_{OH(absmax)}$	-	-	20	nS
HS Line Receiver DC Specifications					
V_{IDTH}	Differential input high voltage threshold			70(1)	mV

Symbol	Description	Min	Typ	Max	Unit
				40(2)	mV
V_{IDTL}	Differential input low voltage threshold	-70(1)			mV
		-40(2)			mV
V_{IHHS}	Single ended input high voltage			460(3)	mV
V_{ILHS}	Single ended input low voltage	-40(3)			mV
V_{CMRXDC}	Input common mode voltage	70		330(4)	mV
Z_{ID}	Differential input impedance	80	100	125	Ohm

(1) D-PHY spec 1.1 compatibility mode (<=1.5Gbps)

(2) In case of High-Speed deskew calibration (>1.5Gbps)

(3) Excluding possible additional RF interference of 100 mV peak sine wave beyond 450 MHz.

(4) Excluding possible additional RF interference of 100 mV peak sine wave beyond 450 MHz. This table value includes a ground difference of 50 mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz

4.9 MIPI DSI TX Electrical Parameters

Table 4-10 summarizes the MIPI DSI high-speed transmitter (TX) electrical characteristics.

Table 4-10 MIPI DSI TX Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Apply to CLKP/N and DATAP/N Inputs					
V_I	Input signal voltage range	-50	-	1350	mV
I_{LEAK}	Pin leakage current	-10	-	10	μA
V_{GNDSH}	Ground shift	-50	-	50	mV
$V_{PIN(absmax)}$	Maximum transient output voltage level	-0.15	-	1.45	V
T_{Voh}	Maximum transient time above $V_{OH(absmax)}$	-	-	20	nS
HS Line Driver DC Specifications					
$\|V_{OD}\|$(1)	HS Transmit Differential output voltage magnitude	140	200	270	mV
$\Delta\|V_{OD}\|$(2)	Change in Differential output voltage magnitude between logic states	-	-	14	mV
V_{CMTX}(2)	Steady-state common-mode output voltage	150	200	250	mV
$\Delta V_{CMTX(1,0)}$ (2)	Changes in steady-state common-mode output voltage between logic states	-	-	5	mV

Symbol	Description	Min	Typ	Max	Unit
V_{OHHS}(2)	HS output high voltage	-	-	360	mV
Z_{OS}	Single-ended output impedance	40	50	62.5	Ohm
ΔZ_{OS}	Single ended output impedance mismatch	-	-	10	%

(1) 80 Ω ≤ RL ≤ 125 Ω Note: It can be programmed using test control register 0x24(cb_sel_v400_prog[2:0]).

(2) 80 Ω ≤ RL ≤ 125 Ω

4.10 USB3.0 Electrical Parameters

Table 4-11 USB3.0 Electrical Parameters summarizes the USB3.0 electrical characteristics.

Table 4-11 USB3.0 Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Transmitter					
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8	-	1.2	V
$V_{TX-DIFF-PP-LOW}$	Low-Power Differential p-p Tx voltage swing	0.4	-	1.2	V
$V_{TX-RCV-DETECT}$	DC differential impedance	N/A	-	0.6	V
$C_{AC-COUPLING}$	AC Coupling Capacitor	75	-	200	nF
Receiver					
R_{RX-DC}	DC common mode impedance	18	-	30	Ohm
$R_{RX-DIFF-DC}$	Receiver DC differential impedance	72	-	120	Ohm
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	25k	-	N/A	Ohm
$V_{RX-LFPS-DET-DIFFp-p}$	LFPS Detect Threshold	100	-	300	mV

4.11 USB2.0 Electrical Parameters

Table 4-12 summarizes the USB2.0 electrical characteristics.

Table 4-12 USB2.0 Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Input Levels for Low-/full-speed					
V_{IH}	High (driven)	2.0	-	N/A	V

Symbol	Description	Min	Typ	Max	Unit
V_{IHZ}	High (floating)	2.7	-	3.6	V
V_{IL}	Low	N/A	-	0.8	V
V_{DI}	Differential Input Sensitivity	0.2	-	N/A	V
V_{CM}	Differential Common Mode Range	0.8	-	2.5	V
Input Levels for High-speed					
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	-	150	mV
V_{HSDSC}	High speed disconnect detection threshold (differential signal amplitude)	525	-	625	mV
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	-50	-	500	mV
Output Levels for Low-/full-speed					
V_{OL}	Low	0.0	-	0.3	V
V_{OH}	High (Driven)	2.8	-	3.6	V
V_{OSE1}	SE1	0.8	-	N/A	V
V_{CRS}	Output Signal Crossover Voltage	3.1	-	2.0	V
Output Levels for High-speed					
V_{HSOI}	High-speed idle level	-10.0	-	10.0	mV
V_{HSOH}	High-speed data signaling high	360	-	440	mV
V_{HSOL}	High-speed data signaling low	-10.0	-	10.0	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	-900	-	-500	mV

5 Thermal Management

5.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature should be below 125℃.

5.2 Package Thermal Characteristics

Table 5-1 lists the thermal resistance parameters of the X5.

Table 5-1 Thermal Resistance Parameters

Symbol	Description	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance in still air	17.4	°C/W
θ_{JB}	Junction-to-board thermal resistance	5.8	°C/W
θ_{JC}	Junction-to-case thermal resistance	0.1	°C/W

Note: The testing PCB is a 4-layer board, with a size of 101.5mm x 114.5mm and a thickness of 1.6mm.