

General Description

The WSK35N25 is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

The WSK35N25 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

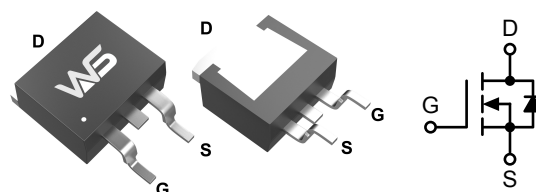
Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D
250V	100mΩ	35A

Applications

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

TO-263-2L Pin Configuration



Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	250	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Continuous Drain Current	35	A
I_{DM}	Pulsed Drain Current	105	A
E_{AS}	Single Pulse Avalanche Energy	900	mJ
I_{AS}	Avalanche Current	14	A
P_D	Power Dissipation ($T_C=25^{\circ}\text{C}$)	40	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	---	62.5	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	3.2	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	250	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ³	$V_{GS}=10V$, $I_D=22.5A$	---	100	130	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	2.0	3.0	4.0	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=250V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1.0	μA
I_{GSS}	Gate-Source Leakage Current	$V_{DS}=0V$, $V_{GS}=\pm 30V$	---	---	± 100	nA
Q_g	Total Gate Charge	$V_{DD}=200V$, $V_{GS}=10V$, $I_D=35A$	---	37.1	---	nC
Q_{gs}	Gate-Source Charge		---	11.4	---	
Q_{gd}	Gate-Drain Charge		---	15.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=125V$, $R_G=25\Omega$, $I_D=30A$	---	23	---	ns
T_r	Rise Time		---	85.4	---	
$T_{d(off)}$	Turn-Off Delay Time		---	40.6	---	
T_f	Fall Time		---	20.4	---	
C_{iss}	Input Capacitance	$V_{DS}=25V$, $V_{GS}=0V$, $f=1.0\text{MHz}$	---	1969	---	pF
C_{oss}	Output Capacitance		---	277	---	
C_{rss}	Reverse Transfer Capacitance		---	22	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current	$T_C=25^{\circ}\text{C}$	---	---	35	A
I_{SM}	Pulsed Source Current		---	---	140	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V$, $I_{SD}=30A$, $T_J=25^{\circ}\text{C}$	---	---	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS}=0V$, $I_S=30A$, $di_F/dt=100A/\mu s$	---	264	---	ns
Q_{rr}	Reverse Recovery Charge		---	3	---	μC

Note:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The E_{AS} data shows Max. rating . $I_{AS}=36A$, $V_{DD}=50V$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. The test condition is Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 1\%$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

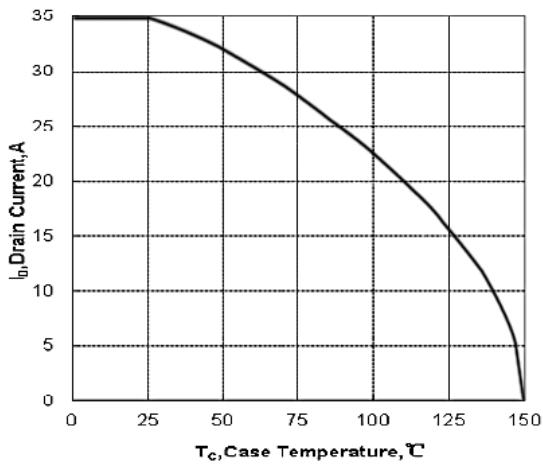


Figure 1 Maximum Continuous Drain Current

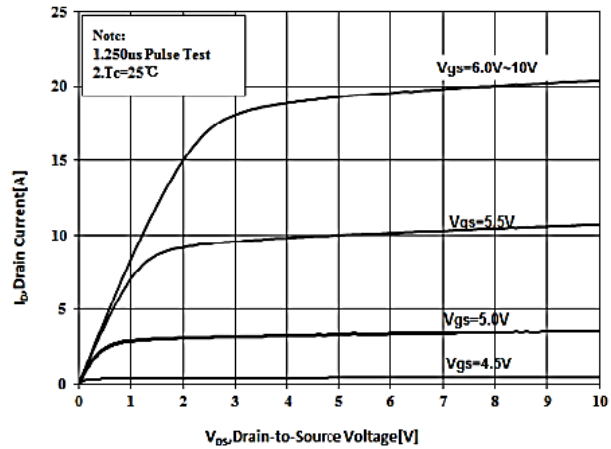


Figure 2 Typical Output Characteristics

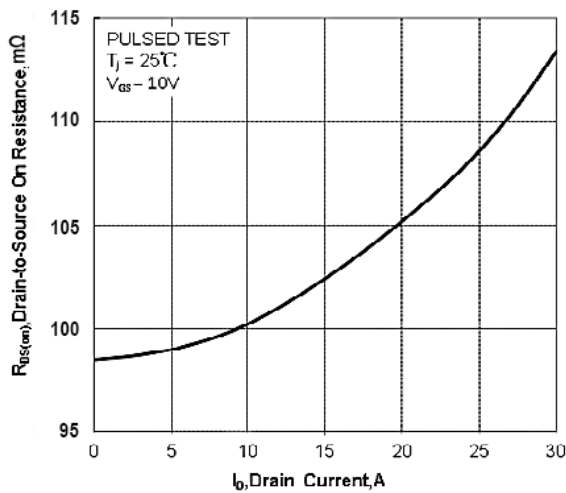


Figure 3 Typical Drain to Source ON Resistance vs Drain Current

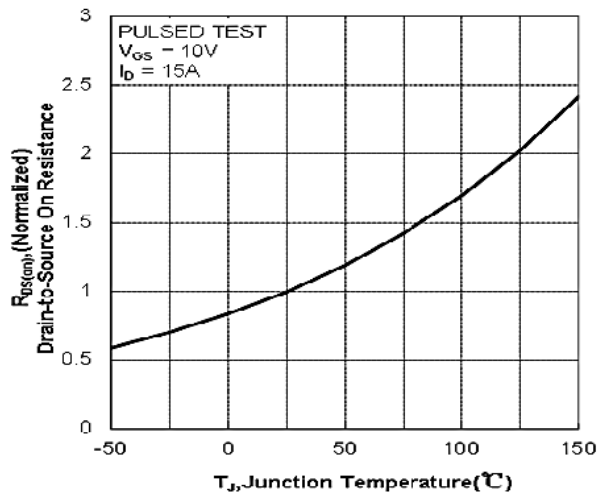


Figure 4 Typical Drain to Source on Resistance vs Junction Temperature

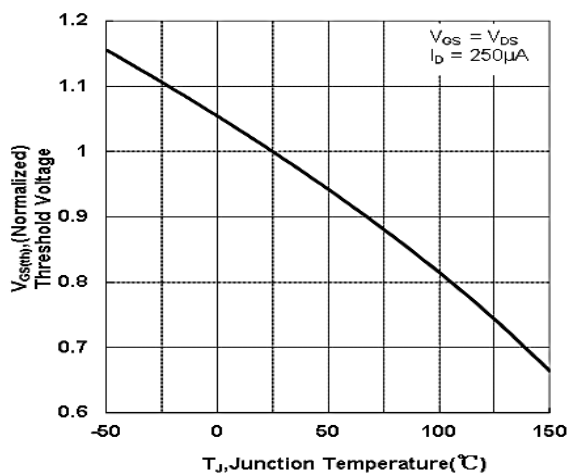


Figure 5 Typical Threshold Voltage vs Junction Temperature

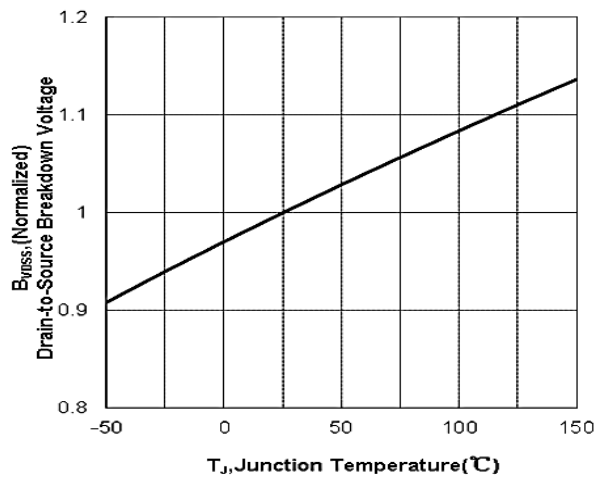


Figure 6 Typical Breakdown Voltage vs Junction Temperature

Typical Characteristics (Cont.)

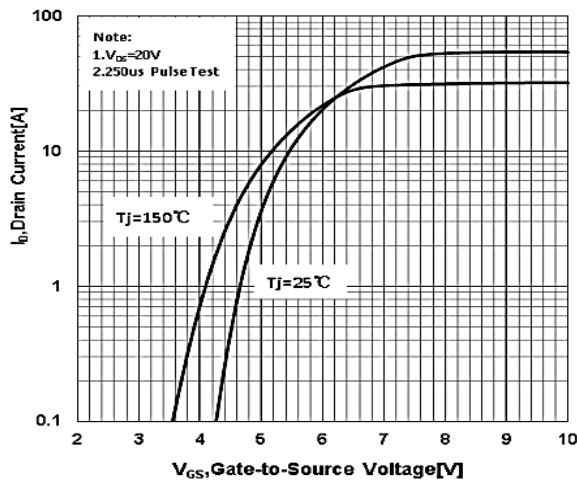


Figure 7 Typical Transfer Characteristics

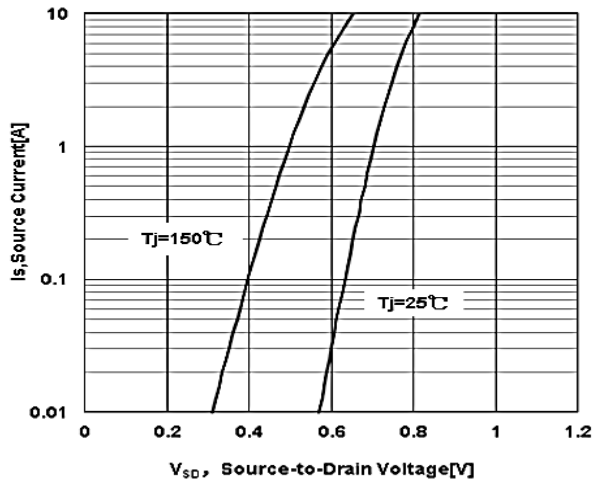


Figure 8 Typical Body Diode Transfer Characteristics

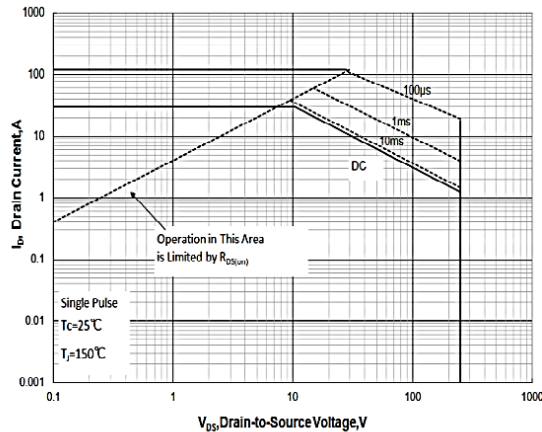


Figure 9 Maximum Forward Bias Safe Operating Area

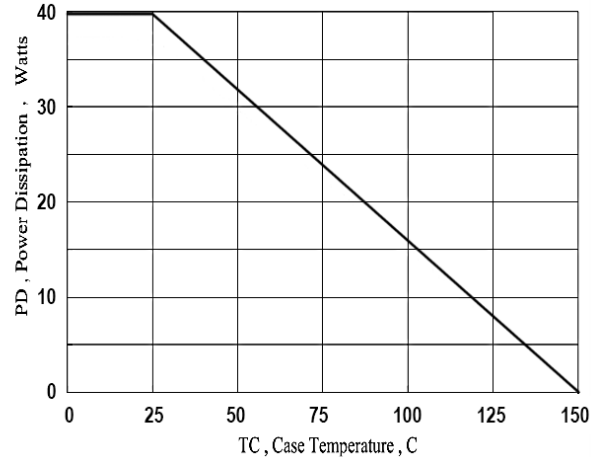


Figure 10 Maximum Power dissipation vs Case Temperature

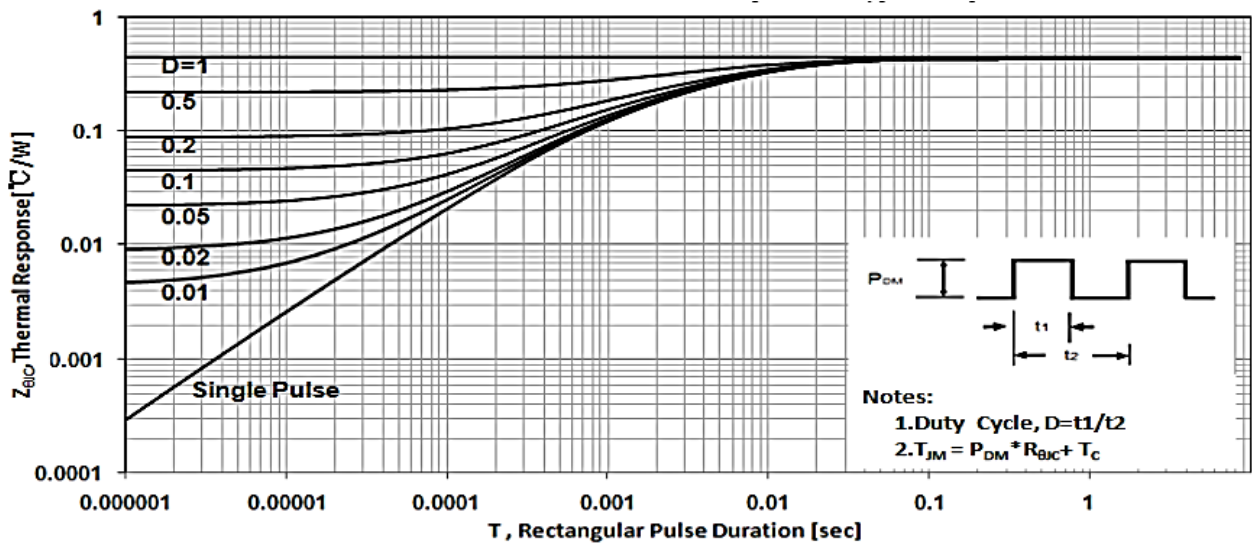
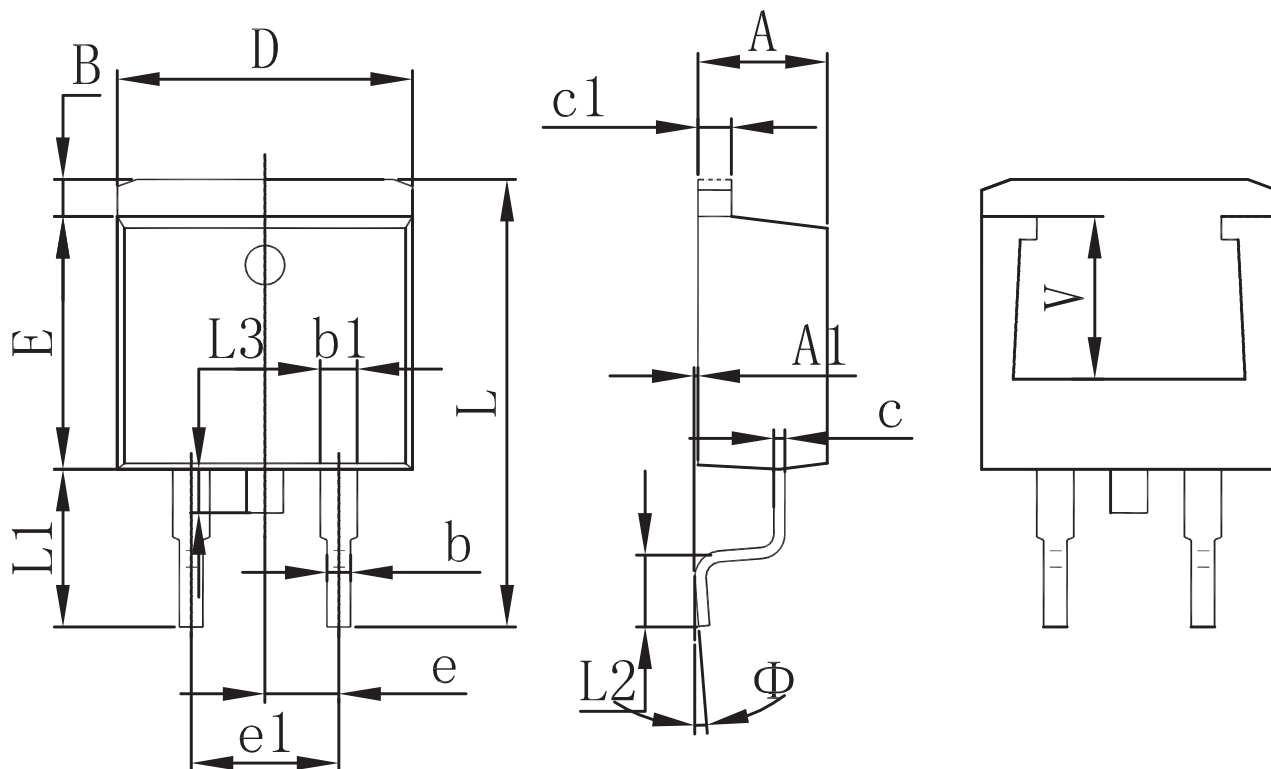


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

Packaging information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.120	1.420	0.044	0.056
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
L	14.940	15.500	0.588	0.610
L1	4.950	5.450	0.195	0.215
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
Φ	0°	8°	0°	8°
V	5.600 REF.		0.220REF.	

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