EVQ1923-RE-00A

100V, 8A, High-Frequency Half-Bridge Gate Driver Evaluation Board

DESCRIPTION

The EVQ1923-RE-00A is an evaluation board designed to demonstrate the MPQ1923, a high-frequency half-bridge gate driver. The MPQ1923 has a 7A source current (I_{SOURCE}) and 8A sink current (I_{SINK}) at a 12V driver power supply voltage (V_{DD}).

The integrated bootstrap (BST) diode reduces the external component count. The device's high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) drivers are controlled independently, and can be matched with a time delay (<5ns). If the IC supply is insufficient, then under-voltage lockout (UVLO) protection on both the HS-FET and LS-FET force the outputs low.

The MPQ1923 is designed for motor drivers and other power-control applications (e.g. telecommunication half-bridge power supplies, avionics DC/DC converters, two-switch forward converters, and active-clamp forward converters.

The MPQ1923 is available in a small QFN-10 (4mmx4mm) or QFN-8 (4mmx4mm) package.

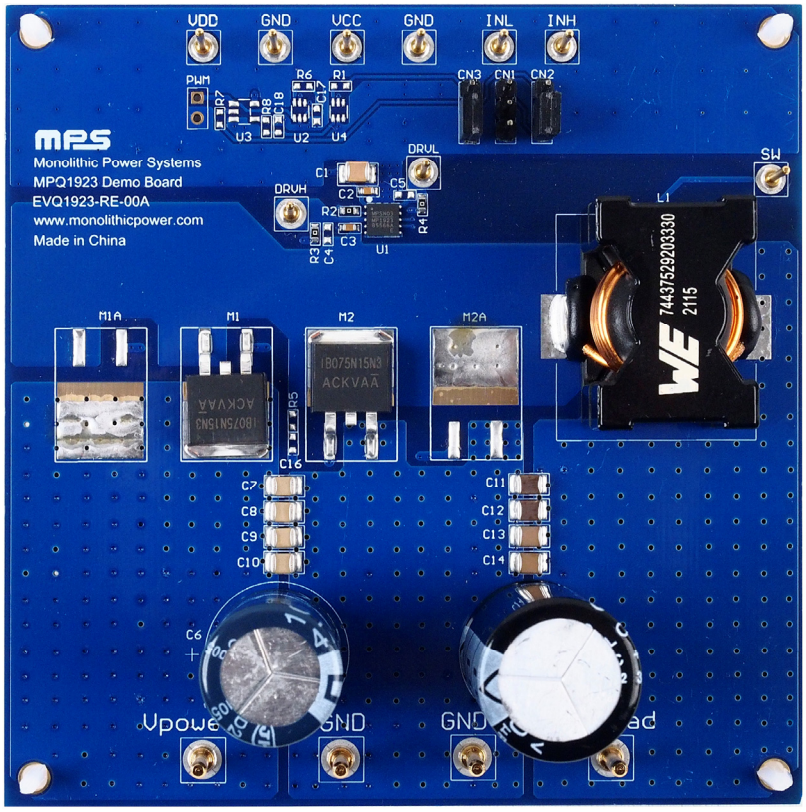
The EVQ1923-RE-00A is configured as a buck converter. The INH and INL pins are independent signals. Choose complementary pulse-width modulation (PWM) signals and a proper dead time (DT) for INH and INL.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Driver power supply voltage range (V_{DD})		5V to 17V
Input power supply voltage range (V_{IN})		0V to 100V
Floating HS-FET gate driver maximum source current (I_{SOURCE_MAX})	V_{DD} = 12V	7A
Floating HS-FET gate driver maximum sink current (I_{SINK_MAX})	V_{DD} = 12V	8A
LS-FET gate driver I_{SOURCE_MAX}	V_{DD} = 12V	7A
LS-FET gate driver I_{SINK_MAX}	V_{DD} = 12V	8A

EVQ1923-RE-00A EVALUATION BOARD



LxWxH (10cmx10cmx3.8cm)

Board Number	MPS IC Number
EVQ1923-RE-00A	MPQ1923GRE-AEC1

QUICK START GUIDE

1. Preset the driver power supply between 5V and 17V.
2. Preset the input voltage (V_{IN}) between 0V and 100V.
3. Connect two complementary pulse-width modulation (PWM) signals with a proper dead time to CN1. It is recommended to choose either 3.3V or 5V for the INH and INL logic high voltage.
4. Connect the driver power supply terminals to:
   a. Positive (+): VDD
   b. Negative (-): GND
5. Connect the input power supply terminals to:
   a. Positive (+): V_{POWER}
   b. Negative (-): GND
6. Attach the load terminals to:
   a. Positive (+): V_{LOAD}
   b. Negative (-): GND
7. Turn on the driver's power supply.
8. Check the INH, INL, DRVH, and DRVL signals to ensure that a sufficient dead time (DT) has been established for DRVH and DRVL.
9. Turn on the input power supply. The board should start up automatically.
10. Turn on the load, then check the output voltage (V_{OUT}) and output current (I_{OUT}) to ensure the buck circuitry is operating normally.
11. To turn off the system, follow the steps below:
    a. Turn off the load.
    b. Turn off the input power supply.
    c. Turn off the driver power supply.

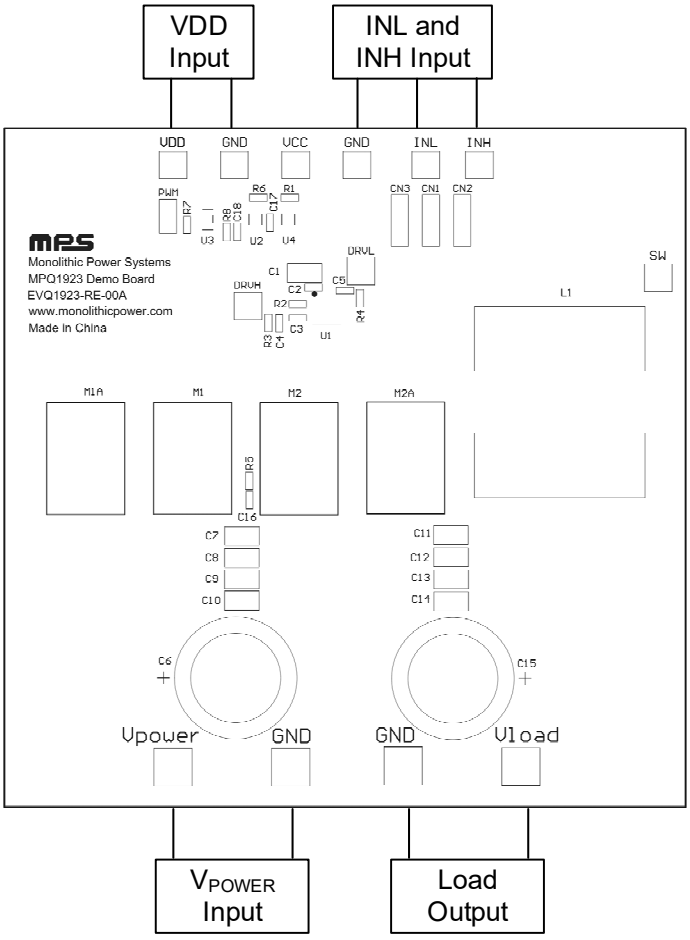


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

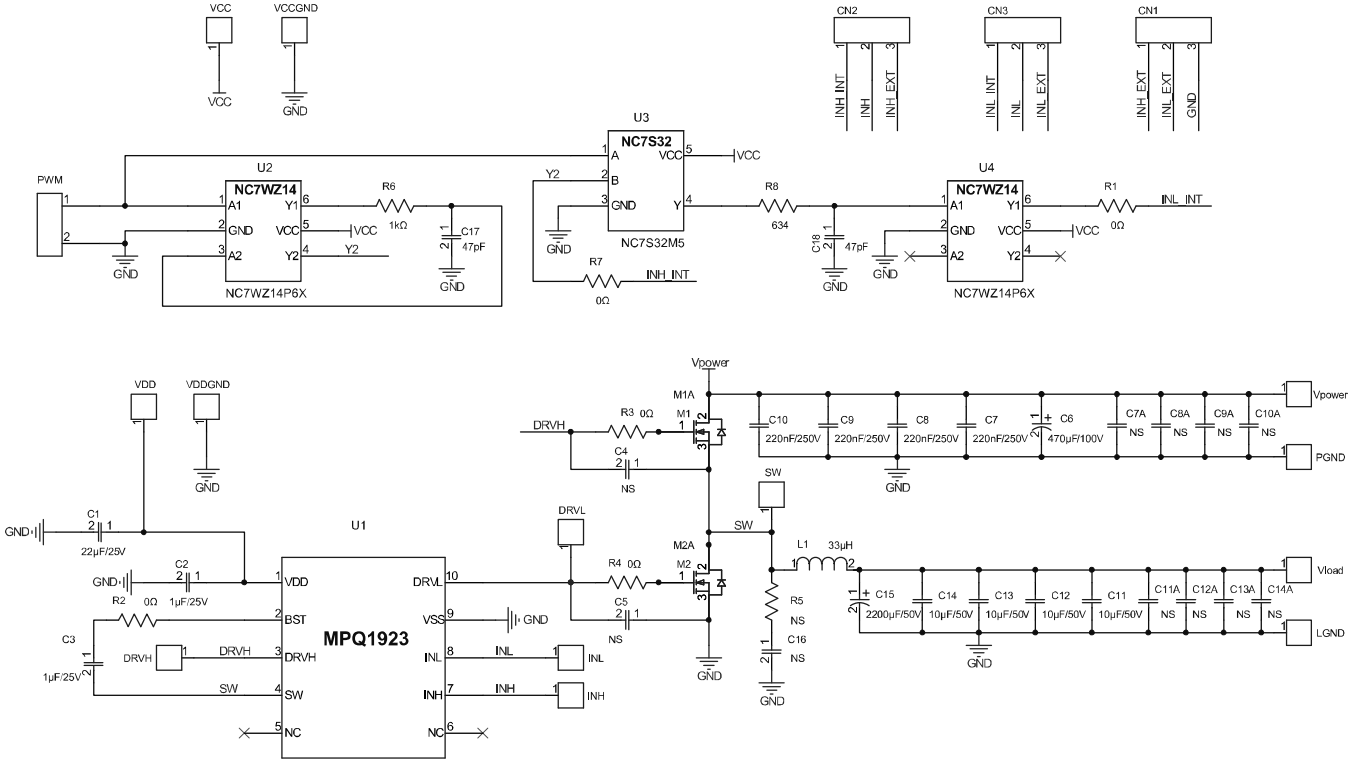


Figure 2: Evaluation Board Schematic

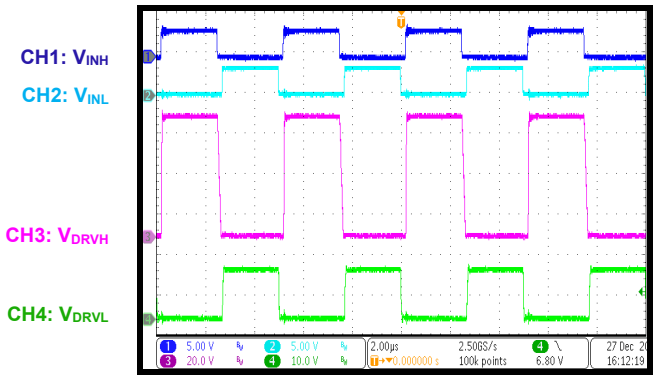
EVQ1923-RE-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	22μF	Ceramic capacitor, 25V, X7R	1210	Murata	GRM32ER71E226KE15L
2	C2, C3	1μF	Ceramic capacitor, 25V, X7R	0603	Murata	GCM188R71E105KA64D
2	C4, C5	NS				
1	C6	470μF	Electrolytic capacitor, 100V	DIP	Jianghai	CD263-100V470
4	C7, C8, C9, C10	220nF	Ceramic capacitor, 250V, X7R	1210	Murata	GRM32DR72E224KW01L
4	C11, C12, C13, C14	10μF	Ceramic capacitor, 50V, X7R	1210	Murata	GRM32ER71H106KA12L
9	C7A, C8A, C9A, C10A, C11A, C12A, C13A, C14A, C16	NS				
1	C15	2200μF	Electrolytic capacitor, 50V	DIP	Jianghai	CD28L-50V2200
3	R2, R3, R4	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
1	R5	NS				
2	M1, M2	150V	N-channel MOSFET, 90A	TO-263	Analog Power	AMIB075N15N3-T1-PF
2	M1A, M2A	NS				
1	L1	33μH	Inductor, 33μH, 15.4A	SMD	Wurth	74437529203330
4	V_{POWER}, V_{LOAD}, GNDx2	2mm	Golden pin	SIP	Custom	
9	VDD, GND, VCC, GND, INL, INH, DRVH, DRVL, SW	1mm	Golden pin	SIP	Custom	
1	U1	MPQ1923	Half-bridge gate driver, 100V, 8A	QFN-10 (4mmx 4mm)	MPS	MPQ1923GRE-AEC1

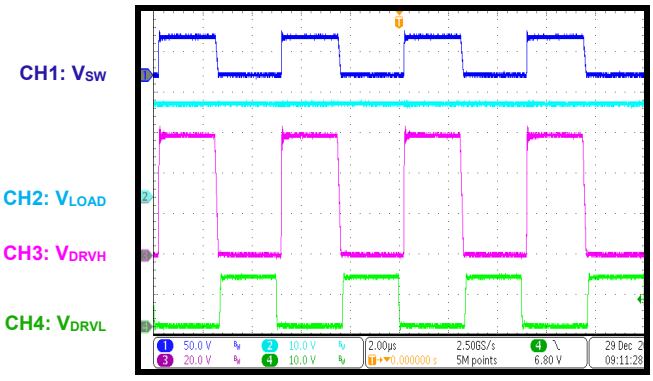
EVB TEST RESULTS

V_{DD} = 12V, V_{POWER} = 48V, INH/INL = 200kHz, dead time = 200ns, I_{LOAD} = 1A, T_A = 25°C, unless otherwise noted.

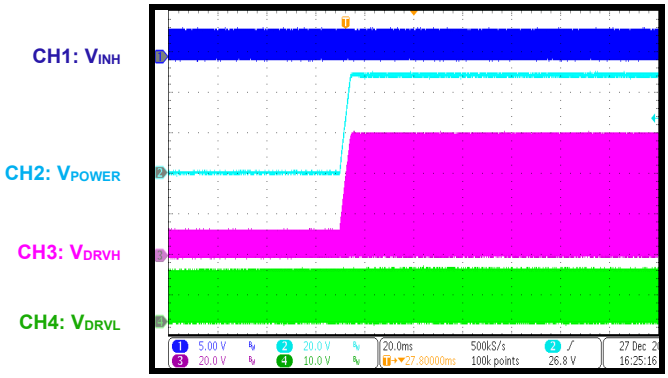
Steady State



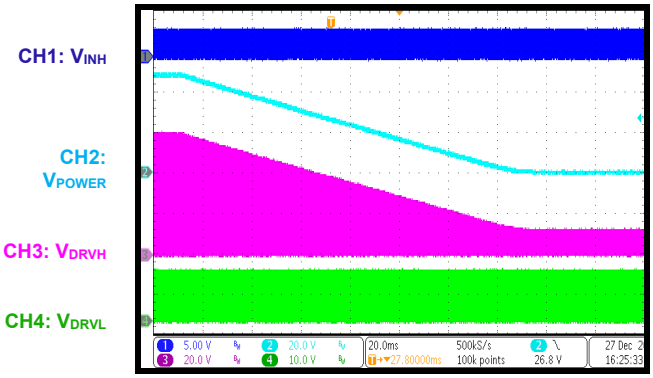
Steady State



Power Ramps Up



Power Ramps Down



PCB LAYOUT

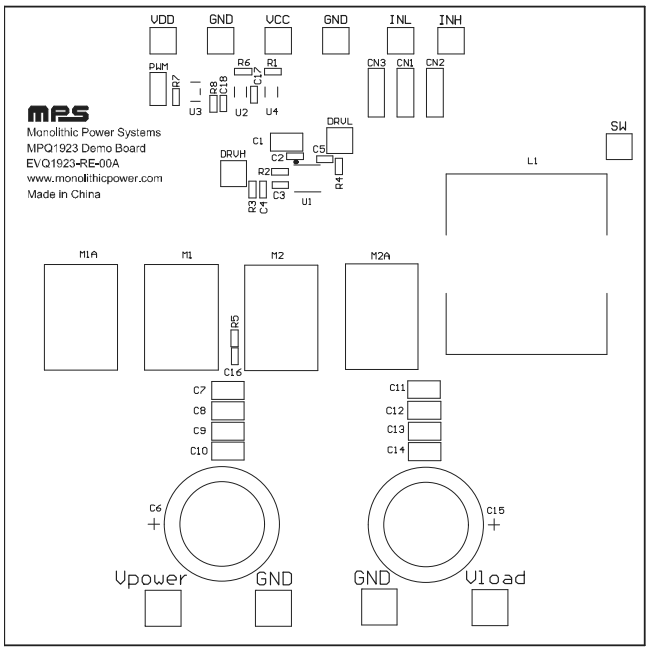


Figure 3: Top Silk

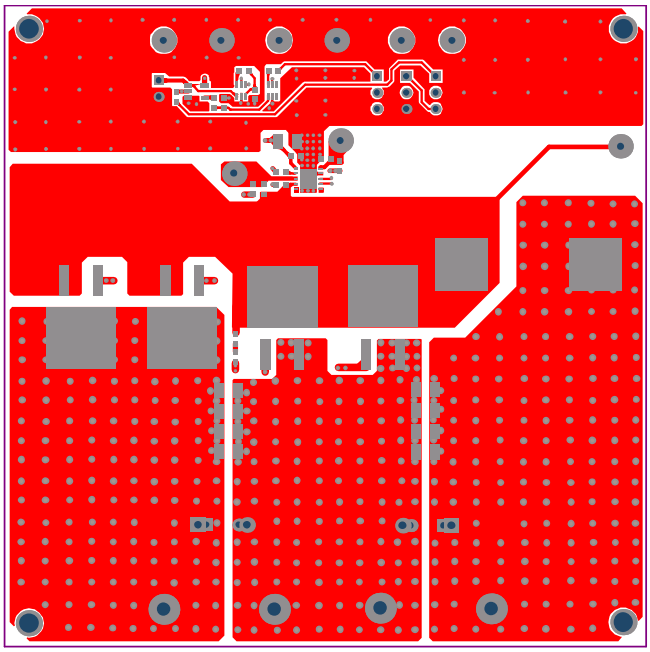


Figure 4: Top Layer

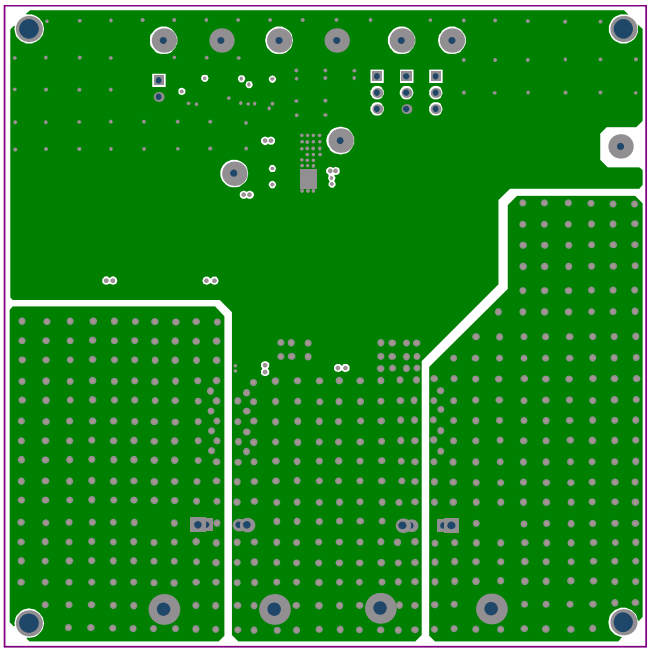


Figure 5: Mid-Layer 1

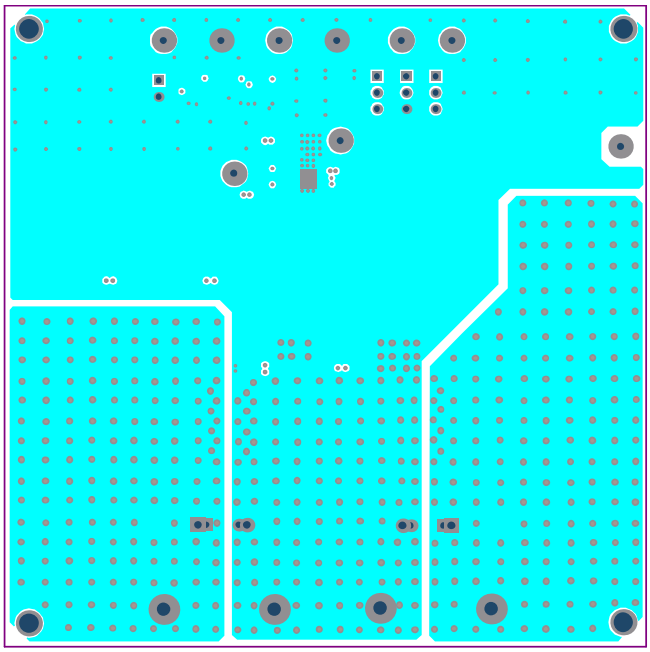


Figure 6: Mid-Layer 2

PCB LAYOUT *(continued)*

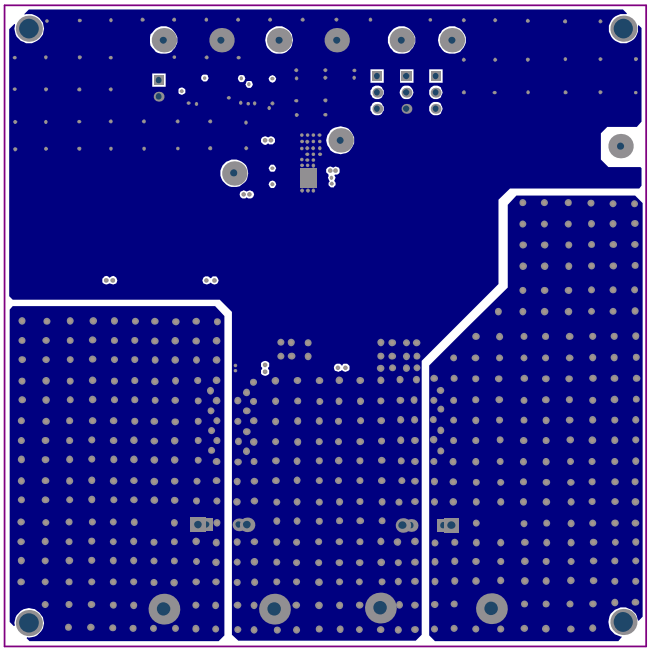


Figure 7: Mid-Layer 3

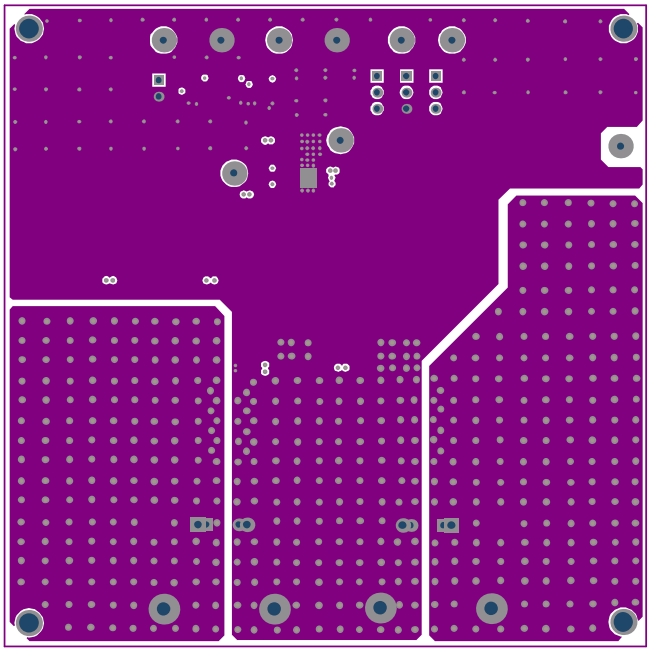


Figure 8: Mid-Layer 4

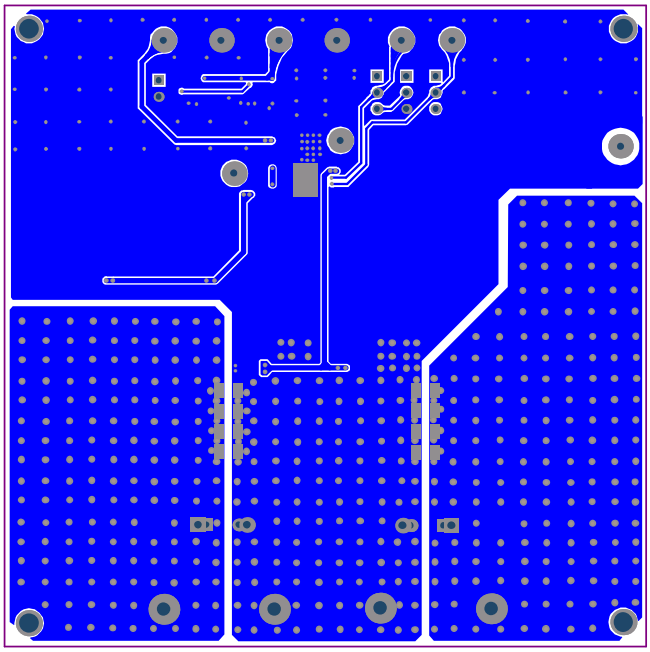


Figure 9: Bottom Layer

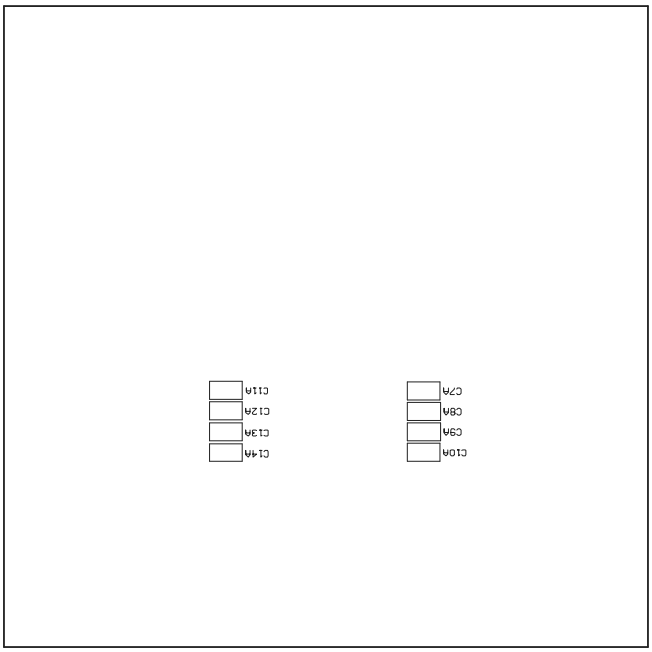


Figure 10: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/8/2022	Initial Release	-