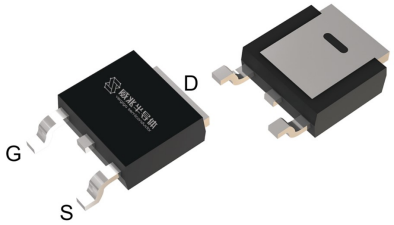
Features

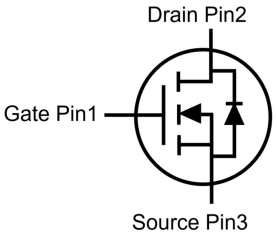
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$
- VitoMOS® Ⅱ Technology
- Fast Switching and High efficiency
- 100% Avalanche test

V_{DS}	40	V
$R_{DS(on),TYP}$@ V_{GS}=10V	3.6	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5V	5.3	mΩ
I_D	90	A

TO-252



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VSD007N04MS-G	TO-252	007N04M	2500PCS/Reel

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		40	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C=25°C	90	A
I_D	Continuous drain current @VGS=10V	T_C=25°C	90	A
		T_C=100°C	64	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	360	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	14	A
		T_A=70°C	11	A
EAS	Avalanche energy, single pulsed ②		45	mJ
P_D	Maximum power dissipation	T_C=25°C	51	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	1.3	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.95	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	120	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=40V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.2	1.7	2.3	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=30A	--	3.6	4.5	mΩ
		T_j=100℃	--	4.3	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=4.5V, I_D=20A	--	5.3	6.6	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=20V,V_{GS}=0V, f=1MHz	970	1295	1720	pF
Coss	Output Capacitance		370	490	650	pF
Crss	Reverse Transfer Capacitance		20	30	40	pF
Rg	Gate Resistance	f=1MHz	0.2	1.5	3	Ω
Qg(10V)	Total Gate Charge	V_{DS}=20V,I_D=30A, V_{GS}=10V	--	27	36	nC
Qg(4.5V)			--	14	19	nC
Qgs	Gate-Source Charge		--	4.4	5.9	nC
Qgd	Gate-Drain Charge		--	6.1	9.2	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=20V, I_D=30A, R_G=3Ω, V_{GS}=10V	--	7.2	--	ns
Tr	Turn-on Rise Time		--	61	--	ns
Td(off)	Turn-Off Delay Time		--	24	--	ns
Tf	Turn-Off Fall Time		--	33	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=30A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=30A, V_{GS}=0V di/dt=100A/μs	--	19	38	ns
Qrr	Reverse Recovery Charge		--	6.7	13.5	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.1mH,R_G = 25Ω, I_{AS} = 30A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

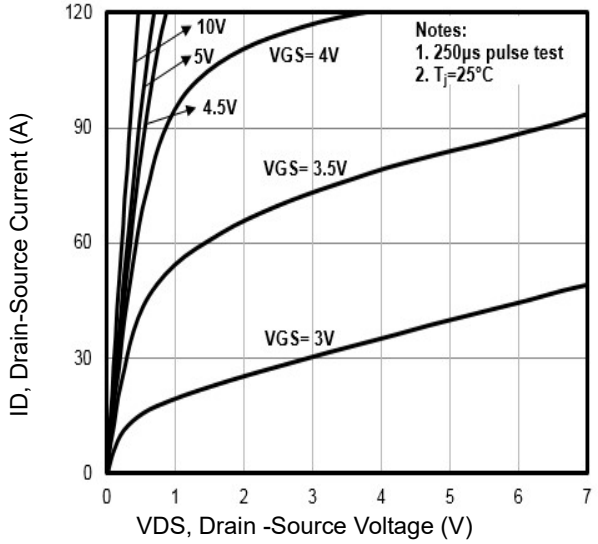


Fig1. Typical Output Characteristics

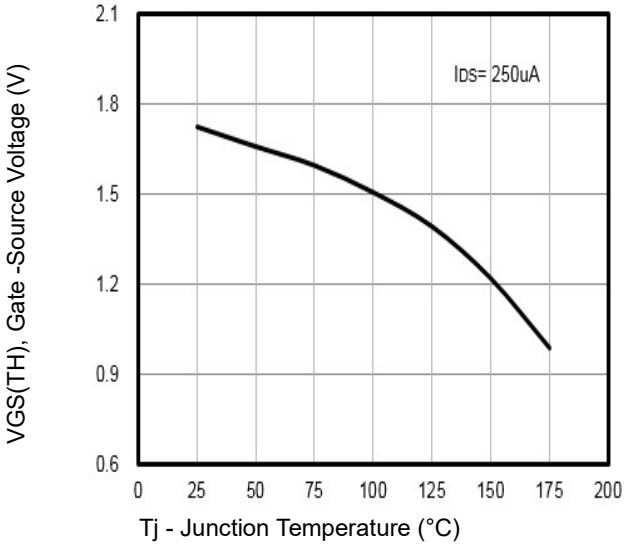


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

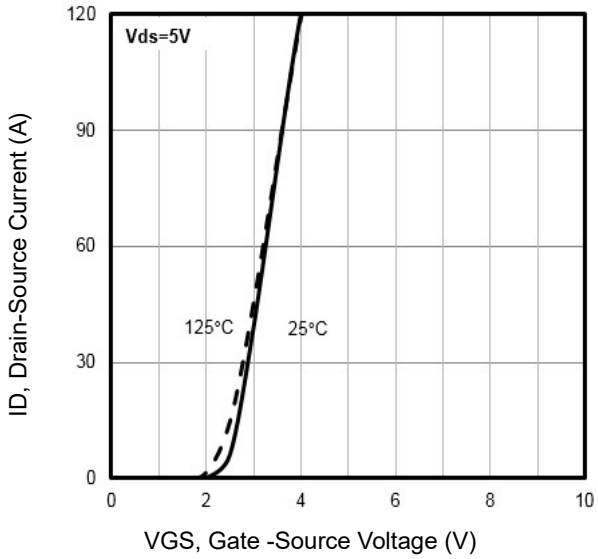


Fig3. Typical Transfer Characteristics

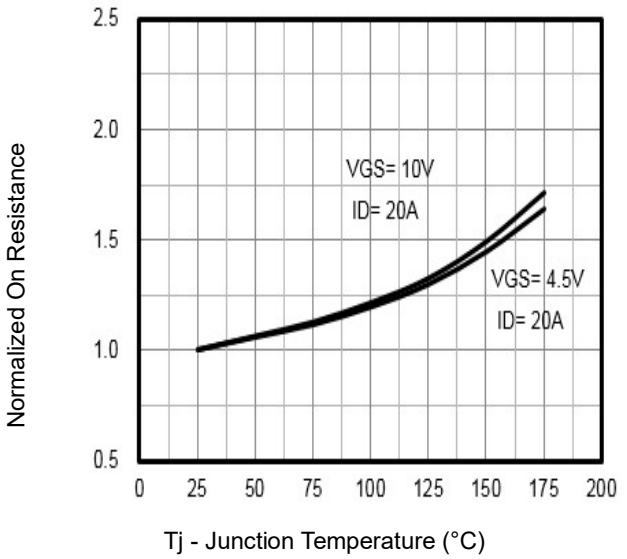


Fig4. Normalized On-Resistance Vs. Tj

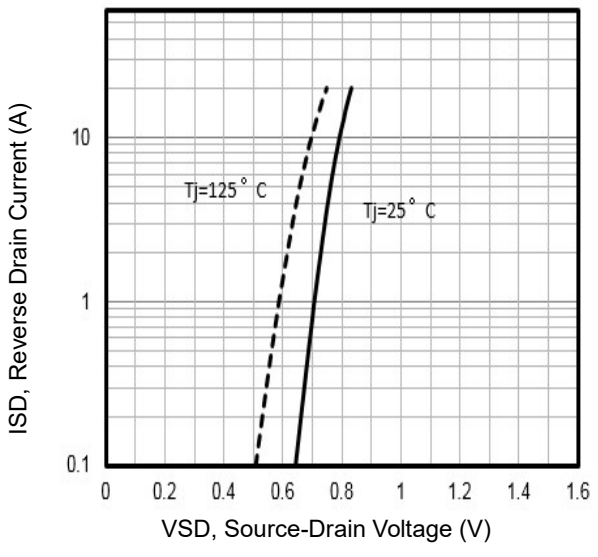


Fig5. Typical Source-Drain Diode Forward Voltage

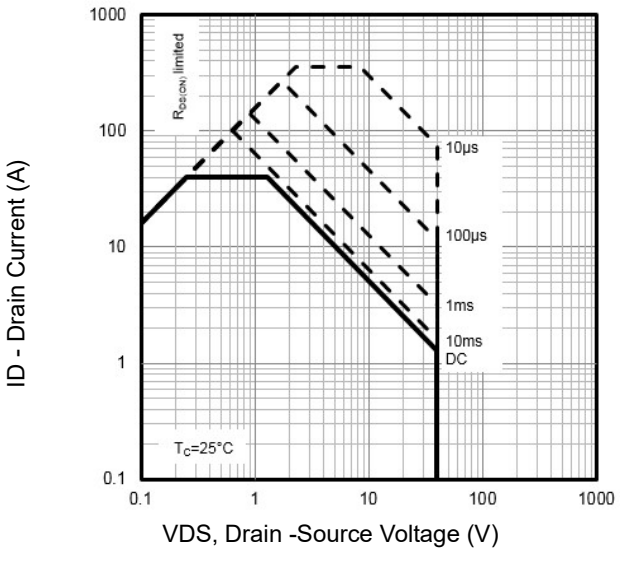


Fig6. Maximum Safe Operating Area

Typical Characteristics

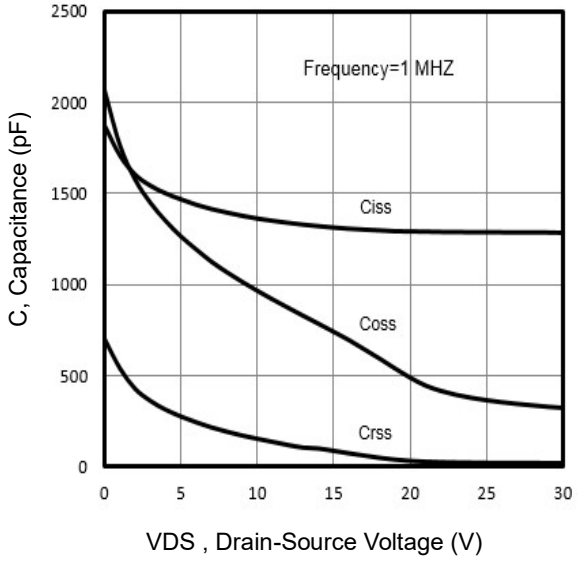


Fig7. Typical Capacitance Vs.Drain-Source Voltage

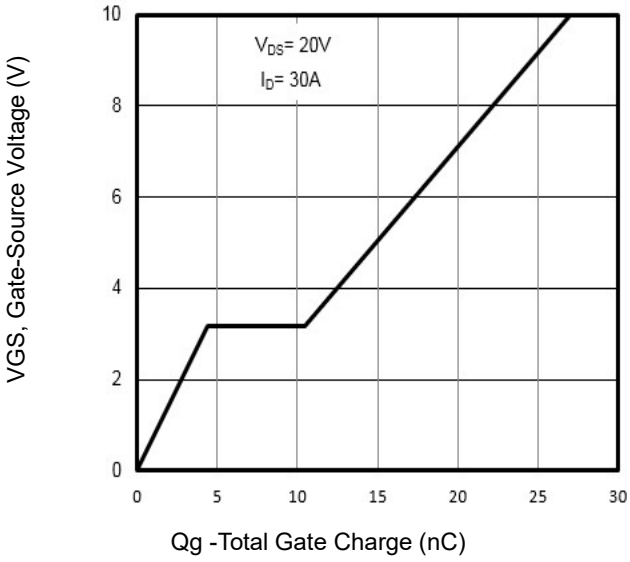


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

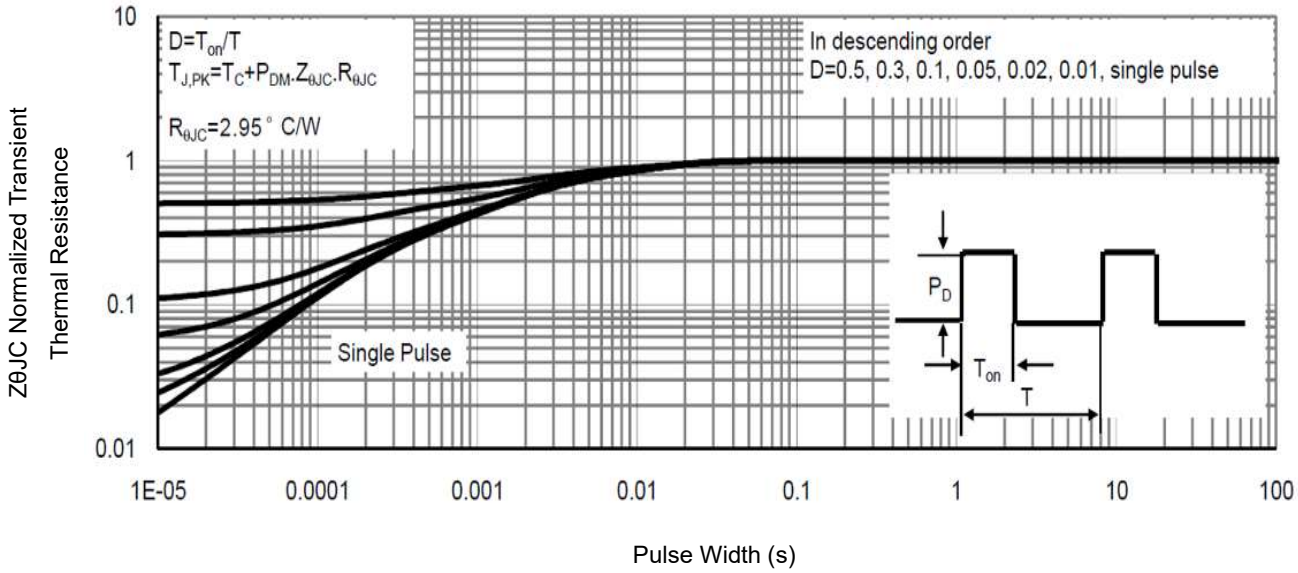


Fig9. Normalized Maximum Transient Thermal Impedance

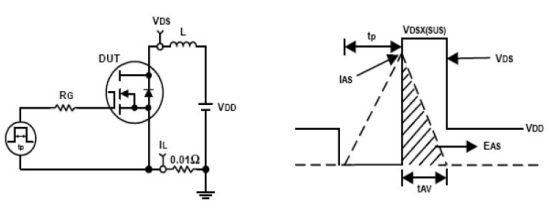


Fig10. Unclamped Inductive Test Circuit and waveforms

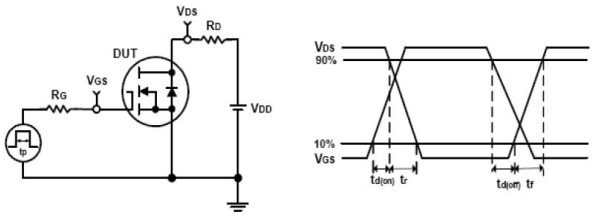
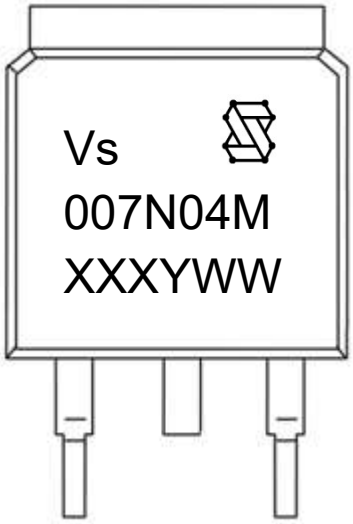


Fig11. Switching Time Test Circuit and waveforms

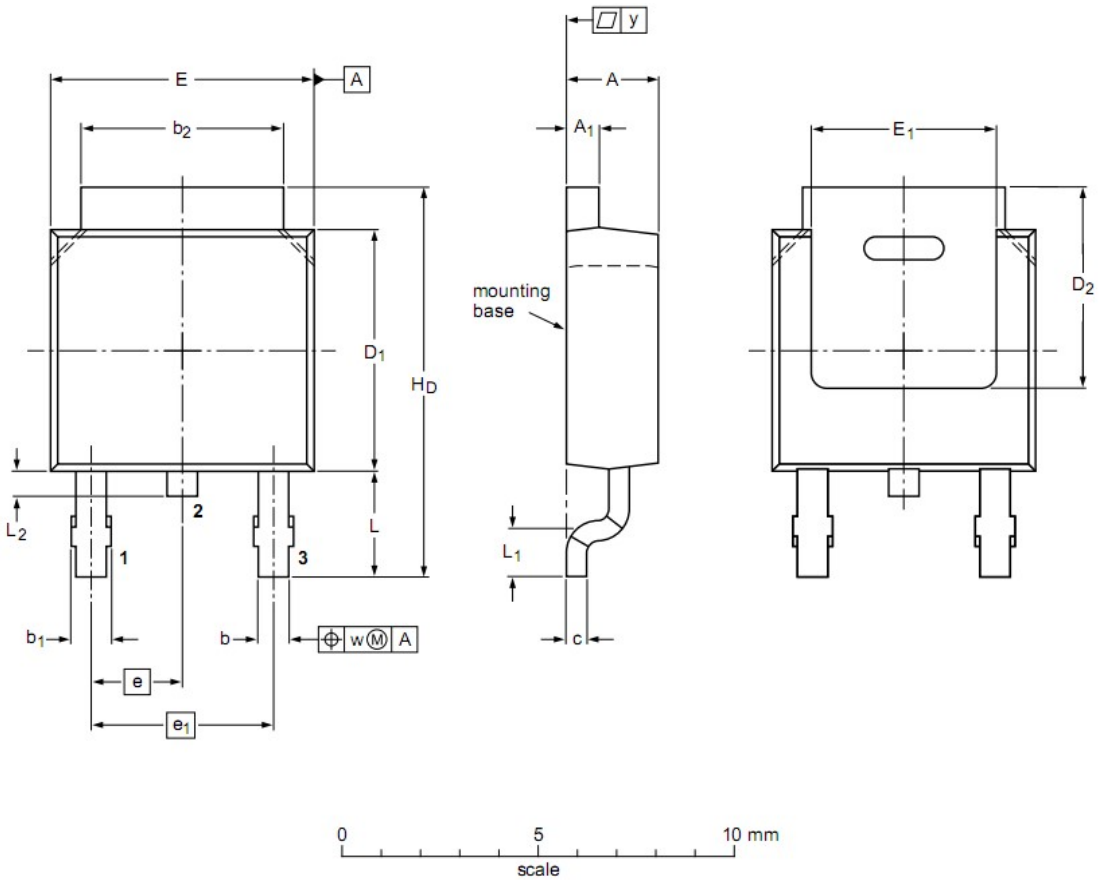
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（007N04M）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A_1	0.46	0.50	0.63
b	0.64	0.76	0.89
b_1	0.77	0.85	1.14
b_2	5.00	5.33	5.46
c	0.458	0.508	0.558
D_1	5.98	6.10	6.223
D_2	5.21	--	--
E	6.40	6.60	6.731
E_1	4.40	--	--
e	2.286 BSC		
e_1	--	4.57	--
H_D	9.40	10.00	10.40
L	2.743 REF		
L_1	1.40	1.52	1.77
L_2	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

Customer Service

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