8-Stage Shift-And-Store Bus Register

1 FEATURES

- **Separate Serial Outputs Synchronous to Both Positive and Negative Clock Edges For Cascading**
- **Operating Voltage Range: 2V to 5.5V**
- **Low Power Consumption: 80μA (Max)**
- **Low input current: 1μA(Max)**
- **Operating Temperature Range: -40°C to +125°C**
- **Balanced Propagation Delay and Transition Times**
- **Micro SIZE PACKAGES: SOP16**

2 APPLICATIONS

- **Serial-to-parallel data conversion**
- **Remote control holding register**

3 DESCRIPTIONS

RS4094 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (D) and two serial outputs (QS1 and QS2) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the CP input. Data is available at QS1 on the LOW-to HIGH transitions of the CP input to allow cascading when clock edges are fast. The same data is available at QS2 on the next HIGH-to-LOW transition of the CP input to allow cascading when clock edges are slow. The data in the shift register is transferred to the storage register when the STR input is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) is HIGH. A LOW on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the registers.

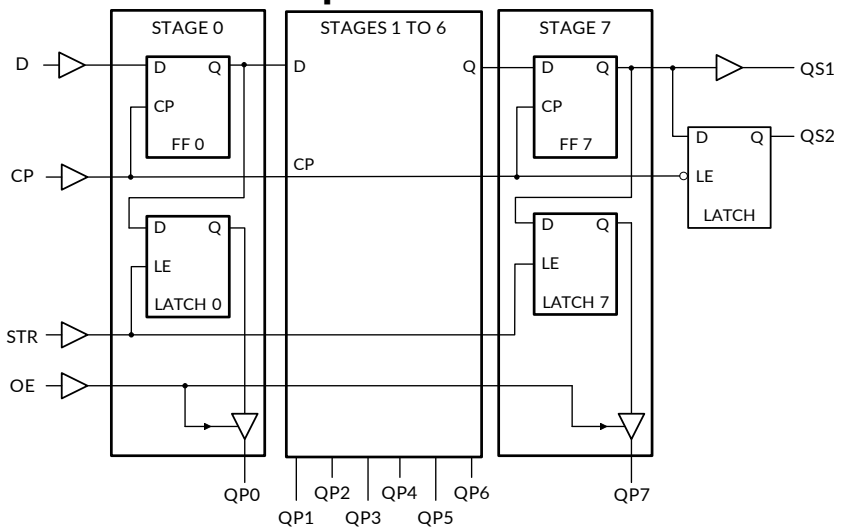
This device available in Green SOP16 packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS4094	SOP16	9.90mm×3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2024/03/11	Initial version completed

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS4094	RS4094XS16	-40°C ~+125°C	SOP16	RS4094	MSL3	Tape and Reel, 4000

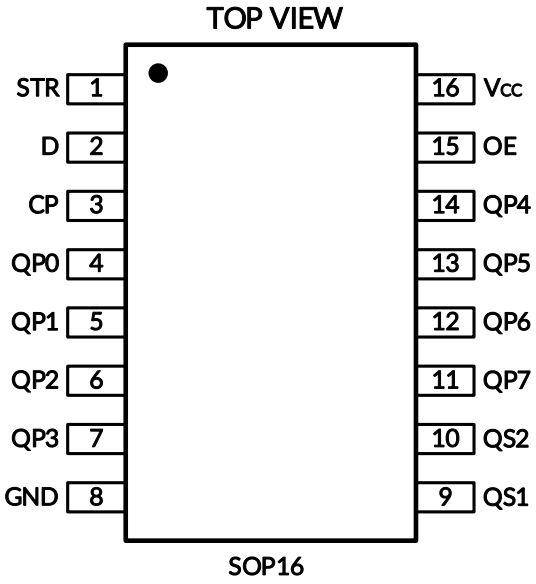
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

7 PIN CONFIGURATIONS



7.1 PIN DESCRIPTION

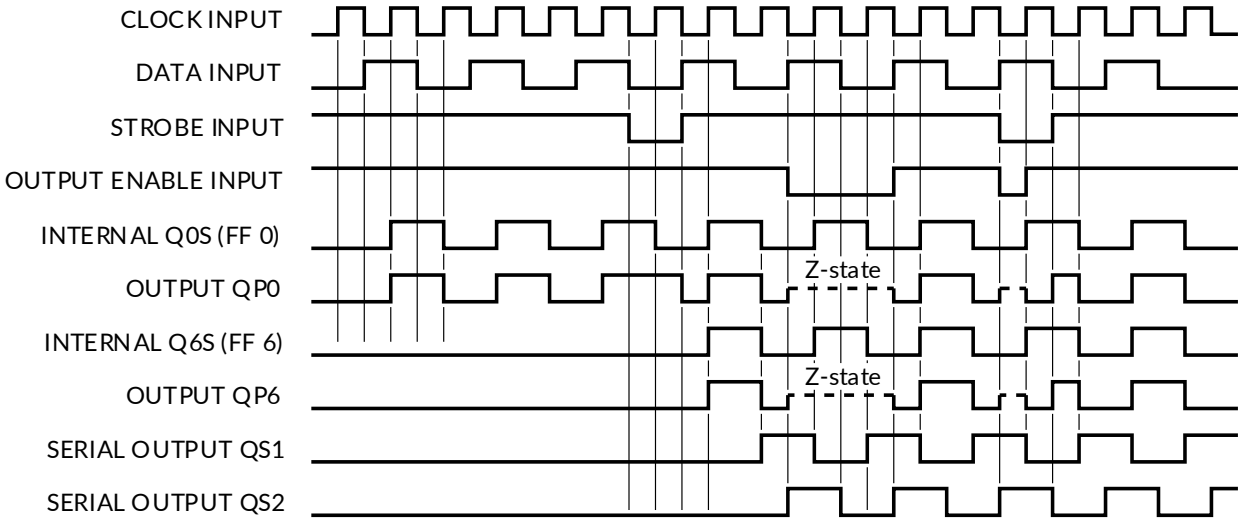
SYMBOL	PIN	DESCRIPTION
	SOP16	
STR	1	Strobe input
D	2	Data input
CP	3	Clock input
QP0 to QP7	4,5,6,7,14,13,12,11	Parallel output
GND	8	Ground supply voltage
QS1, QS2	9,10	Serial output
OE	15	Output enable input
V_{CC}	16	Supply voltage

7.2 FUNCTION TABLE

Inputs				Parallel Outputs		Serial Outputs	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn-1	Q6S	NC
↑	H	H	H	H	QPn-1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

(1) H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = HIGH-impedance OFF-state; NC = no change;
(2) ↑ = positive-going transition; ↓ = negative-going transition;
(3) Q6S = the data in register stage 6 before the LOW to HIGH clock transition;
(4) Q7S = the data in register stage 7 before the HIGH to LOW clock transition.

7.3 Timing diagram



At the positive clock edge, the information in the 7th register stage is transferred to the 8th register stage and the QSn outputs.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	6.5	V
I_{IK}	Input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
I_O	Output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		±25	mA
I_{CC}	Supply current			50	mA
I_{GND}	Ground current			-50	mA
θ_{JA}	Package thermal impedance (3)	SOP16		150	°C/W
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD-51.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), JEDEC EIA/ JESD22-A114	±2000	V
	Charged-device model (CDM), ANSI/ESDA/ JEDEC JS-002-2022	±1000	V
	Machine model (MM), JESD22-A115C (2010)	±200	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, unless otherwise noted.) (1)

9.1 Recommended Operating Conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{amb}	Ambient temperature		-40	25	125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V			1000	ns/V
		V_{CC}=3.3V			600	
		V_{CC}=4.5V			500	
		V_{CC}=5.5V			400	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

9.2 DC Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

PARAMETER		TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
				25°C			-40°C to 85°C			-40°C to 125°C			
				MIN (1)	TYP (2)	MAX (1)	MIN (1)	TYP (2)	MAX (1)	MIN (1)	TYP (2)	MAX (1)	
V_{IH}	HIGH-level input voltage		2.0V	1.5			1.5			1.5			V
			3.3V	2.35			2.35			2.35			
			4.5V	3.15			3.15			3.15			
			5.5V	3.85			3.85			3.85			
V_{IL}	LOW-level input voltage		2.0V			0.5			0.5			0.5	V
			3.3V			0.95			0.95			0.95	
			4.5V			1.35			1.35			1.35	
			5.5V			1.65			1.65			1.65	
V_{OH}	HIGH-level output voltage	I_O = −20μA	2.0V	1.9			1.9			1.9			V
		I_O = −20μA	3.3V	3.2			3.2			3.2			
		I_O = −20μA	4.5V	4.4			4.4			4.4			
		I_O = −20μA	5.5V	5.4			5.4			5.4			
		I_O = −6mA	4.5V	3.98			3.84			3.7			
		I_O = −7.8mA	5.5V	4.86			4.68			4.5			
V_{OL}	LOW-level output voltage	I_O = 20μA	2.0V			0.1			0.1			0.1	V
		I_O = 20μA	3.3V			0.1			0.1			0.1	
		I_O = 20μA	4.5V			0.1			0.1			0.1	
		I_O = 20μA	5.5V			0.1			0.1			0.1	
		I_O = 6mA	4.5V			0.26			0.33			0.4	
		I_O = 7.8mA	5.5V			0.3			0.38			0.45	
I_I	Input leakage current	V_I = V_{CC} or GND	6.0V			±0.3			±1			±1	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND	5.5V			±0.3			±1			±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND I_O = 0A	5.5V			4			40			80	μA
C_I	Input capacitance				5								pF

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

9.3 AC Characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified.

PARAMETER		TEST CONDITIONS	Vcc	25°C			-40°C to 85°C			-40°C to 125°C			UNIT
				MIN (2)	TYP (3)	MAX (2)	MIN (2)	TYP (3)	MAX (2)	MIN (2)	TYP (3)	MAX (2)	
t_{pd}	Propagation delay	CP to QS1	2V		24	36			40			42	ns
			3.3V		15	22			24			26	
			4.5V		8	12			14			15	
			5.5V		7	11			12			13	
		CP to QS2	2V		15	23			25			27	ns
			3.3V		11	16.5			18			21	
			4.5V		5	8			8.5			9	
			5.5V		4.5	7			7.5			8	
		CP to QPn	2V		30	45			48			51	ns
			3.3V		17	25			28			32	
			4.5V		10	15			17			18	
			5.5V		9	13			14.5			15	
		STR to QPn	2V		23	34			39			42	ns
			3.3V		14	21			23			25.5	
			4.5V		9	13			14			15	
			5.5V		8	12			12.5			13	
t_{en}	Enable time	OE to QPn	2V		19	29			34			37	ns
			3.3V		12	18			22			24	
			4.5V		7	11			13			14	
			5.5V		6.5	10			11			12	
t_{dis}	Disable time	OE to QPn	2V		19.5	30			30.5			31	ns
			3.3V		18	27			28			29.5	
			4.5V		15	23			24			25	
			5.5V		14	21			22			23	
t_t	Transition time	QPn and QSn	2V		19.5	30			36			42	ns
			3.3V		11	16.5			20			22	
			4.5V		7	11			13			16	
			5.5V		6	9			11			12	
t_w	Pulse width	CP HIGH or LOW	2V	80			100			120			ns
			3.3V	30			35			45			
			4.5V	16			20			24			
			5.5V	14			17			20			
		STR HIGH	2V	80			100			120			ns
			3.3V	30			35			45			
			4.5V	16			20			24			
			5.5V	14			17			20			

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

AC Characteristics (continued)

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified.

PARAMETER		TEST CONDITIONS	V_{CC}	25°C			-40°C to 85°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{su}	Set-up time	D to CP	2V	50			65			75			ns
			3.3V	20			22			26			
			4.5V	10			13			15			
			5.5V	9			11			13			
		CP to STR	2V	100			125			150			ns
			3.3V	35			42			52			
			4.5V	20			25			30			
			5.5V	17			21			26			
t_h	Hold time	D to CP	2V	2.5									ns
			3.3V	2									
			4.5V	1.5									
			5.5V	1.5									
		CP to STR	2V	-5									ns
			3.3V	-3									
			4.5V	-2.5									
			5.5V	-2									
f_{max}	Maximum frequency	CP	2V	6			5			4			MHz
			3.3V	15			12			10			
			4.5V	30			24			20			
			5.5V	35			28			24			
C_{PD} (4)	Power dissipation capacitance	V_{CC}=5.5V, D = 1 MHz; CP=10MHz; V_I = GND to V_{CC} (5) (6)		135									pF

(4) Power dissipation capacitance per transceiver.

(5) C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

(6) $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_O)$ where:

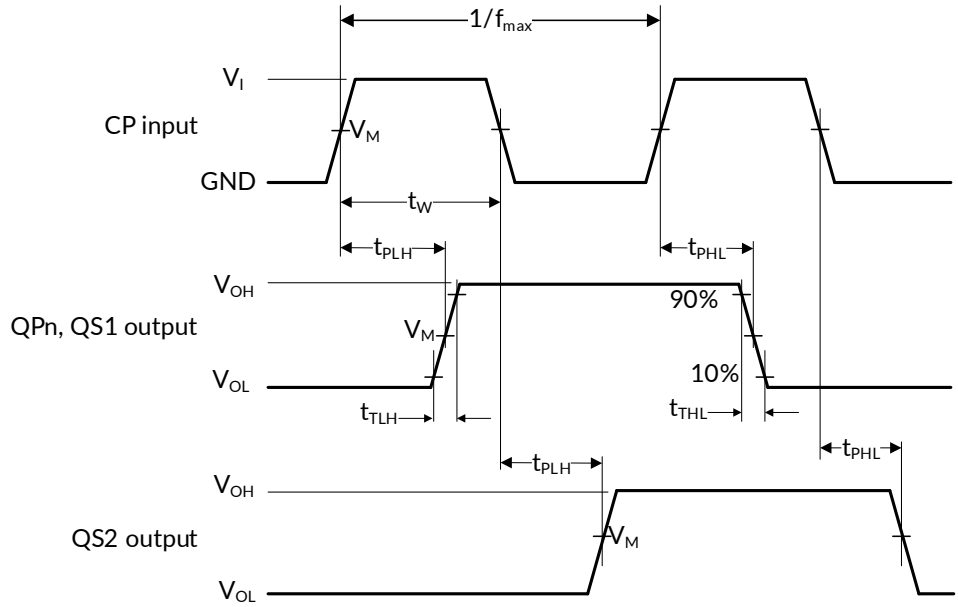
f_i = input frequency in MHz;

f_O = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs;

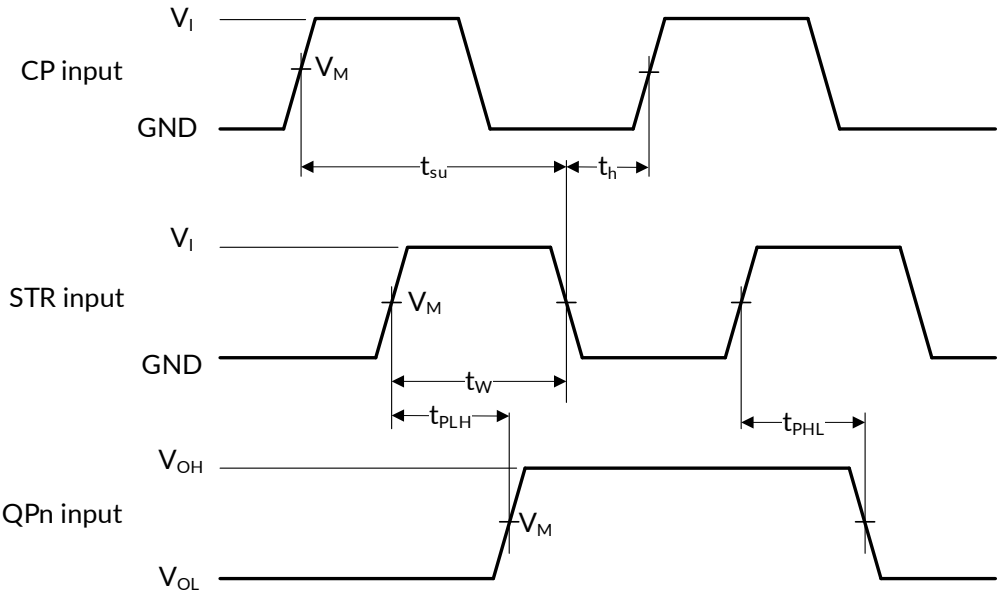
C_L = output load capacitance in pF;

10 Waveforms and test circuits



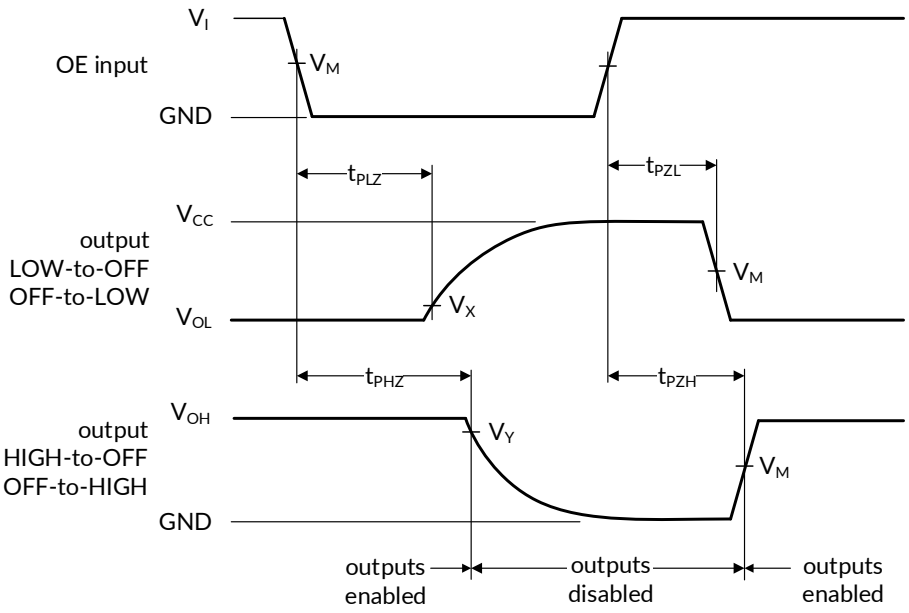
Measurement points are given in Table 1.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 1. Propagation delay input (CP) to output (QPn, QS1, QS2), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



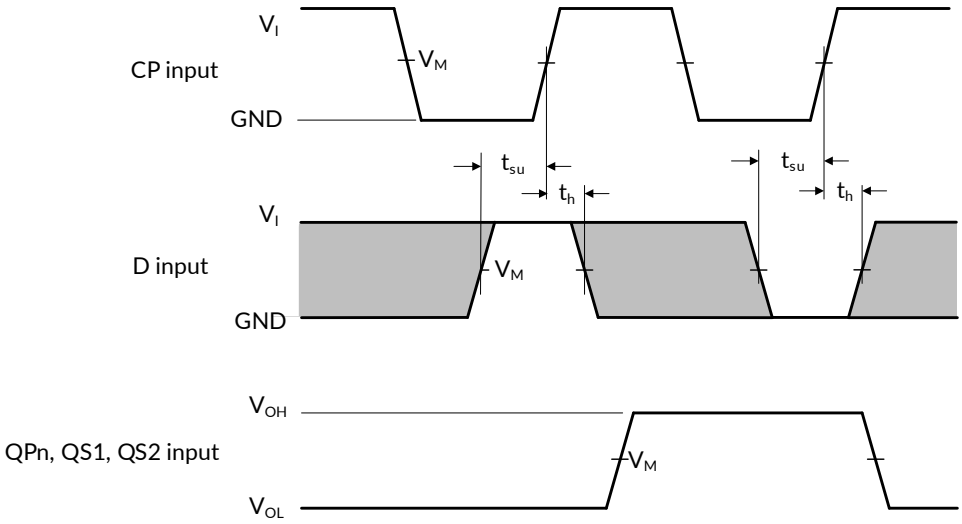
Measurement points are given in Table 1.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 2. Propagation delay strobe input (STR) to output (QPn), strobe input (STR) pulse width and the clock set-up and hold times for strobe input



Measurement points are given in Table 1.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 3. Enable and disable times

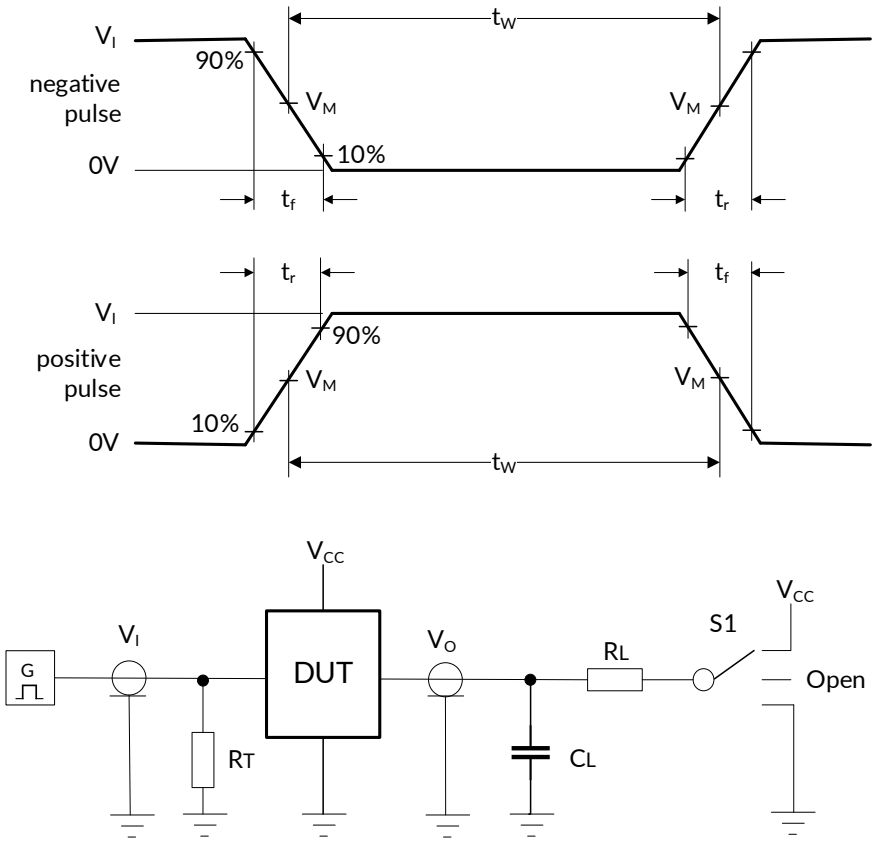


Measurement points are given in Table 1.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 4. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

Table 1. Measurement points

INPUT	OUTPUT		
V_M	V_M	V_x	V_y
$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{OH}$	$0.9V_{OH}$



Test data is given in Table 2.
Definitions test circuit:
R_T = Termination resistance should be equal to output impedance Zo of the pulse generator.
C_L = Load capacitance including jig and probe capacitance.
R_L = Load resistance.
S_1 = Test selection switch.

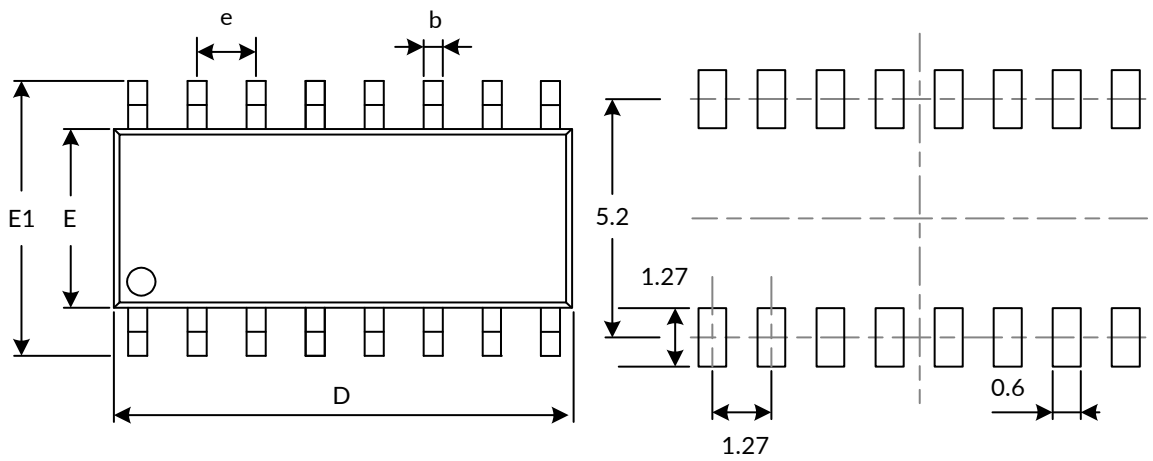
Figure 5. Test circuit for measuring switching times

Table 2. Test data

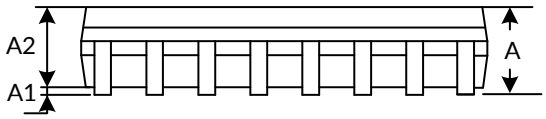
INPUT		LOAD		S1 POSITION		
V_I	t_r/t_f	C_L	R_L	t_{PLH}/t_{PHL}	t_{PHZ}/t_{PZH}	t_{PLZ}/t_{PZL}
V_{CC}	6ns	50pF	1kΩ	Open	GND	V_{CC}

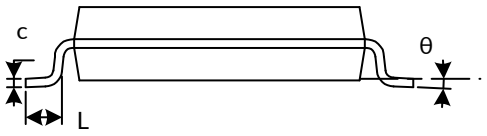
11 PACKAGE OUTLINE DIMENSIONS

SOP16 (3)



RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D (1)	9.800	10.200	0.386	0.402
E (1)	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC) (2)		0.050(BSC) (2)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

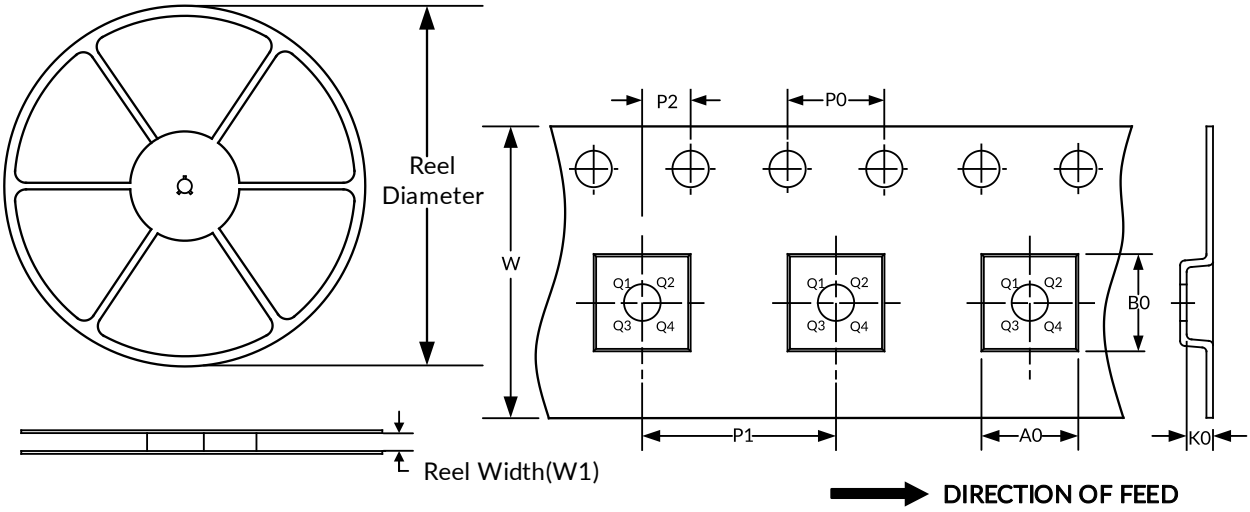
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP16	13”	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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