MP8853

2.85V to 18V, 4A, High-Efficiency, Wide-Input, Synchronous, Step-Down Converter with I²C Interface

DESCRIPTION

The MP8853 is a high-frequency, synchronous, rectified, step-down switch-mode converter with an I²C control interface. The MP8853 offers a fully integrated solution that achieves 4A of continuous output current (I_{OUT}) with excellent load and line regulation across a wide input voltage (V_{IN}) supply range.

The output voltage (V_{OUT}) can be controlled on the fly through an I²C serial interface. The reference voltage (V_{REF}) range can be adjusted from 0.6V to 1.108V in 4mV steps. The V_{OUT} slew rate, switching frequency (f_{SW}), current limit, hiccup/latch-off protection, enable, and power-save mode (PSM) can also be selected via the I²C interface.

Constant-on-time (COT) control provides fast transient response. An open-drain power good (PG) pin indicates when V_{OUT} is within the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8853 is available in a QFN-14 (3mmx3mm) package.

FEATURES

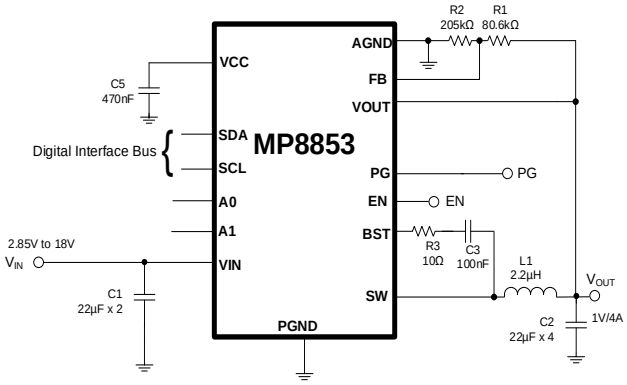
- Wide 2.85V to 18V Operating Input Voltage (V_{IN}) Range
- 4A of Continuous Output Current (I_{OUT})
- 1% Internal Reference Accuracy
- I²C-Configurable Reference Voltage (V_{REF}) Range from 0.6V to 1.108V in 4mV Steps with Slew Rate Control
- Default Forced Pulse-Width Modulation (PWM) Mode
- Selectable Pulse-Frequency Modulation (PFM)/PWM Mode via the I²C
- Adjustable Switching Frequency (f_{SW}) and Current Limit via the I²C
- 16 Selectable I²C Addresses
- Internal Soft Start (SS)
- Open-Drain Power Good (PG) Indication
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP) with Hiccup/Latch-Off Mode
- Output Voltage (V_{OUT}) Adjustable from 0.6V Up to 5.5V Using the FB Pin
- Available in a QFN-14 (3mmx3mm) Package

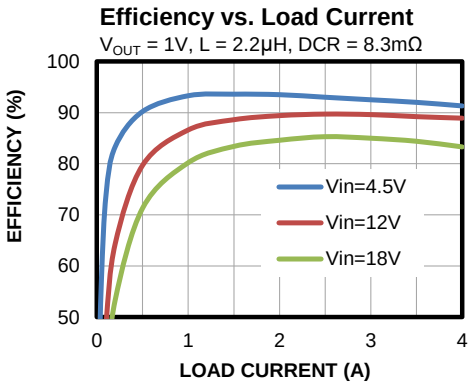
MPL Optimized Performance with MPL-AL MPS Inductor Series

APPLICATIONS

- Solid-State Drives (SSDs)
- Flat-Panel Televisions and Monitors
- Digital Set-Top Boxes
- Distributed Power Systems
- Networking/Servers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP8853GQ	QFN-14 (3mmx3mm)	*See Below*	1
EVKT-MP8853	Evaluation kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP8853GQ-Z).

TOP MARKING

BQKY

LLLL

BQK: Product code of MP8853GQ
Y: Year code
LLLL: Lot number

EVALUATION KIT EVKT-MP8853

EVKT-MP8853 kit contents (items can be ordered separately):

#	Part Number	Item	Quantity
1	EVL8853-Q-00A	MP8853GQ evaluation board	1
2	EVKT-USBI2C-02	Includes one USB-to-I^{2}C communication device, one USB cable, and one ribbon cable	1
3	Online resources	Include GUI installation file and supplemental documents	-

Order directly from MonolithicPower.com or our distributors.

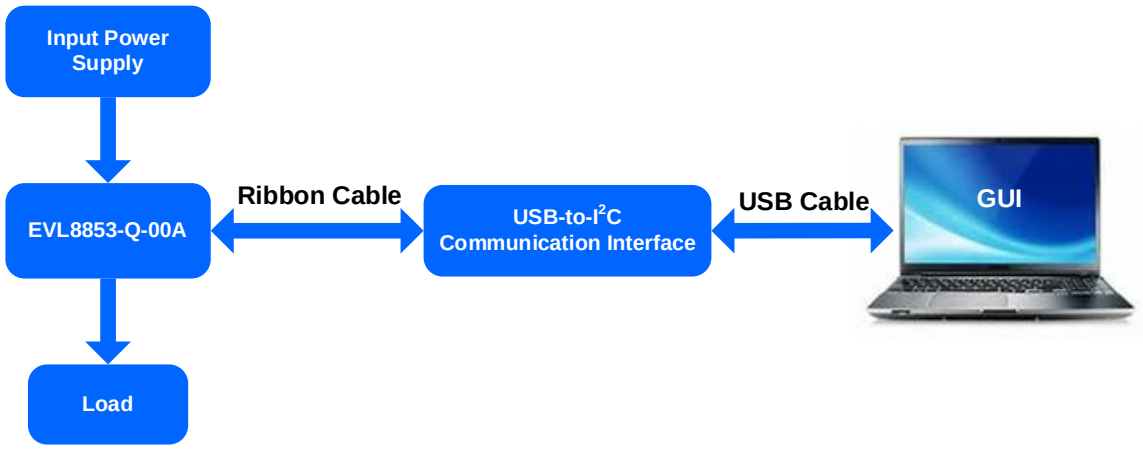
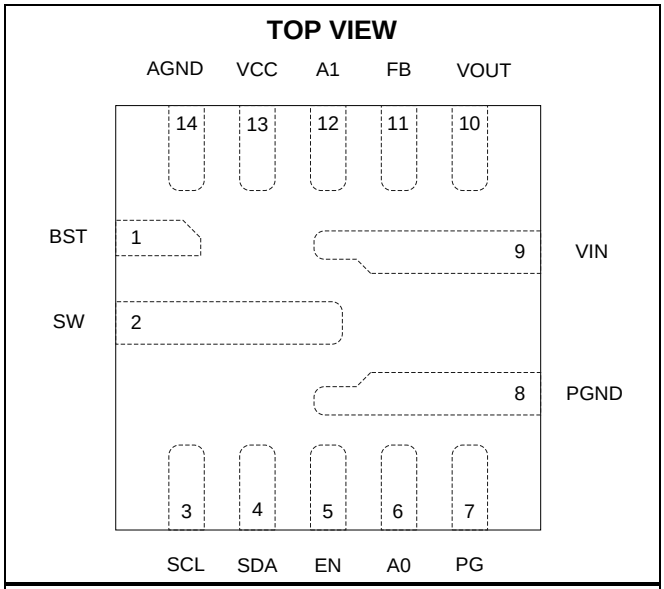


Figure 1: EVKT-MP8853 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-14 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** A capacitor must be placed between SW and BST to form a floating supply across the high-side MOSFET driver. For designs where the VCC decoupling capacitor layout cannot be optimized to the recommended layout, connect a 10Ω BST resistor in series with the BST capacitor.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	SCL	**I^2C serial clock.**
4	SDA	**I^2C serial data.**
5	EN	**Enable.** Set EN high to enable the MP8853. EN has a 1MΩ internal pull-down resistor connected to GND. EN is a high-voltage pin, so it can be connected directly to VIN for automatic start-up.
6	A0	**I^2C address set-up.** Connect a resistor divider from VCC to A0 to set different I^2C addresses. A0 can work with A1 to set 16 selectable I^2C addresses.
7	PG	**Power good indication.** The PG pin is an open-drain structure. PG de-asserts if the output voltage (V_{OUT}) is out of its regulation window.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage and requires special consideration during PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8853 operates from a 2.85V to 18V input rail. Decouple the input rail with a ceramic capacitor. Connect VIN using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the load's positive terminal.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. FB cannot be left floating.
12	A1	**I^2C address set-up.** Connect a resistor divider from VCC to A1 to set different I^2C addresses. A1 can work with A0 to set 16 selectable I^2C addresses.
13	VCC	**Internal LDO regulator output.** Decouple the VCC pin with a 0.47µF capacitor.
14	AGND	**Signal ground.** AGND is not connected to PGND internally. Ensure that AGND is connected to PGND in the PCB layout.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +19V
V_{SW}.....-0.6V (-6V for <10ns) to V_{IN} + 0.7V (+24V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
Output voltage (V_{OUT})..... 7V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2)
QFN-14 (3mmx3mm)..... 3.57W (2)
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.85V to 18V
Output voltage (V_{OUT}).....0.6V to 5.5V
Operating junction temp (T_J)..... -40°C to+125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (3mmx3mm)		
EVL8853-Q-00A (4)	35	6 °C/W
JESD51-7 (5)	55.5	55.8 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient, temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EVL8853-Q-00A, a 4-layer, 63.5mmx63.5mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2.1	4	μA
Supply current (quiescent)	I_Q	No switching, V_{FB} = 105% of V_{REF}, PFM mode		0.42	0.6	mA
		No switching, V_{FB} = 105% of V_{REF}, forced PWM mode		1.6	2.5	mA
High-side (HS) switch on resistance	$HS_{RDS(ON)}$	V_{BST} - V_{SW} = 3.3V		29		mΩ
Low-side (LS) switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		14		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V, T_J = 25°C			1	μA
Low-side valley current limit	I_{LIMIT_L}	Adjustable via the I²C		5.1		A
Low-side negative current limit	I_{LIMIT_LN}	In forced PWM mode or OVP state		-3.8		A
Switching frequency	f_{SW}	V_{OUT} = 2V, I_{OUT} = 0A, forced PWM mode	400	500	600	kHz
Minimum off time (7)	t_{OFF_MIN}			185		ns
Minimum on time (7)	t_{ON_MIN}			50		ns
Reference voltage	V_{REF}	T_J = 25°C	-1%	720	+1%	mV
		-40°C < T_J < 125°C (6)	-1.5%	720	+1.5%	
FB current	I_{FB}	V_{FB} = 740mV		10	50	nA
A0/A1 voltage threshold 1	V_{ADD_1}				24%	V_{CC}
A0/A1 voltage threshold 2	V_{ADD_2}		28%		49%	V_{CC}
A0/A1 voltage threshold 3	V_{ADD_3}		53%		72%	V_{CC}
A0/A1 voltage threshold 4	V_{ADD_4}		77%			V_{CC}
A0/A1 to GND pull-down resistor	R_{A0_PD} / R_{A1_PD}			1		MΩ
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN threshold hysteresis	V_{EN_HYS}			110		mV
EN-to-GND pull-down resistor	R_{EN}			1		MΩ
V_{IN} under-voltage lockout (UVLO) threshold rising	$V_{INUVVTH\_R}$		2.45	2.65	2.85	V
V_{IN} UVLO falling threshold	$V_{INUVVTH\_F}$			2.5	2.7	V
Power good (PG) under-voltage (UV) threshold rising	V_{PGUV-R}	Good	86%	90%	94%	V_{OUT}
PG UV threshold falling	V_{PGUV-F}	Fault	81%	85%	89%	V_{OUT}
PG over-voltage (OV) threshold rising	V_{PGOV-R}	Fault	111%	115%	119%	V_{OUT}
PG OV threshold falling	V_{PGOV-F}	Good	101%	105%	109%	V_{OUT}
PG deglitch time	t_{PGTD}	I²C-configurable		30		μs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over-voltage protection (OVP) rising threshold	V_{OVP_RISE}	V_{FB}	121%	125%	129%	V_{REF}
OVP falling threshold	$V_{OVP\_FALLING}$	V_{FB}	106%	110%	114%	V_{REF}
OVP delay	t_{OVP}			5		µs
Output pin absolute OV	V_{OVP2}		6	6.5	7	V
Under-voltage protection (UVP) threshold	$V_{FB\_UV\_th}$	Hiccup entry	45%	50%	55%	V_{REF}
UVP delay (7)	t_{UVP}			10		µs
Soft-start time	t_{SS}	0% to 100% of V_{OUT}		2		ms
VCC voltage	V_{CC}			3.5		V
VCC load regulation	V_{CC_REG}	I_{CC} = 20mA			3	%
Thermal shutdown (7)	T_{TSD}			160		°C
Thermal hysteresis (7)	T_{TSD_HYS}			20		°C

Notes:

6) Not tested in production. Derived by over-temperature correlation.
7) Derived by sample characterization. Not tested in production.

I/O LEVEL CHARACTERISTICS (8)

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	0.3 x V_{CC}	-0.5	0.3 x V_{CC}	V
High-level input voltage	V_{IH}		0.7 x V_{CC}	V_{CC} + 0.5	0.7 x V_{CC}	V_{CC} + 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{CC} > 2V	0.05 x V_{CC}		0.05 x V_{CC}		V
		V_{CC} < 2V	0.1 x V_{CC}		0.1 x V_{CC}		
Low-level output voltage (open drain) at 3mA sink current	V_{OL}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	0.2 x V_{CC}	0	0.2 x V_{CC}	
Low-level output current	I_{OL}			3		3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{ONL}	V_{OL} level, I_{OL} = 3mA		50		50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{ONH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50		50		kΩ
Pull-up current of the SCLH current source	I_{CS}	SCLH output levels between 30% and 70% of V_{CC}	2	6	2	6	mA
Rising time of the SCLH or SCL signal	t_{RCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Falling time of the SCLH or SCL signal	t_{FCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rising time of SDAH signal	t_{RDA}	Capacitive load from 10pF to 100pF	10	80			ns
		Capacitive load of 400pF	20	160	20	250	ns
Falling time of SDAH signal	t_{FDA}	Capacitive load from 10pF to 100pF	10	80			ns
		Capacitive load of 400pF	20	160	20	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O pin	I_I	Input voltage between 10% to 90% of V_{CC}		10	-10	+10	µA
Capacitance for each I/O pin	$C_{I/O}$			10		10	pF

I²C SPECIFICATIONS (8)

Parameter	Symbol	Condition	C_B = 100pF		C_B = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start command	t_{SU_STA}		160		600		ns
Hold time for a (repeated) start command	t_{HD_STA}		160		600		ns
Low period of the SCL clock	t_{LOW}		160		1300		ns
High period of the SCL clock	t_{HIGH}		60		600		ns
Data set-up time	t_{SU_DAT}		10		100		ns
Data hold time	t_{HD_DAT}		0	70	0		ns
Rising time of the SCLH signal	t_{RCL}		10	40	20 x 0.1 x C_B	300	ns
Rising time of the SCLH signal after a repeated start command and after an acknowledge bit	t_{FCL1}		10	80	20 x 0.1 x C_B	300	ns
Falling time of SCLH signal	t_{FCL}		10	40	20 x 0.1 x C_B	300	ns
Rising time of SDAH signal	t_{RDA}		10	80	20 x 0.1 x C_B	300	ns
Falling time of SDAH signal	t_{FDA}		10	80	20 x 0.1 x C_B	300	ns
Set-up time for stop command	t_{SU_STO}		160		600		ns
Bus free time between a stop and start command	t_{BUF}		160		1300		ns
Data valid time	t_{VD_DAT}			16		90	ns
Data valid acknowledge time	t_{VD_ACK}			160		900	ns
Capacitive load for each bus line	C_B	SDAH and SCLH line		100		400	pF
		SDAH + SDA line and SCLH + SCL line		400		400	pF
Noise margin at the low level	C_I	For each connected device		0.1 x V_{CC}	0.1 x V_{CC}		V
Noise margin at the high level	V_{NH}	For each connected device		0.2 x V_{CC}	0.2 x V_{CC}		V

Note:

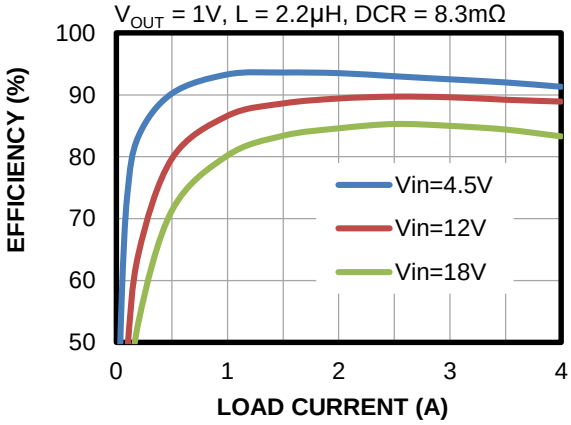
8) V_{CC} is the I²C bus voltage, which is within the 1.8V to 3.6V range. It is used for 1.8V, 2.5V, and 3.3V bus voltages.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

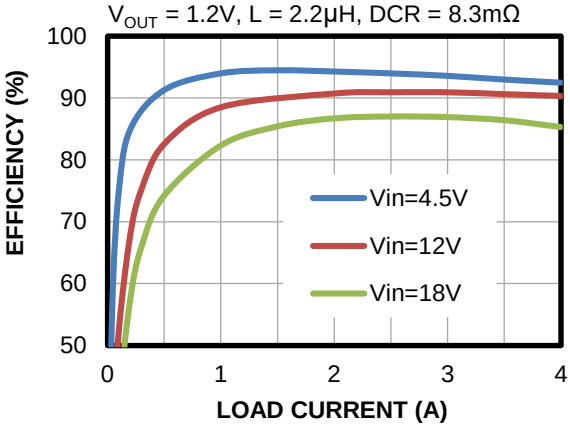
Efficiency vs. Load Current

V_{OUT} = 1V, L = 2.2µH, DCR = 8.3mΩ



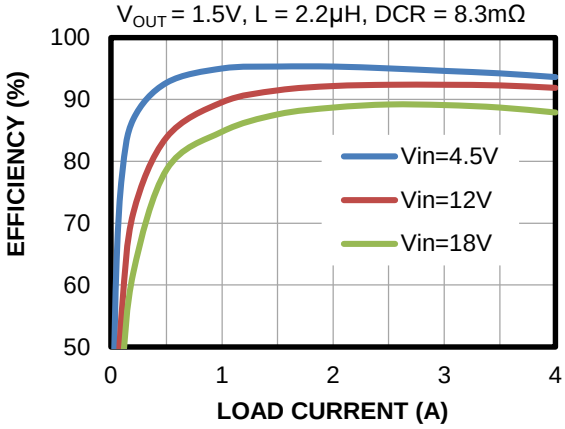
Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 2.2µH, DCR = 8.3mΩ



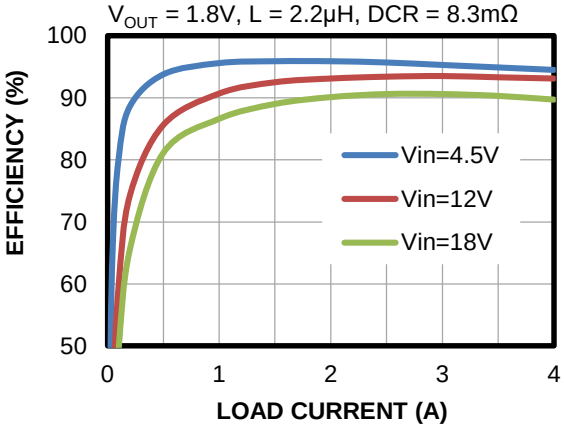
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 2.2µH, DCR = 8.3mΩ



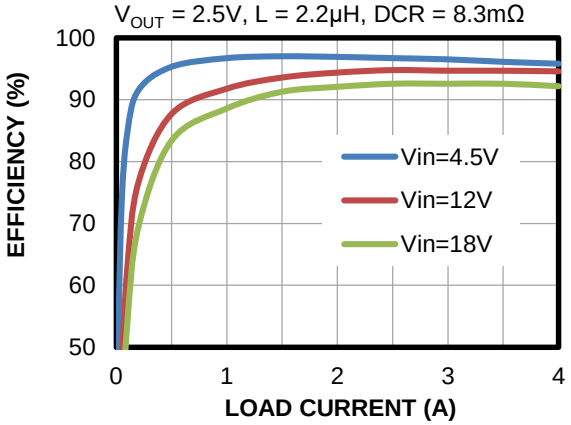
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 2.2µH, DCR = 8.3mΩ



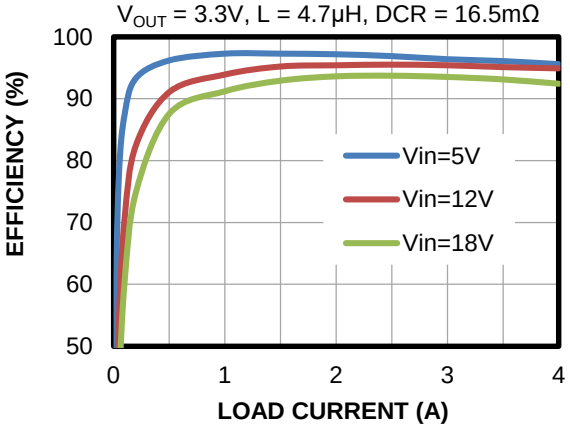
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 2.2µH, DCR = 8.3mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 4.7µH, DCR = 16.5mΩ

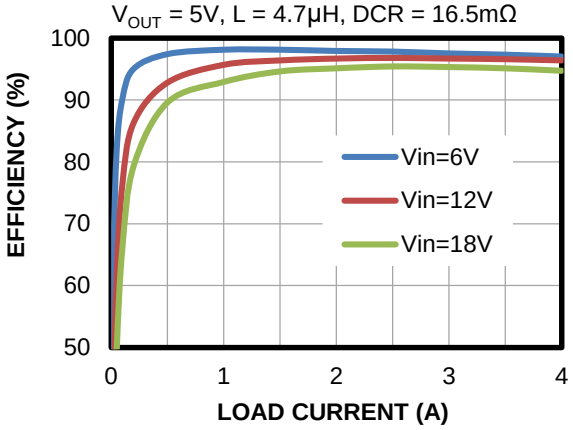


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

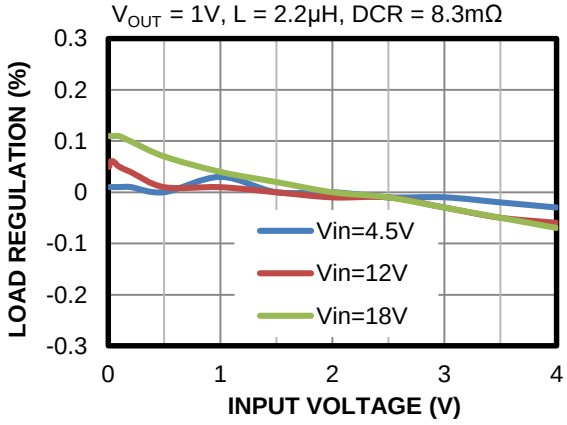
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 16.5mΩ



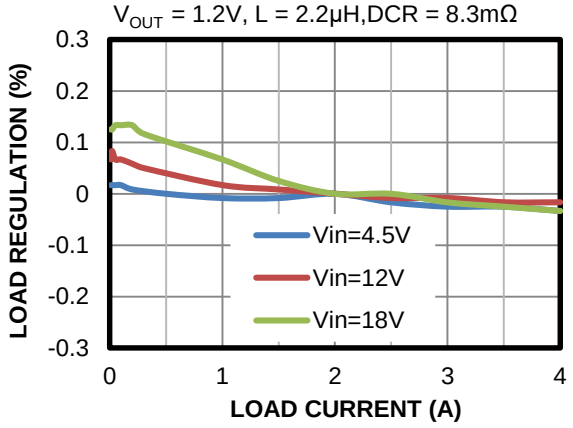
Load Regulation

V_{OUT} = 1V, L = 2.2µH, DCR = 8.3mΩ



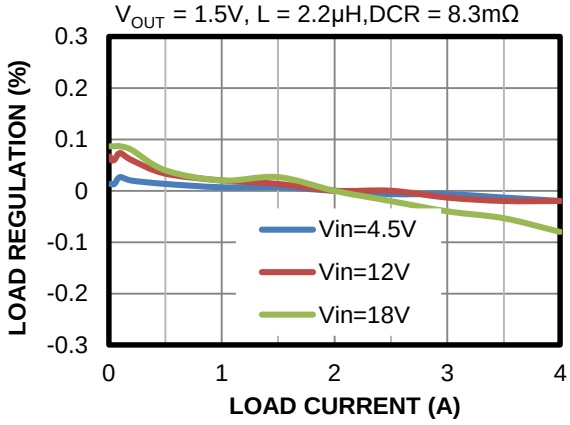
Load Regulation

V_{OUT} = 1.2V, L = 2.2µH,DCR = 8.3mΩ



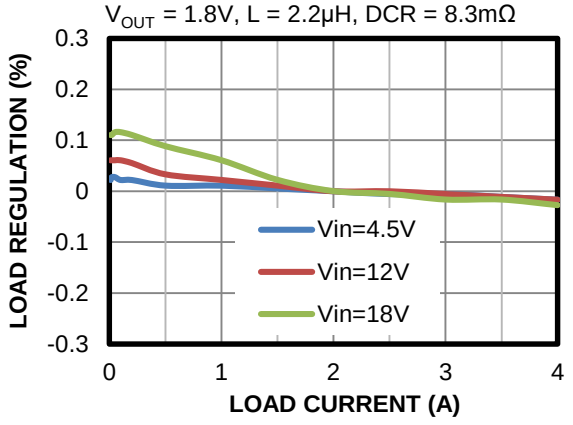
Load Regulation

V_{OUT} = 1.5V, L = 2.2µH,DCR = 8.3mΩ



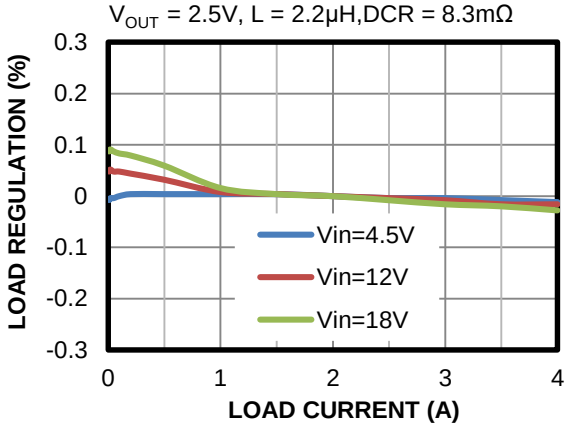
Load Regulation

V_{OUT} = 1.8V, L = 2.2µH, DCR = 8.3mΩ



Load Regulation

V_{OUT} = 2.5V, L = 2.2µH,DCR = 8.3mΩ

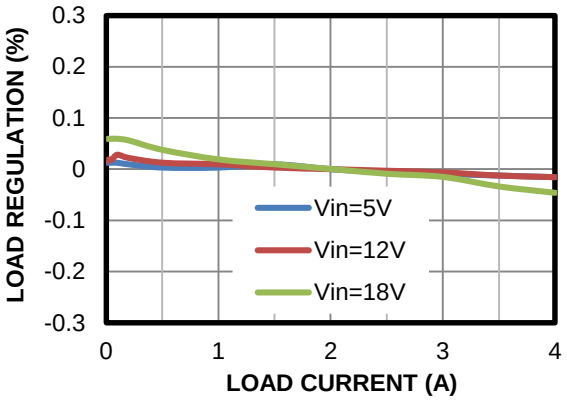


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

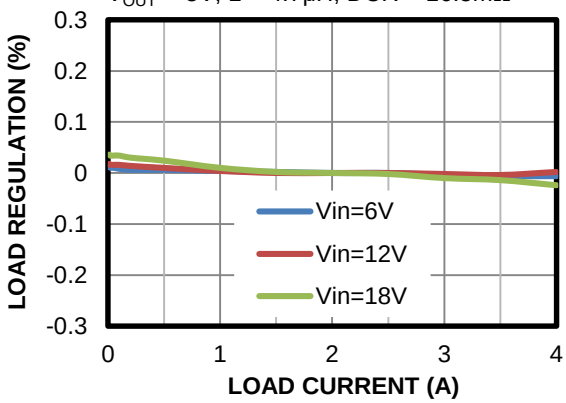
Load Regulation

V_{OUT} = 3.3V, L = 4.7µH, DCR = 16.5mΩ



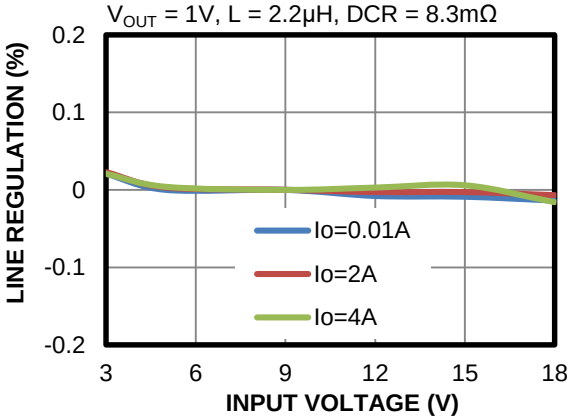
Load Regulation

V_{OUT} = 5V, L = 4.7µH, DCR = 16.5mΩ

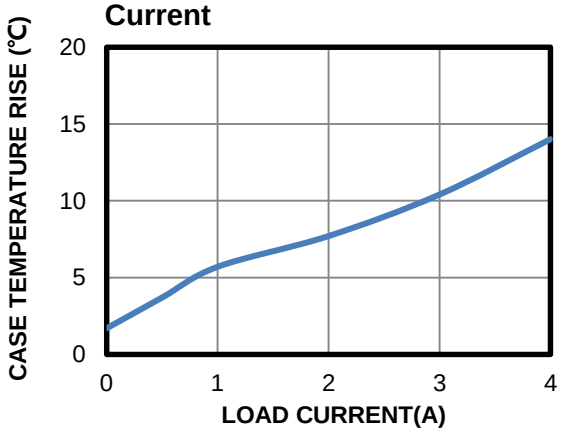


Line Regulation

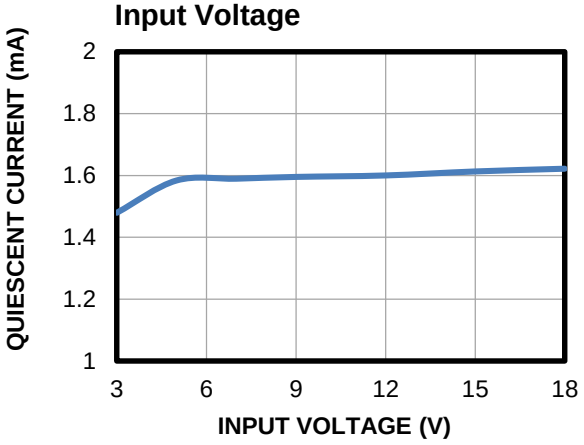
V_{OUT} = 1V, L = 2.2µH, DCR = 8.3mΩ



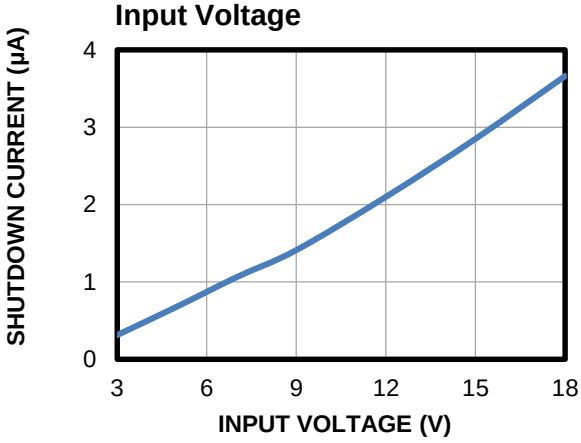
Case Temperature Rise vs. Load Current



Quiescent Supply Current vs. Input Voltage



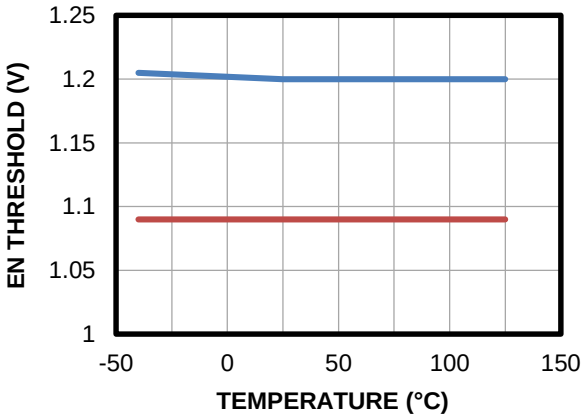
Shutdown Supply Current vs. Input Voltage



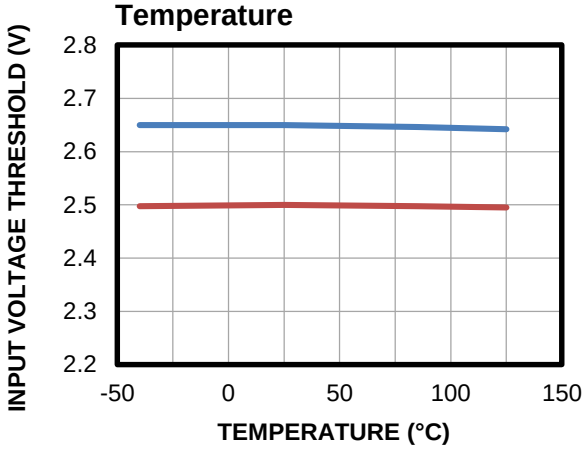
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

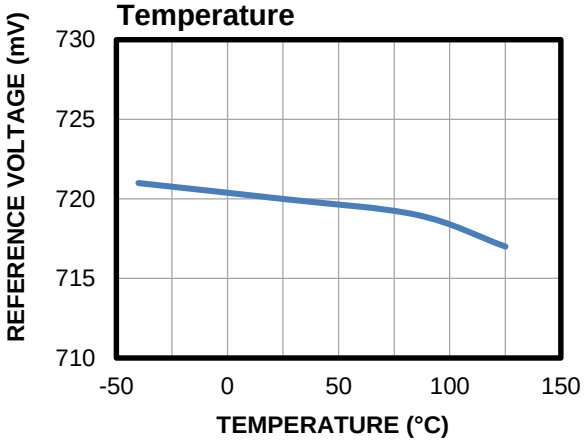
EN Threshold vs. Temperature



Input Voltage Threshold vs. Temperature



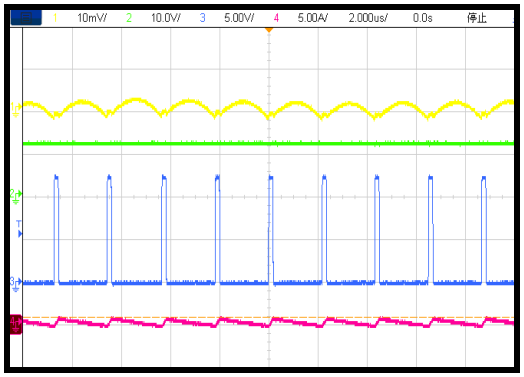
Reference Voltage vs. Temperature



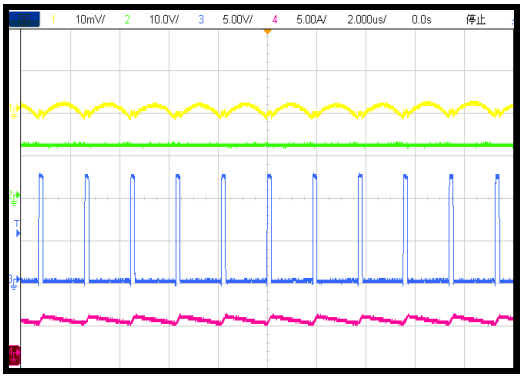
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

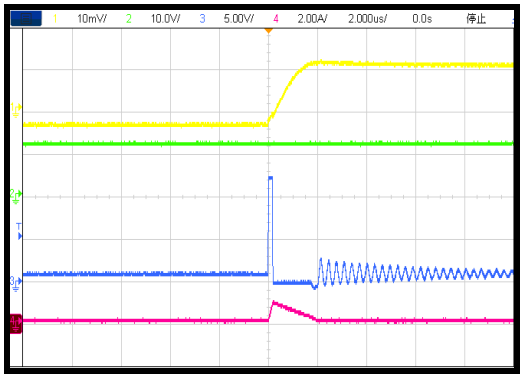
Steady State
I_{OUT} = 0A



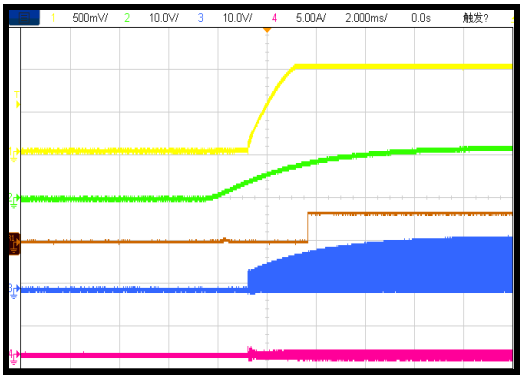
Steady State
I_{OUT} = 4A



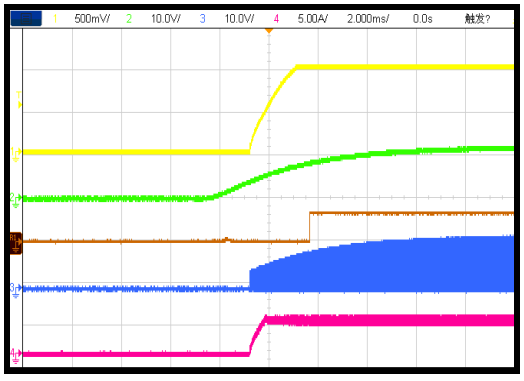
Steady State
PFM mode, I_{OUT} = 0A



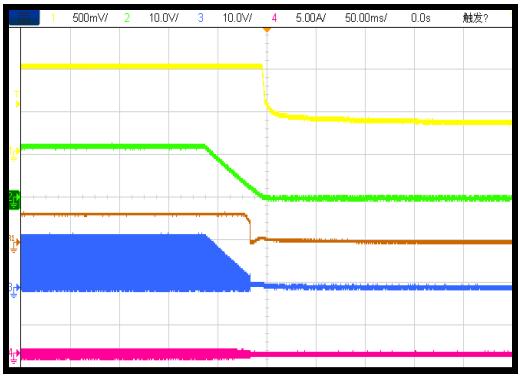
Input Power Start-Up
I_{OUT} = 0A



Input Power Start-Up
I_{OUT} = 4A



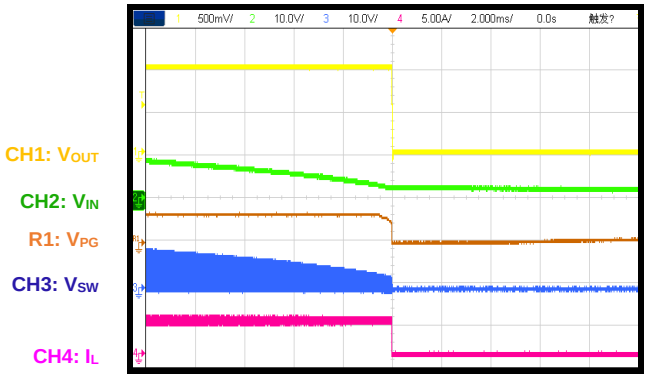
Input Power Shutdown
I_{OUT} = 0A



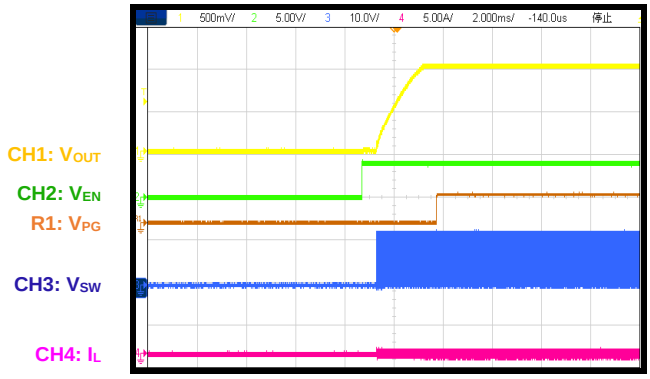
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

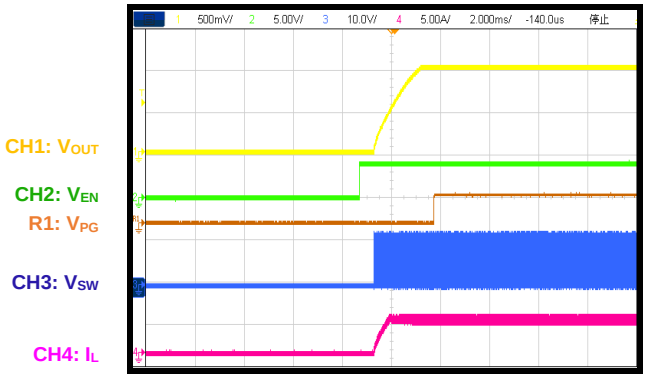
Input Power Shutdown
I_{OUT} = 4A



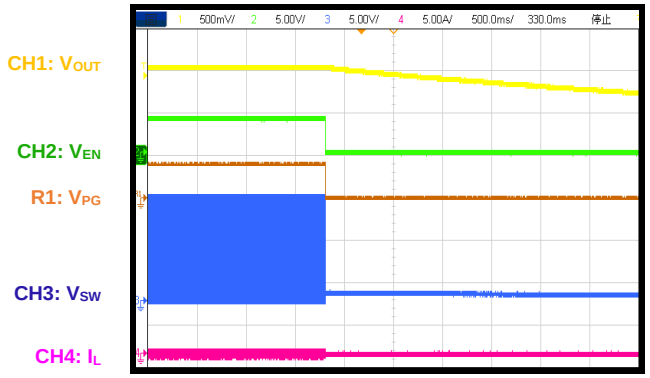
Start-Up through EN
I_{OUT} = 0A



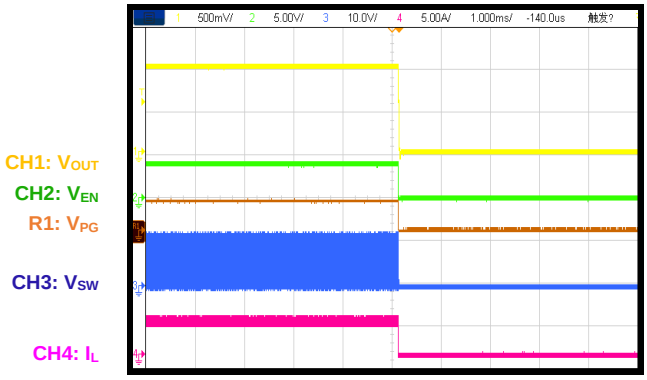
Start-Up through EN
I_{OUT} = 4A



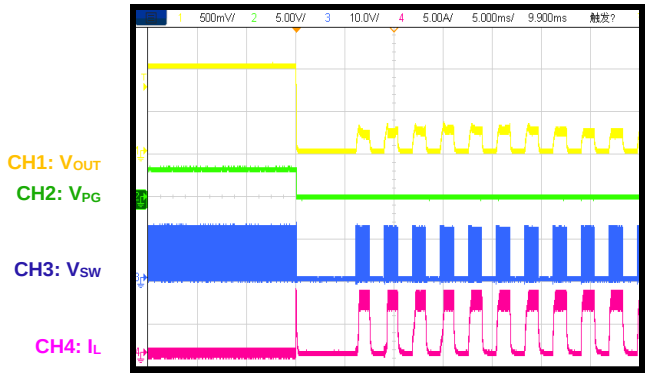
Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 4A



SCP Entry
I_{OUT} = 0A

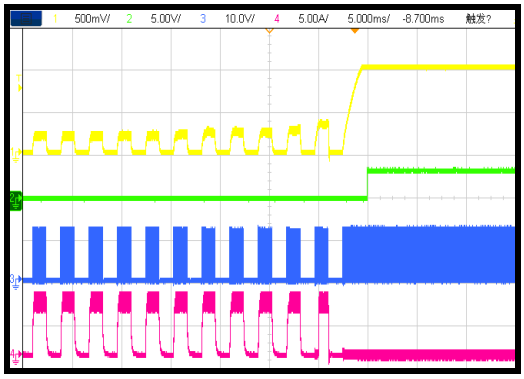


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

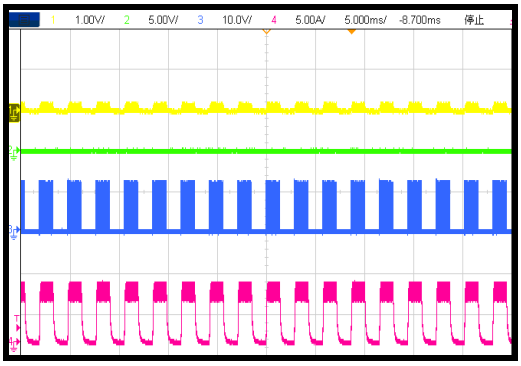
Performance waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1V, L = 2.2µH, f_{SW} = 500kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

SCP Recovery

I_{OUT} = 0A

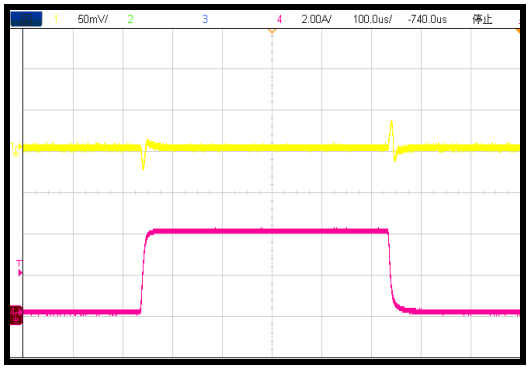


SCP Steady State



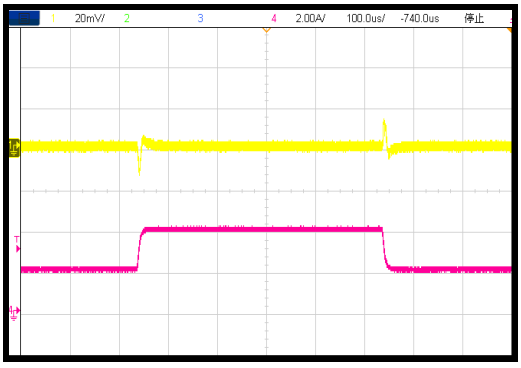
Load Transient Response

I_{OUT} = 0A to 4A, 2.5A/µs with e-load



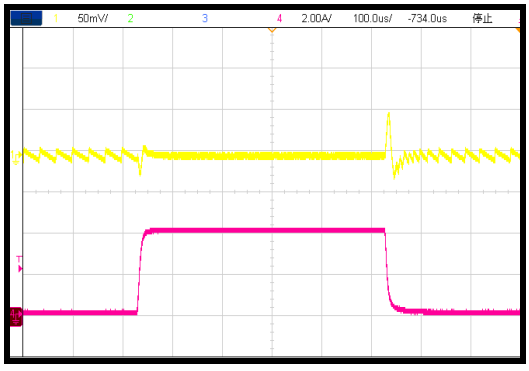
Load Transient Response

I_{OUT} = 2A to 4A, 2.5A/µs with e-load



Load Transient Response

PFM mode, I_{OUT} = 0A to 4A, 2.5A/µs with E-load



FUNCTIONAL BLOCK DIAGRAM

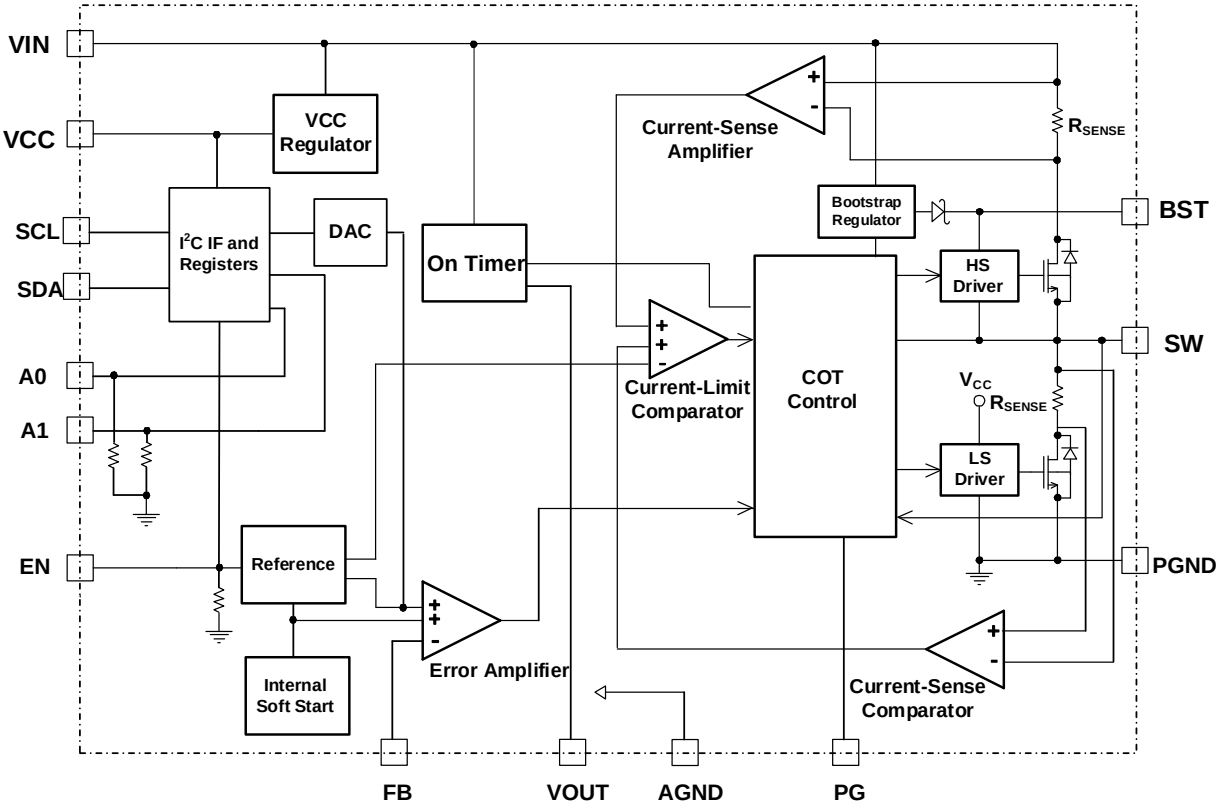


Figure 2: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MP8853 is a fully integrated, synchronous, rectified, step-down switch-mode converter. The MP8853 uses constant-on-time (COT) control to provide fast transient response and facilitate loop stabilization. Figure 3 shows the simplified ramp compensation block.

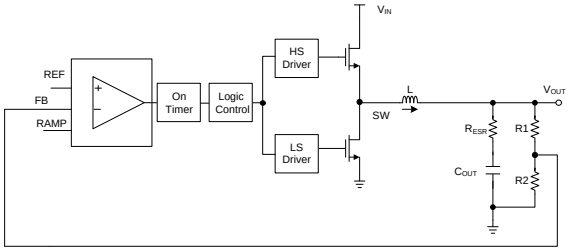


Figure 3: Simplified Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{RAMP}) is below the error amplifier's output voltage (V_{EAO}), which indicates an insufficient output voltage (V_{OUT}). The on period is determined by both V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the V_{IN} range.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET's on and off state, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are turned on at the same time, causing a dead short between the input and GND, which reduces efficiency dramatically. The MP8853 prevents shoot-through by generating a dead time (DT) internally between the HS-FET off and LS-FET on period, and the LS-FET off and HS-FET on period. The MP8853 enters either heavy-load operation or light-load operation depending on the amplitude of the output current (I_{OUT}).

Switching Frequency (f_{SW})

The MP8853 uses COT control, so there is no dedicated oscillator in the IC. V_{IN} is fed into the one-shot on-timer through the internal frequency resistor. The duty ratio is V_{OUT} / V_{IN}, and f_{SW} is fairly constant across the V_{IN} range.

The MP8853's f_{SW} can be adjusted via the I²C interface (SYSCNTLREG2 (02h), bits[5:4]).

When V_{OUT} is set too low and V_{IN} is high, the switching on time may be limited by the internal minimum on time limit, and f_{SW} decreases. Table 1 shows the maximum f_{SW} vs. V_{OUT} when V_{IN} = 12V and V_{IN} = 5V.

Table 1: Maximum Frequency Selection vs. Output Voltage

	Maximum Frequency Selection	
V_{OUT} (V)	V_{IN} = 12V	V_{IN} = 5V
5	1.25MHz	-
3.3	1.25MHz	1.25MHz
2.5	1.25MHz	1.25MHz
1.8	1.25MHz	1.25MHz
1.5	1.25MHz	1.25MHz
1.2	1MHz	1.25MHz
1	750kHz	1.25MHz
0.9	750kHz	1.25MHz
0.6	500kHz	1.25MHz

Forced PWM Operation

When the MP8853 works in forced pulse-width modulation (PWM) mode, the MP8853 enters continuous conduction mode (CCM), where the HS-FET and LS-FET repeat the on/off operation, even if the inductor current (I_L) is zero or a negative value. Meanwhile, f_{SW} is fairly constant. Figure 4 shows the timing diagram during PWM operation.

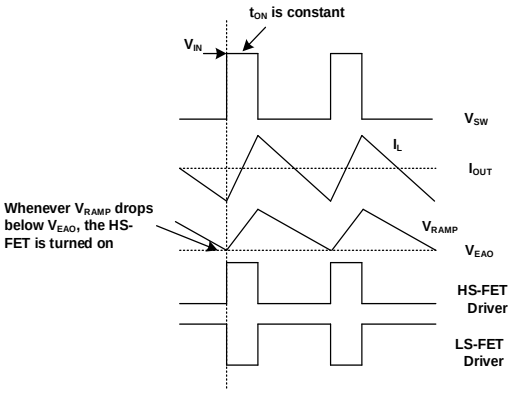


Figure 4: Forced PWM Operation

Light-Load Operation

When the MP8853 works in automatic pulse-frequency modulation (PFM) mode during light-load operation, the MP8853 reduces f_{SW} automatically to maintain high efficiency, and I_L drops.

When I_L reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 5). The output capacitors discharge slowly to GND through R1 and R2. This operation greatly improves efficiency when I_{OUT} is low.

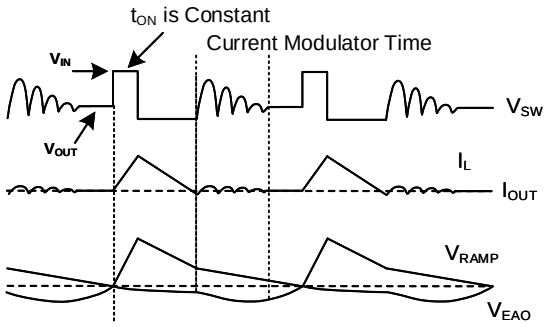


Figure 5: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of I_{OUT}. As I_{OUT} increases, the current modulator's regulation time period becomes shorter; this means that the HS-FET turns on more frequently, and f_{SW} increases. I_{OUT} reaches critical levels when the current modulator time is zero. I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The MP8853 reverts to PWM mode once I_{OUT} exceeds the critical level. Afterward, f_{SW} remains fairly constant across the I_{OUT} range.

The MP8853 can operate in PFM mode under light loads to improve efficiency (low-power mode). The MP8853 can also operate in forced PWM mode under any load condition. The mode can be selected via I^2C control. To enable low-power mode, set the MODE bit to 1. To disable low-power mode, set the MODE bit to 0, and the converter works in forced PWM mode. The MODE bit is set to 0 (forced PWM) by default.

Operating without an External Ramp

The traditional constant-on-time (COT) control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to be an effective current-sense resistor.

The MP8853 has built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. A solution using only ceramic capacitors can reduce the output ripple, total BOM cost, and board area significantly.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitry. This regulator takes the VIN input and operates across the full V_{IN} range. After EN is pulled high and V_{IN} exceeds 3.5V, the output of the regulator is in full regulation. When V_{IN} is below 3.5V, V_{OUT} decreases and follows V_{IN}. A 0.47µF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage (V_{FB}) against the internal 0.6V reference voltage (V_{REF}) and outputs a PWM signal. V_{REF} can be configured from 0.6V to 1.108V via the I^2C. Optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

Enable (EN)

EN is a digital control pin that turns the regulator, including the I^2C block, on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1MΩ resistor is connected from EN to ground. EN can operate with an 18V input voltage, which allows EN to be directly connected to VIN for automatic start-up. When the external EN is high, set the EN bit in the SYSCNTLREG1 (01h) register to 0 to stop the HS-FET and LS-FET from switching. The MP8853 resumes switching by setting the EN bit to 1.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8853's UVLO comparator monitors V_{IN} and the output voltage of the VCC regulator. The MP8853 is active when both voltages exceed the UVLO rising threshold.

Pre-Bias Start-Up and Soft Stop

If the output of the MP8853 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed output voltage at FB.

The MP8853 also provides a selectable soft-stop function, which defines the output discharge behavior after EN shutdown. By default, the output is not controlled after EN shutdown. If the SOFT_STOP bit (SYSCNTLREG2 (02h), bit[3]) is set to 1 via the I^2C, the output discharges linearly to zero.

Over-Current Protection (OCP)

By default, the MP8853 has cycle-by-cycle over-current limit control with hiccup mode. The current-limit circuit employs both high-side current limits and a low-side valley current-sensing algorithm. The MP8853 uses the on resistance ($R_{DS(ON)}$) of the LS-FET as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal exceeds the current-limit threshold, the PWM on pulse is terminated, and the LS-FET turns on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current-sensing node, so GND should be connected to the source terminal of the bottom MOSFET. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit is reached, V_{OUT} drops until it falls below the under-voltage (UV) threshold (typically 50% of V_{REF}). Once the UV condition is triggered, the MP8853 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP8853 exits hiccup mode once the OC condition is removed.

Short the output to ground first, and then start on the part. The MP8853's I^2C is disabled under this condition. The I^2C resumes operation after the short circuit is removed. When the HICCCUP_OCP bit (SYSCNTLREG1 (01h), bit[1]) is set to 0 by the I^2C, the device latches off if OCP is triggered, and V_{FB} UVP is triggered.

Power Good (PG)

The power good (PG) pin indicates whether V_{FB} is in the normal range compared to the internal reference voltage. PG is an open-drain structure. An external pull-up supply is required. During start-up, the PG output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce inrush current at start-up.

When V_{FB} exceeds 90% and is below 115% of the internal V_{REF} and the soft start is finished, then the PG signal is pulled high. When V_{FB} is below 85% after soft start finishes, the PG signal remains low. When V_{FB} exceeds 115% of the internal V_{REF}, PG switches low. The PG signal rises high again after V_{FB} drops below 105% of V_{REF}.

PG implements an adjustable deglitch time via the I^2C whenever V_{OUT} crosses the UV / over-voltage (OV) rising and falling threshold. This guarantees the correct indication when the FB voltage is scaled through the I^2C.

The PG output is pulled low immediately when EN UVLO, input UVLO, OCP, or over-temperature protection (OTP) is triggered.

Input Over-Voltage Protection (V_{IN} OVP)

The MP8853 monitors V_{IN} to detect an input OV event. This function is active only when V_{FB} exceeds 125% of V_{REF}. When the output is in an over-voltage protection (OVP) condition, the LS-FET turns on to discharge the output. In this scenario, the MP8853 works as a boost converter and may charge VIN until VIN is too high. When V_{IN} exceeds the input OVP threshold, both the HS-FET and LS-FET stop switching.

Output Over-Voltage Protection (OVP)

The MP8853 monitors both V_{FB} and V_{OUT} to detect an OV event. An internal comparator monitors V_{FB}. When V_{FB} exceeds 125% of the internal V_{REF}, the controller enters dynamic regulation mode, and V_{IN} may be charged up during this time.

When input OVP is triggered, the IC stops switching. If OVP mode is set to automatic retry via the I^2C, the IC begins switching once V_{IN}

drops below the V_{IN} OVP recovery threshold. Otherwise, the MP8853 latches off. OVP automatic retry mode or latch-off mode occurs only if the soft start has finished.

Dynamic regulation mode can be operated by turning on the LS-FET until the low-side negative current limit is triggered. Then the body diode of the HS-FET free-wheels the current.

The output power charges the input, which may trigger the V_{IN} OVP function. If V_{IN} OVP occurs, neither the HS-FET or LS-FET turn on, and they stop charging V_{IN}. If the output is still experiencing an OV condition and V_{IN} drops below the V_{IN} OVP threshold, repeat the operation. If V_{OUT} is below 110% of the internal V_{REF}, then the MP8853 exits output OVP.

Output Absolute Over-Voltage Protection (OVP_ABS)

The MP8853's V_{OUT} can be adjusted by the output reference voltage and the external resistor dividers. The MP8853's V_{OUT} must be below the absolute OVP threshold (typically 6.5V). The MP8853 monitors V_{OUT} to detect absolute OVP. When V_{OUT} exceeds 6.5V, the controller enters dynamic regulation mode if the RETRY_OVP bit (SYSCNTLREG1 (01h), bit[2]) is set to 1. Otherwise, the MP8853 latches off when output OVP and input OVP are both triggered. Absolute OVP works once V_{IN} and EN exceed their rising thresholds. This means that this function can work even during a soft start.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 140°C), the chip is enabled again.

STATUS (06h), bits[2:1] can be monitored for more information regarding the IC's silicon temperature.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. Its UVLO rising threshold is 2.4V with a 150mV hysteresis. The bootstrap capacitor's voltage is regulated by V_{IN} internally through D1, M1, C3, L1, and C2 (see Figure 6). If V_{BST} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C3.

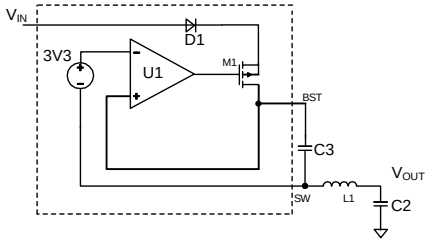


Figure 6: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If V_{IN}, V_{CC}, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitry. Several events can shut down the chip: EN going low, V_{IN} going low, V_{CC} going low, thermal shutdown, OVP latch-off mode, and OCP latch-off mode. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{EAO} and the internal supply rail are then pulled down.

I²C Control and Default Output Voltage

When the MP8853 is enabled, V_{OUT} is determined by the FB resistors with a soft-start time. Afterward, the I²C bus can communicate with the master. If the chip does not receive a continuous I²C communication signal, the MP8853 can work through FB and perform a behavior similar to a traditional non-I²C part. V_{OUT} is determined by the resistor dividers R1 and R2, as well as the FB reference voltage. V_{OUT} can be calculated with Equation (2):

$$V_{OUT} = V_{REF} \times (\frac{R1+R2}{R2}) \quad (2)$$

V_{OUT} cannot be set above the absolute OVP threshold (typically 6.5V).

I²C Slave Address

To support multiple devices using the same I²C bus, the A0 and A1 pins can be used to select 16 different addresses.

A resistor divider connected from VCC to GND can achieve an accurate reference voltage on A0 and A1. Connect A0 and A1 to this reference voltage to set a different I²C slave address (see Figure 7). The internal circuit changes the I²C address accordingly.

When the master sends an 8-bit address value, the 7-bit I²C address should be followed by 0 or 1 to indicate a write or read operation, respectively. Table 2 shows the recommended I²C address selection by the A0 and A1 divide resistors.

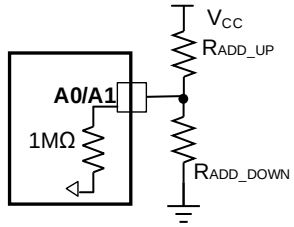


Figure 7: I²C Slave Address Selection Set-Up

Table 2: Recommended I²C Slave Address Selection by A0 and A1 Resistor Divider

A0 Upper Resistor: R_{A0_UP} (kΩ)	A0 Lower Resistor: R_{A0_DOWN} (kΩ)	A1 Upper Resistor: R_{A1_UP} (kΩ)	A1 Lower Resistor: R_{A1_DOWN} (kΩ)	I²C Slave Address (Hex)
No connection	No connection	No connection	No connection	60h
No connection	No connection	470	360	61h
No connection	No connection	360	1000	62h
No connection	No connection	100	No connection	63h
470	360	No connection	No connection	64h
470	360	470	360	65h
470	360	360	1000	66h
470	360	100	No connection	67h
360	1000	No connection	No connection	68h
360	1000	470	360	69h
360	1000	360	1000	6Ah
360	1000	100	No connection	6Bh
100	No connection	No connection	No connection	6Ch
100	No connection	470	360	6Dh
100	No connection	360	1000	6Eh
100	No connection	100	No connection	6Fh

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8853 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 8).

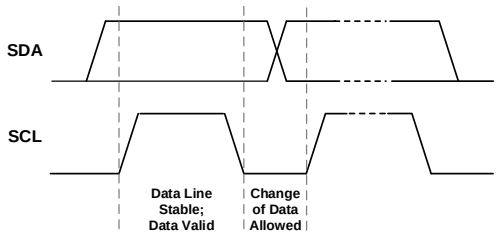


Figure 8: Bit Transfer on the I²C Bus

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

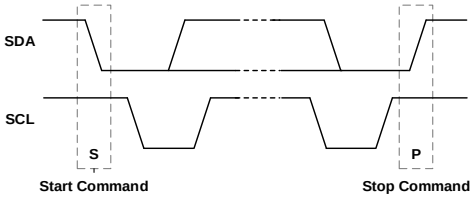


Figure 9: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered to be busy after the start command, and it is considered to be free again after a minimum of 4.7µs after the stop command. The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable and low during the high period of the clock pulse.

Figure 10 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

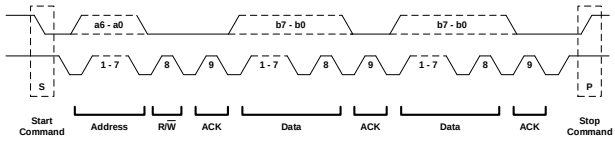


Figure 10: Complete Data Transfer

The MP8853 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8853 acknowledges this by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8853. The MP8853 performs an update on the falling edge of the least significant bit (LSB) byte.

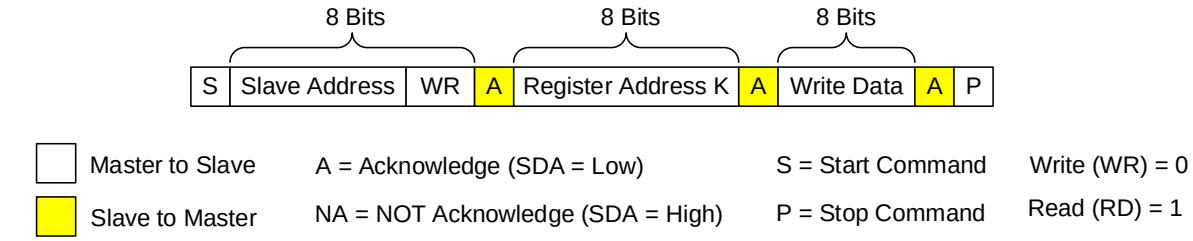


Figure 11: I²C Write Example (Write Register)

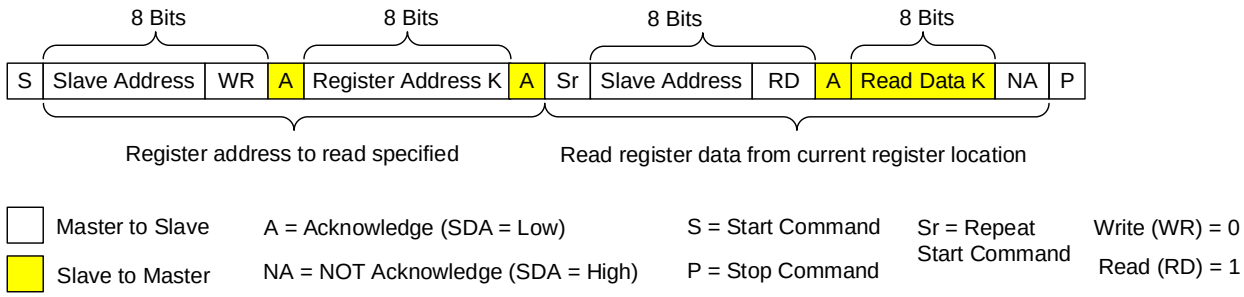


Figure 12: I²C Read Example (Read Register)

REGISER DESCRIPTION

Register Map

The MP8853 contains 6 write or read registers.

VSEL (00h) selects the output reference voltage. SYSCNTLREG1 (01h) is the first system control register and can be used to set the slew rate and hiccup over-current protection (OCP). SYSCNTLREG2 (02h) is the second system control register that can be used to set the switching frequency and current limit. OUTPUT_CURRENT (03h) and OUTPUT_VOLTAGE (04h) indicate the output current and output voltage, respectively. ID1 (05h) returns the IC's ID register. STATUS (06h) indicates the IC's protection status.

The register map is shown below.

ADD	Command Name	Type	Bytes	D7	D6	D5	D4	D3	D2	D1	D0
00h	VSEL	R/W	1	RESERVED	OUTPUT_REFERENCE_VOLTAGE						
01h	SYSCNTLREG1	R/W	1	EN	GO_BIT	SLEW_RATE			RETRY_OVP	HICCUP_OCP	MODE
02h	SYSCNTLREG2	R/W	1	PG_DEGLITCH_TIME		SWITCHING_FREQUENCY		SOFT_STOP	CURRENT_LIMIT		
03h	OUTPUT_CURRENT	R	1	OUTPUT_CURRENT							
04h	OUTPUT_VOLTAGE	R	1	OUTPUT_VOLTAGE							
05h	ID1	R	1	VENDOR_ID				IC_REVISION_ID			
06h	STATUS	R	1	RESERVED				OC	OTEW	OT	PG

Register Description

VSEL (00h)

The VSEL command selects the output V_{REF}. The MP8853's default output voltage is determined by the FB resistor divider after the MP8853's power start-up or EN start-up. This reference voltage can be set between 0.6V and 1.108V. Before adjusting the output reference voltage, GO_BIT (SYSCNTLREG1 (01h), bit[6]) should be set to 1, and then the reference voltage can be adjusted by bits[6:0] of this command.

When the output reference voltage setting command is finished, GO_BIT automatically resets to 0 to prevent false operation of the V_{OUT} scaling.

Bits	Access	Bit Name	Default	Description
7	R/W	RESERVED	1	Reserved.
6:0	R/W	OUTPUT_REFERENCE_VOLTAGE	001 1110	Sets the output V_{REF} from 0.6V to 1.108V (see Table 3 on page 27). The default value is 0.72V.

Table 3 on page 27 shows the output reference voltage selection chart from 0.6V to 1.108V via the I^2C.

Table 3: Output V_{REF} Selection Chart

Bits [6:0]	V_{REF} (V)	Bits[6:0]	V_{REF} (V)	Bits [6:0]	V_{REF} (V)	Bits[6:0]	V_{REF} (V)
000 0000	0.6	010 0000	0.728	100 0000	0.856	110 0000	0.984
000 0001	0.604	010 0001	0.732	100 0001	0.86	110 0001	0.988
000 0010	0.608	010 0010	0.736	100 0010	0.864	110 0010	0.992
000 0011	0.612	010 0011	0.74	100 0011	0.868	110 0011	0.996
000 0100	0.616	010 0100	0.744	100 0100	0.872	110 0100	1
000 0101	0.62	010 0101	0.748	100 0101	0.876	110 0101	1.004
000 0110	0.624	010 0110	0.752	100 0110	0.88	110 0110	1.008
000 0111	0.628	010 0111	0.756	100 0111	0.884	110 0111	1.012
000 1000	0.632	010 1000	0.76	100 1000	0.888	110 1000	1.016
000 1001	0.636	010 1001	0.764	100 1001	0.892	110 1001	1.02
000 1010	0.64	010 1010	0.768	100 1010	0.896	110 1010	1.024
000 1011	0.644	010 1011	0.772	100 1011	0.9	110 1011	1.028
000 1100	0.648	010 1100	0.776	100 1100	0.904	110 1100	1.032
000 1101	0.652	010 1101	0.78	100 1101	0.908	110 1101	1.036
000 1110	0.656	010 1110	0.784	100 1110	0.912	110 1110	1.04
000 1111	0.66	010 1111	0.788	100 1111	0.916	110 1111	1.044
001 0000	0.664	011 0000	0.792	101 0000	0.92	111 0000	1.048
001 0001	0.668	011 0001	0.796	101 0001	0.924	111 0001	1.052
001 0010	0.672	011 0010	0.8	101 0010	0.928	111 0010	1.056
001 0011	0.676	011 0011	0.804	101 0011	0.932	111 0011	1.06
001 0100	0.68	011 0100	0.808	101 0100	0.936	111 0100	1.064
001 0101	0.684	011 0101	0.812	101 0101	0.94	111 0101	1.068
001 0110	0.688	011 0110	0.816	101 0110	0.944	111 0110	1.072
001 0111	0.692	011 0111	0.82	101 0111	0.948	111 0111	1.076
001 1000	0.696	011 1000	0.824	101 1000	0.952	111 1000	1.08
001 1001	0.7	011 1001	0.828	101 1001	0.956	111 1001	1.084
001 1010	0.704	011 1010	0.832	101 1010	0.96	111 1010	1.088
001 1011	0.708	011 1011	0.836	101 1011	0.964	111 1011	1.092
001 1100	0.712	011 1100	0.84	101 1100	0.968	111 1100	1.096
001 1101	0.716	011 1101	0.844	101 1101	0.972	111 1101	1.1
001 1110	0.72	011 1110	0.848	101 1110	0.976	111 1110	1.104
001 1111	0.724	011 1111	0.852	101 1111	0.98	111 1111	1.108

SYSCNTLREG1 (01h)

The SYSCNTLREG1 command is the first system control register that turns the device on and off. It also sets I^2C writing authority for the output reference command, slew rate, and certain protection modes.

Bits	Access	Bit Name	Default	Description
7	R/W	EN	1	Turns the device on or off when the external EN is high. When the external EN is low, the converter is off, and the I^2C shuts down. 0: Off 1: On

6	R/W	GO_BIT	0	Enables I^2C writing authority for the output reference command (VSEL (00h), bits[6:0]). Set GO_BIT to 1 to enable I^2C authority to write the output reference. The IC switches to forced PWM mode when GO_BIT is set to 1 to achieve a smooth output waveform during the output's dynamic scaling. When the command is finished, GO_BIT automatically resets to 0 to prevent false operation of the V_{REF} scaling, and the IC operation mode switches to the original mode set by the MODE bit. Follow the example below to change the output reference: 1) Set GO_BIT = 1. 2) Write VSEL (00h): set the output reference 3) Read back the GO_BIT value to see if output scaling is finished. If GO_BIT = 0, voltage scaling is done. Otherwise, V_{REF} is still being adjusted 4) Set GO_BIT = 1 if output voltage scaling is needed a second time 5) Write to VSEL (00h): set the output reference
5:3	R/W	SLEW_RATE	100	Sets the slew rate when the voltage changes due to I^2C control. The output voltage changes linearly from the previous voltage to the new set voltage with this slew rate to reduce the inrush current, voltage overshoot, and voltage undershoot. 000: 13mV/μs 001: 10mV/μs 010: 7.5mV/μs 011: 4mV/μs 100: 2mV/μs 101: 1mV/μs 110: 0.5mV/μs 111: 0.25mV/μs
2	R/W	RETRY_OVP	1	Selects the V_{OUT} over-voltage protection (OVP) mode. 0: Latch off once output OVP and V_{IN} OVP are both triggered, then stay latched off until the power is rest on VIN or EN 1: Automatically recover when the OVP condition is removed
1	R/W	HICCUP_OCP	1	Selects the over-current protection (OCP) mode when both OCP and under-voltage protection (UVP) are triggered. 0: Latch-off mode 1: Hiccup mode
0	R/W	MODE	0	Selects the operation mode. 0: FCCM 1: Automatic PFM/PWM mode

SYSCNTLREG2 (02h)

The SYSCNTLREG2 command is the second system control register.

Bits	Access	Bit Name	Default	Description
7:6	R/W	PG_DEGLITCH_ TIME	11	Sets the power good signal's rising and falling edge delay time. When V_{FB} or V_{OUT} is out of regulation window, the PG comparator is triggered. The delay time is needed before the PG signal can turn high or low. 00: <1μs 01: 6μs 10: 12μs 11: 30μs

5:4	R/W	SWITCHING_ FREQUENCY	00	Sets the switching frequency (f_{SW}). There is no dedicated frequency oscillator inside the part. f_{SW} is fairly constant due to t_{ON} timer control. 00: 500kHz 01: 750kHz 10: 1MHz 11: 1.25MHz
3	R/W	SOFT_STOP	0	Sets the V_{OUT} discharge behavior after EN shutdown. 0: V_{OUT} is not controlled after EN shutdown 1: V_{OUT} discharges linearly to zero with the set soft-stop time
2:0	R/W	CURRENT_LIMIT	100	Sets the valley current limit. 000: 9.6A 001: 8.4A 010: 7.2A 011: 6A 100: 5.1A 101: 4.2A 110: 3.6A 111: 3A

OUTPUT_CURRENT (03h)

The OUTPUT_CURRENT command indicates I_{OUT}. After the part starts up, the DC output current information can be read via I^2C communication. When the inductor current is in discontinuous conduction mode (DCM), the output current sense is not very accurate. The MODE bit can be set to 0 (forced PWM mode) for excellent current-sensing accuracy at light loads. When the inductor current enters CCM, the output current sense accuracy is excellent.

Bits	Access	Bit Name	Default	Description
7:0	R	OUTPUT_CURRENT	0x00	Monitors I_{OUT}. Table 4 shows the I_{OUT} monitor chart.

Table 4 shows the output current chart from 0A to 5.1A.

Table 4: Output Current Chart

Bits[7:0]	I_{OUT} (A)	Bits[7:0]	I_{OUT} (A)	Bits[7:0]	I_{OUT} (A)
0000 0000	0	0010 0011	1.75	0100 0110	3.5
0000 0001	0.05	0010 0100	1.8	0100 0111	3.55
0000 0010	0.1	0010 0101	1.85	0100 1000	3.6
0000 0011	0.15	0010 0110	1.9	0100 1001	3.65
0000 0100	0.2	0010 0111	1.95	0100 1010	3.7
0000 0101	0.25	0010 1000	2	0100 1011	3.75
0000 0110	0.3	0010 1001	2.05	0100 1100	3.8
0000 0111	0.35	0010 1010	2.1	0100 1101	3.85
0000 1000	0.4	0010 1011	2.15	0100 1110	3.9
0000 1001	0.45	0010 1100	2.2	0100 1111	3.95
0000 1010	0.5	0010 1101	2.25	0101 0000	4
0000 1011	0.55	0010 1110	2.3	0101 0001	4.05
0000 1100	0.6	0010 1111	2.35	0101 0010	4.1
0000 1101	0.65	0011 0000	2.4	0101 0011	4.15
0000 1110	0.7	0011 0001	2.45	0101 0100	4.2
0000 1111	0.75	0011 0010	2.5	0101 0101	4.25
0001 0000	0.8	0011 0011	2.55	0101 0110	4.3
0001 0001	0.85	0011 0100	2.6	0101 0111	4.35

0001 0010	0.9	0011 0101	2.65	0101 1000	4.4
0001 0011	0.95	0011 0110	2.7	0101 1001	4.45
0001 0100	1	0011 0111	2.75	0101 1010	4.5
0001 0101	1.05	0011 1000	2.8	0101 1011	4.55
0001 0110	1.1	0011 1001	2.85	0101 1100	4.6
0001 0111	1.15	0011 1010	2.9	0101 1101	4.65
0001 1000	1.2	0011 1011	2.95	0101 1110	4.7
0001 1001	1.25	0011 1100	3	0101 1111	4.75
0001 1010	1.3	0011 1101	3.05	0110 0000	4.8
0001 1011	1.35	0011 1110	3.1	0110 0001	4.85
0001 1100	1.4	0011 1111	3.15	0110 0010	4.9
0001 1101	1.45	0100 0000	3.2	0110 0011	4.95
0001 1110	1.5	0100 0001	3.25	0110 0100	5
0001 1111	1.55	0100 0010	3.3	0110 0101	5.05
0010 0000	1.6	0100 0011	3.35	0110 0110	5.1
0010 0001	1.65	0100 0100	3.4	-	-
0010 0010	1.7	0100 0101	3.45	-	-

OUTPUT VOLTAGE (04h)

The OUTPUT_VOLTAGE command indicates V_{OUT}. After the part starts up, V_{OUT} can be read via I^2C communication. Under light loads, if the MODE bit is set to 1, the MP8853 works in PFM mode. At extremely light-load or no-load conditions, the analog-to-digital converter (ADC) only works when the first pulse comes, and then the MP8853 refreshes the output voltage register before entering sleep mode. At this moment, the sensed V_{OUT} is at its maximum value, and it is not the average V_{OUT}. Therefore, the I^2C's read-back voltage is slightly higher than the set point. When applying a load to the part, a higher voltage-sense accuracy can be achieved. The MODE bit can be set to 0 (forced PWM mode) for excellent voltage-sensing accuracy at light loads.

Bits	Access	Bit Name	Default	Description
7:0	R	OUTPUT_VOLTAGE	0x00	Monitors V_{OUT}. Table 5 shows the V_{OUT} monitor chart.

Table 5 shows the output voltage chart from 0.5V to 5.643V.

Table 5: Output Voltage Chart

Bits[7:0]	V_{OUT} (V)	Bits[7:0]	V_{OUT} (V)	Bits[7:0]	V_{OUT} (V)	Bits[7:0]	V_{OUT} (V)	Bits[7:0]	V_{OUT} (V)	Bits[7:0]	V_{OUT} (V)
0000 0000	0.500	0010 1011	1.367	0101 0110	2.235	1000 0001	3.102	1010 1100	3.969	1101 0111	4.837
0000 0001	0.520	0010 1100	1.387	0101 0111	2.255	1000 0010	3.122	1010 1101	3.989	1101 1000	4.857
0000 0010	0.540	0010 1101	1.408	0101 1000	2.275	1000 0011	3.142	1010 1110	4.010	1101 1001	4.877
0000 0011	0.561	0010 1110	1.428	0101 1001	2.295	1000 0100	3.162	1010 1111	4.030	1101 1010	4.897
0000 0100	0.581	0010 1111	1.448	0101 1010	2.315	1000 0101	3.183	1011 0000	4.050	1101 1011	4.917
0000 0101	0.601	0011 0000	1.468	0101 1011	2.335	1000 0110	3.203	1011 0001	4.070	1101 1100	4.937
0000 0110	0.621	0011 0001	1.488	0101 1100	2.356	1000 0111	3.223	1011 0010	4.090	1101 1101	4.958
0000 0111	0.641	0011 0010	1.509	0101 1101	2.376	1000 1000	3.243	1011 0011	4.110	1101 1110	4.978
0000 1000	0.661	0011 0011	1.529	0101 1110	2.396	1000 1001	3.263	1011 0100	4.131	1101 1111	4.998
0000 1001	0.682	0011 0100	1.549	0101 1111	2.416	1000 1010	3.283	1011 0101	4.151	1110 0000	5.018
0000 1010	0.702	0011 0101	1.569	0110 0000	2.436	1000 1011	3.304	1011 0110	4.171	1110 0001	5.038
0000 1011	0.722	0011 0110	1.589	0110 0001	2.456	1000 1100	3.324	1011 0111	4.191	1110 0010	5.058
0000 1100	0.742	0011 0111	1.609	0110 0010	2.477	1000 1101	3.344	1011 1000	4.211	1110 0011	5.079
0000 1101	0.762	0011 1000	1.630	0110 0011	2.497	1000 1110	3.364	1011 1001	4.231	1110 0100	5.099
0000 1110	0.782	0011 1001	1.650	0110 0100	2.517	1000 1111	3.384	1011 1010	4.252	1110 0101	5.119
0000 1111	0.803	0011 1010	1.670	0110 0101	2.537	1001 0000	3.404	1011 1011	4.272	1110 0110	5.139
0001 0000	0.823	0011 1011	1.690	0110 0110	2.557	1001 0001	3.425	1011 1100	4.292	1110 0111	5.159
0001 0001	0.843	0011 1100	1.710	0110 0111	2.578	1001 0010	3.445	1011 1101	4.312	1110 1000	5.179
0001 0010	0.863	0011 1101	1.730	0110 1000	2.598	1001 0011	3.465	1011 1110	4.332	1110 1001	5.200
0001 0011	0.883	0011 1110	1.751	0110 1001	2.618	1001 0100	3.485	1011 1111	4.352	1110 1010	5.220
0001 0100	0.903	0011 1111	1.771	0110 1010	2.638	1001 0101	3.505	1100 0000	4.373	1110 1011	5.240
0001 0101	0.924	0100 0000	1.791	0110 1011	2.658	1001 0110	3.526	1100 0001	4.393	1110 1100	5.260

0001 0110	0.944	0100 0001	1.811	0110 1100	2.678	1001 0111	3.546	1100 0010	4.413	1110 1101	5.280
0001 0111	0.964	0100 0010	1.831	0110 1101	2.699	1001 1000	3.566	1100 0011	4.433	1110 1110	5.300
0001 1000	0.984	0100 0011	1.851	0110 1110	2.719	1001 1001	3.586	1100 0100	4.453	1110 1111	5.321
0001 1001	1.004	0100 0100	1.872	0110 1111	2.739	1001 1010	3.606	1100 0101	4.473	1111 0000	5.341
0001 1010	1.024	0100 0101	1.892	0111 0000	2.759	1001 1011	3.626	1100 0110	4.494	1111 0001	5.361
0001 1011	1.045	0100 0110	1.912	0111 0001	2.779	1001 1100	3.647	1100 0111	4.514	1111 0010	5.381
0001 1100	1.065	0100 0111	1.932	0111 0010	2.799	1001 1101	3.667	1100 1000	4.534	1111 0011	5.401
0001 1101	1.085	0100 1000	1.952	0111 0011	2.820	1001 1110	3.687	1100 1001	4.554	1111 0100	5.421
0001 1110	1.105	0100 1001	1.972	0111 0100	2.840	1001 1111	3.707	1100 1010	4.574	1111 0101	5.442
0001 1111	1.125	0100 1010	1.993	0111 0101	2.860	1010 0000	3.727	1100 1011	4.595	1111 0110	5.462
0010 0000	1.145	0100 1011	2.013	0111 0110	2.880	1010 0001	3.747	1100 1100	4.615	1111 0111	5.482
0010 0001	1.166	0100 1100	2.033	0111 0111	2.900	1010 0010	3.768	1100 1101	4.635	1111 1000	5.502
0010 0010	1.186	0100 1101	2.053	0111 1000	2.920	1010 0011	3.788	1100 1110	4.655	1111 1001	5.522
0010 0011	1.206	0100 1110	2.073	0111 1001	2.941	1010 0100	3.808	1100 1111	4.675	1111 1010	5.543
0010 0100	1.226	0100 1111	2.093	0111 1010	2.961	1010 0101	3.828	1101 0000	4.695	1111 1011	5.563
0010 0101	1.246	0101 0000	2.114	0111 1011	2.981	1010 0110	3.848	1101 0001	4.716	1111 1100	5.583
0010 0110	1.266	0101 0001	2.134	0111 1100	3.001	1010 0111	3.868	1101 0010	4.736	1111 1101	5.603
0010 0111	1.287	0101 0010	2.154	0111 1101	3.021	1010 1000	3.889	1101 0011	4.756	1111 1110	5.623
0010 1000	1.307	0101 0011	2.174	0111 1110	3.041	1010 1001	3.909	1101 0100	4.776	1111 1111	5.643
0010 1001	1.327	0101 0100	2.194	0111 1111	3.062	1010 1010	3.929	1101 0101	4.796	-	-
0010 1010	1.347	0101 0101	2.214	1000 0000	3.082	1010 1011	3.949	1101 0110	4.816	-	-

ID1 (05h)

The ID1 command returns information about the IC and vendor ID.

Bits	Access	Bit Name	Default	Description
7:4	R	VENDOR_ID	1000	Returns the vendor ID.
3:0	R	IC_REVISION_ID	0111	Returns the IC version.

STATUS (06h)

The STATUS command indicates certain fault conditions.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	0000	Reserved.
3	R	OC	0	Indicates whether an output over-current (OC) condition has occurred. When this bit is high, the IC is in hiccup mode or has latched off.
2	R	OTEW	0	Indicates the die temperature's early warning. When the bit is high, the die temperature exceeds 120°C.
1	R	OT	0	Indicates when over-temperature (OT) shutdown has occurred. When this bit is high, the IC is in thermal shutdown.
0	R	PG	1	Indicates whether the output is power good. PG compares V_{FB}/V_{OUT} with V_{REF}. 0: The V_{OUT} power is not normal 1: The V_{OUT} power is normal. V_{OUT} exceeds 90% of the designed regulation voltage and is below 105% of the regulation voltage

APPLICATION INFORMATION

Setting the Output Voltage in a FB Control Loop

The MP8853 can be controlled by the FB loop. V_{OUT} can be set by the external resistor dividers. The FB loop reference voltage is the default value (0.72V), but it can be configured via the I^2C.

Figure 13 shows the FB loop network.

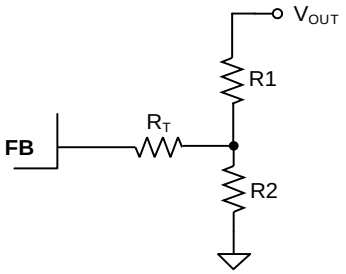


Figure 13: FB Loop Network

Choose R1 and R2 with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.72V} - 1} \quad (3)$$

Table 6 lists the recommended feedback resistor values for common output voltages.

Table 6: Resistor Selection for Common Output Voltages (8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (µH)
1.0	80.6	205	10	2.2
1.2	80.6	121	10	2.2
1.5	80.6	74.4	10	2.2
1.8	80.6	53.6	10	2.2
2.5	80.6	32.4	10	2.2
3.3	80.6	22.6	10	4.7
5	80.6	13.7	10	4.7

Note:

8) The recommended parameters are based on a 12V input voltage and 22µF x 4 output capacitance. Different input voltage and output capacitor values may affect the selection of R1 and R2. For other components' parameters, see the Typical Application Circuits section starting on page 36.

Output Voltage (V_{OUT}) Dynamic Scale

The output voltage's dynamic scale can be accomplished via the I^2C. To set the dynamic scale, refer to Figure 14 and follow the steps below:

1) Write GO_BIT (SYSCNTLREG1 (01h), bit[6]) to 1.
2) Write OUTPUT_REFERENCE_VOLTAGE (VSEL (00h), bits[6:0]) to set the reference voltage by simultaneously.
3) When the command is finished, GO_BIT automatically resets to 0 to prevent false operation for V_{OUT} scaling.

Repeat the steps above if the output voltage must be changed to a different voltage.

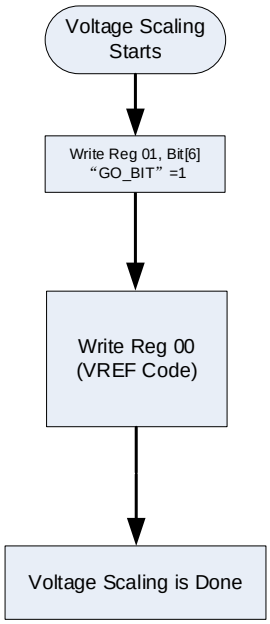


Figure 14: Output Voltage Dynamic Scale Flow Chart

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL Series**

Use a 0.47µH to 5µH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance below 5mΩ. For most designs, the inductance can be calculated with Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current.

The maximum inductor peak current can be estimated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Use a higher inductance for improved efficiency under light-load conditions below 100mA.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 7 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 7: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL	2.2µH to 4.7µH	MPS
MPL-AL-6050-2R2	2.2µH	MPS
MPL-AL-6050-4R7	4.7µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down current has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22µF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (9)$$

Where L_1 is the inductance, and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8853 can be optimized for a wide range of capacitance and ESR values.

Selecting the Bootstrap Capacitor and Resistor

The bootstrap capacitor powers the floating power MOSFET driver. It is recommended to use a 0.1μF ceramic capacitor.

The value of bootstrap resistor is generally recommended to be between 0Ω and 10Ω. The BST resistor determines the HS-FET's turn-on speed. For designs where the VCC decoupling capacitor layout cannot be optimized to follow the recommended layout, it is recommended to place the 10Ω BST resistor in series with the BST capacitor.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- V_{OUT} is 5V or 3.3V
- The duty cycle is high (D > 50%)

In these cases, add an external BST diode from VCC to BST (see Figure 15).

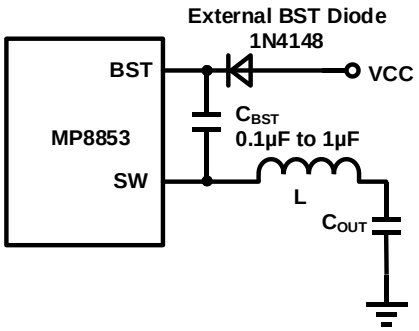


Figure 15: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is between 0.1μF and1μF.

Connect VCC to VIN at a Low Input Voltages

VCC can be connected directly to VIN when V_{IN} is below 3.5V. This improves the MP8853's efficiency at low input voltages. To use this application set-up, the V_{IN} spike must be limited below 4V; otherwise, VCC may be damaged.

Design Example

Table 8 shows a design example following the application guidelines for the specifications below.

Table 8: Design Example

V_{IN}	2.85V to 18V
V_{OUT}	1V
I_{OUT}	4A

The detailed application schematics are shown in the Typical Application Circuits section starting on page 36. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section starting on page 11. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 16 and follow the guidelines below. A 4-layer layout is strongly recommended to achieve better thermal performance.

1. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large copper planes.
3. Use two layers for the VIN and PGND trace to improve thermal performance.
4. Add several vias close to the PGND pads to help with thermal dissipation.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and PGND as possible.
7. Place the external feedback resistors next to FB.
8. Ensure that there is no via on the FB trace.
9. Keep the switching node (SW) short and route it away from the feedback network.
10. Keep the BST voltage path (BST, R3, C3, and SW) as short as possible.
11. Connect AGND together at the VCC capacitor
12. Kelvin connect AGND and PGND at the PGND pin.

Note:

9) The recommended layout is based on the Typical Application Circuits section starting on page 36.

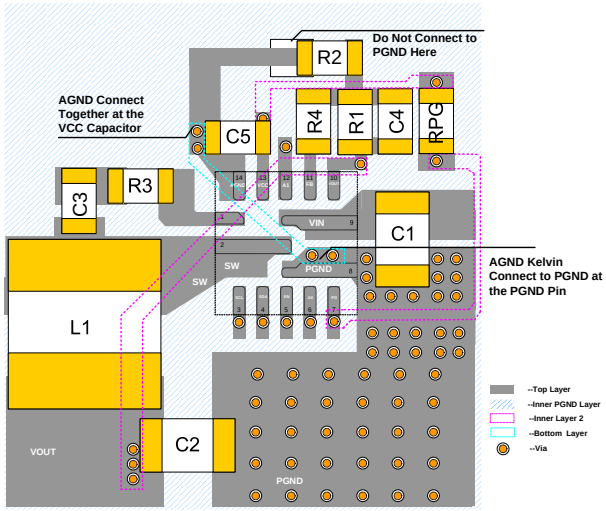


Figure 16: Recommend Layout

TYPICAL APPLICATION CIRCUITS (10)

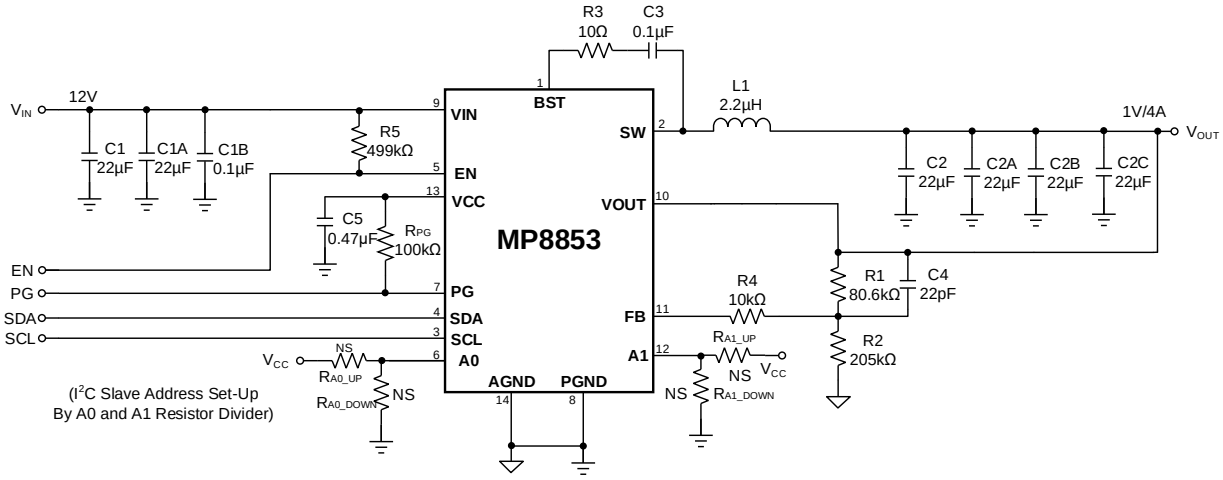


Figure 17: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 4A)

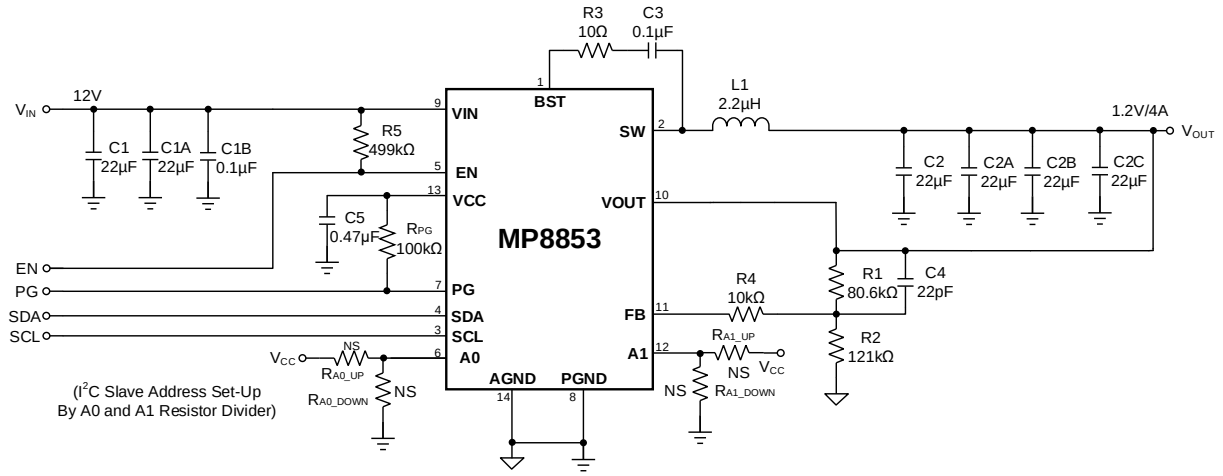


Figure 18: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 4A)

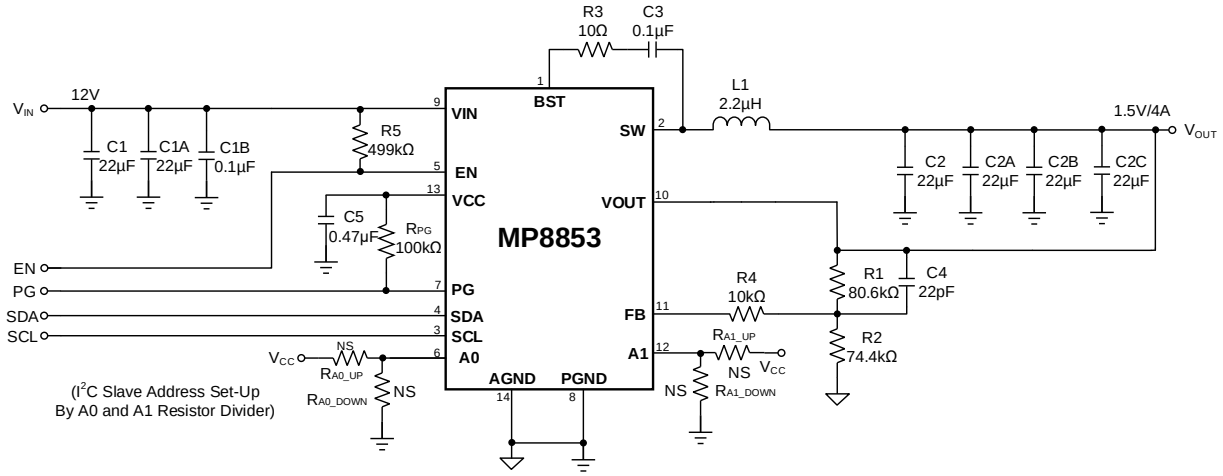


Figure 19: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 4A)

TYPICAL APPLICATION CIRCUITS *(continued)*

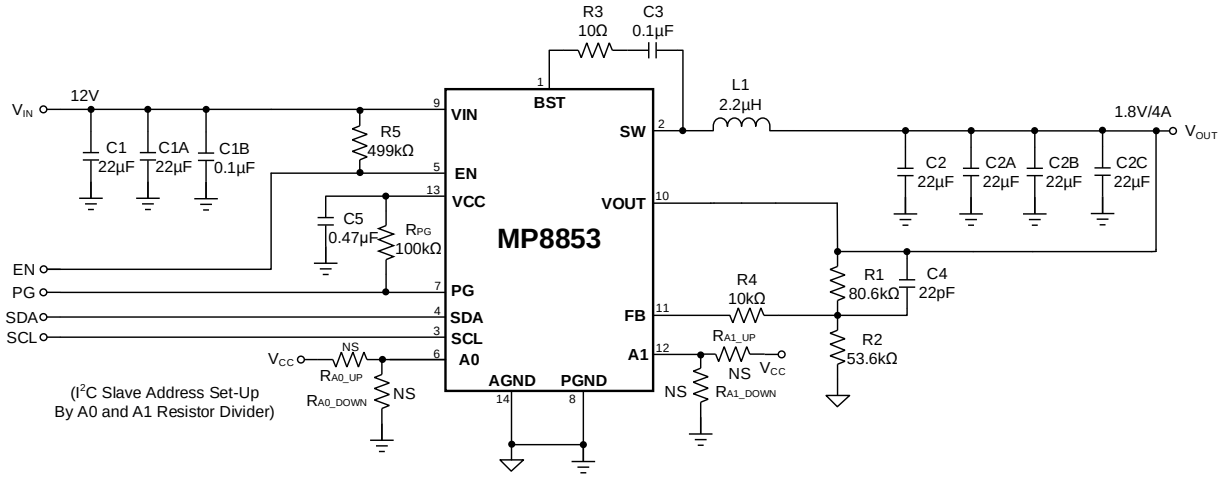


Figure 20: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 4A)

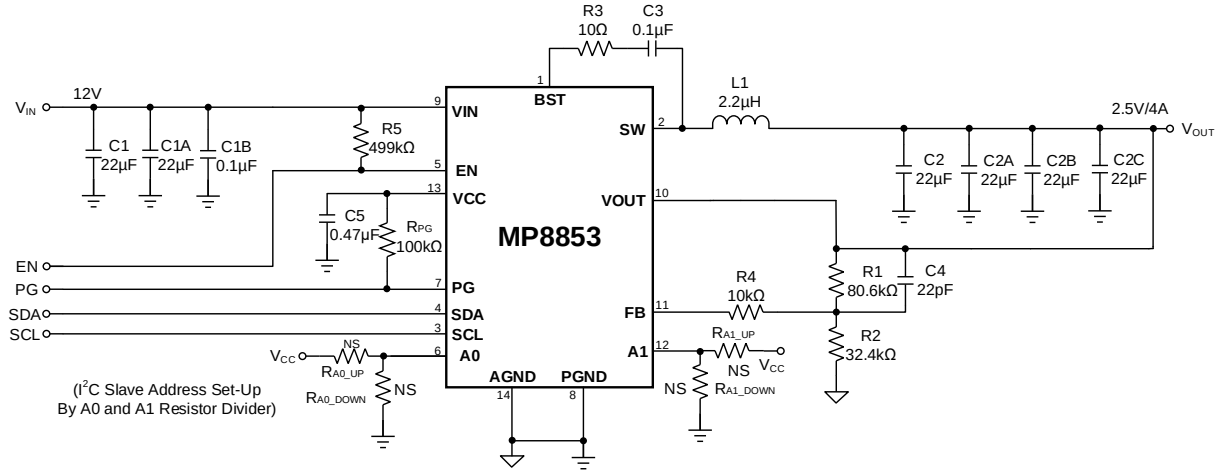


Figure 21: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 4A)

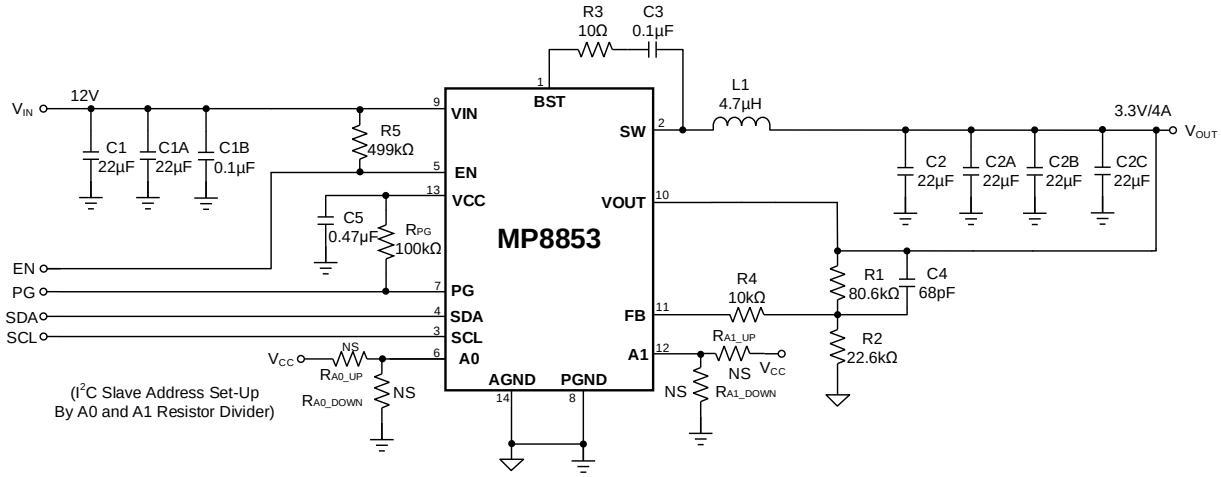


Figure 22: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 4A)

TYPICAL APPLICATION CIRCUITS *(continued)*

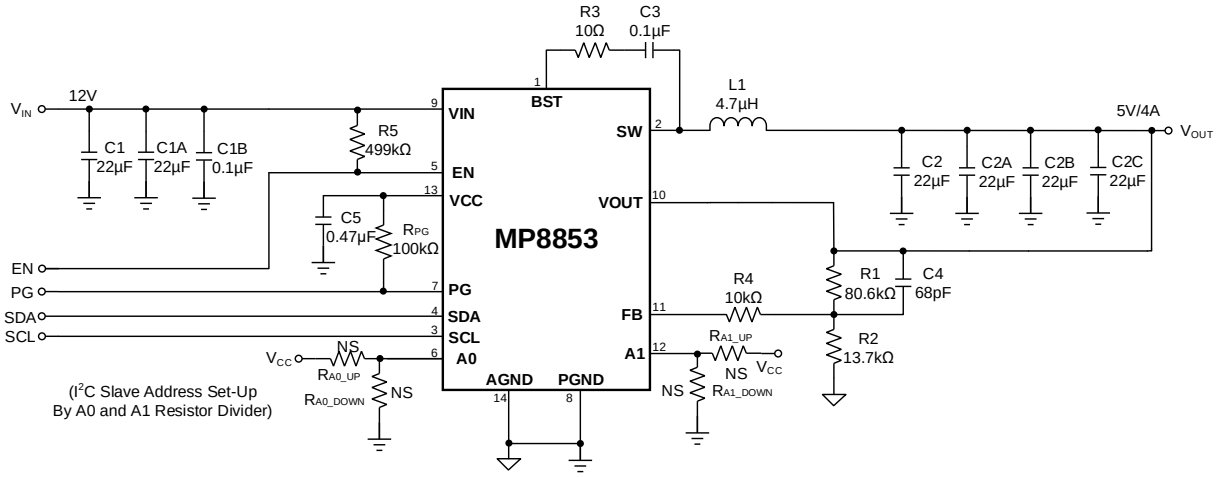
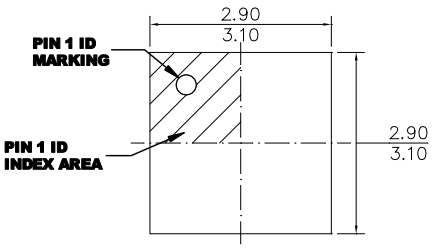


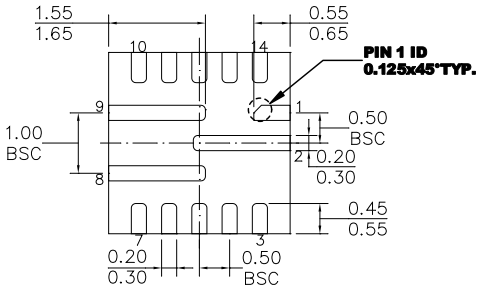
Figure 23: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4A)

PACKAGE INFORMATION

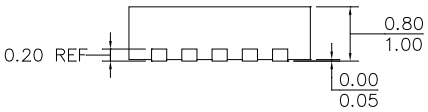
QFN-14 (3mmx3mm)



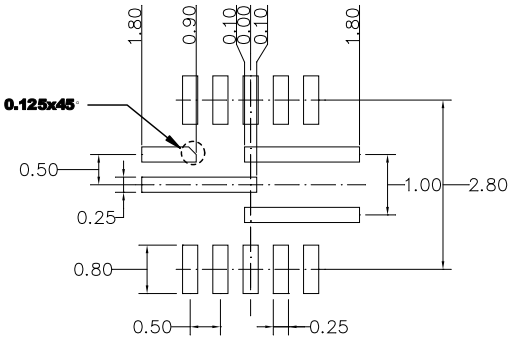
TOP VIEW



BOTTOM VIEW



SIDE VIEW

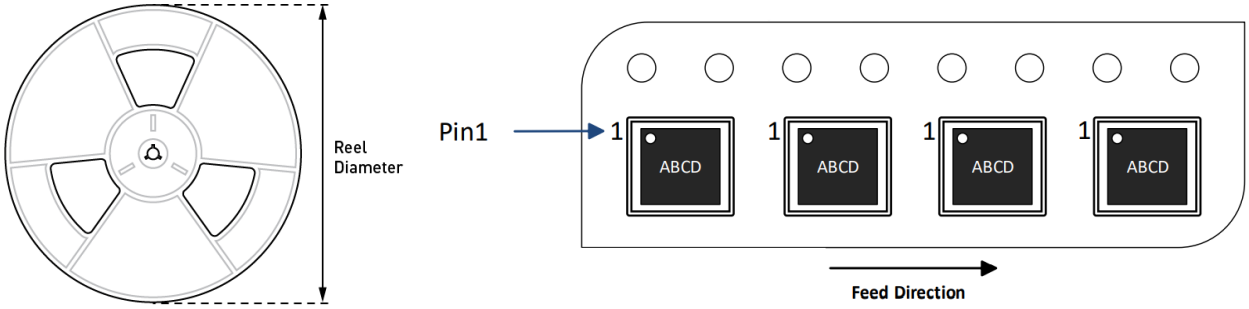


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8853GQ-Z	QFN-14 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/13/2024	Initial Release	-

