



## Description

The HNVATS4A104PZT4G uses advanced trench technology

to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

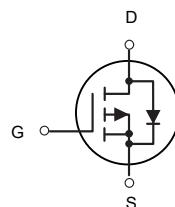


TO-252-2L

## General Features

$V_{DS} = -30V$   $I_D = -70A$

$R_{DS(ON)} < 10m\Omega$  @  $V_{GS} = -10V$



P-Channel MOSFET

## Application

Battery protection

Load switch

Uninterruptible power supply

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
HNVATS4A104PZT4G	TO-252-2L	HXY MOSFET	2500

## Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_c = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^{1.6}$	-70	A
$I_D @ T_c = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^{1.6}$	-50	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-200	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	80	mJ
$I_{AS}$	Avalanche Current	-40	A
$P_D @ T_c = 25^\circ C$	Total Power Dissipation <sup>4</sup>	90	W
$T_{STG}$	Storage Temperature Range	-55 to 175	°C
$T_J$	Operating Junction Temperature Range	-55 to 175	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup> ( $t \leq 10S$ )	20	°C/W
	Thermal Resistance Junction-ambient <sup>1</sup> (Steady State)	50	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-case <sup>1</sup>	1.6	°C/W



**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	---	---	V
R <sub>DSON</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	---	7	10	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-15A	---	11	18	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.2	---	-2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	-5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
R <sub>G</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	1.2	---	Ω
Q <sub>g</sub>	Total Gate Charge (-10V)	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-18A	---	60	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	9	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	15	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-20A	---	17	---	ns
T <sub>r</sub>	Rise Time		---	40	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	55	---	
T <sub>f</sub>	Fall Time		---	13	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-25V, V <sub>GS</sub> =0V, f=1MHz	---	3450	---	pF
C <sub>oss</sub>	Output Capacitance		---	255	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	140	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-70	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =-20A, di/dt=100A/μs, T <sub>J</sub> =25°C	---	22	---	nS
			---	72	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-50V,V<sub>GS</sub>=-10V,L=0.1mH,I<sub>AS</sub>=-40A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation
- 6.The maximum current rating is package limited.



### Typical Characteristics

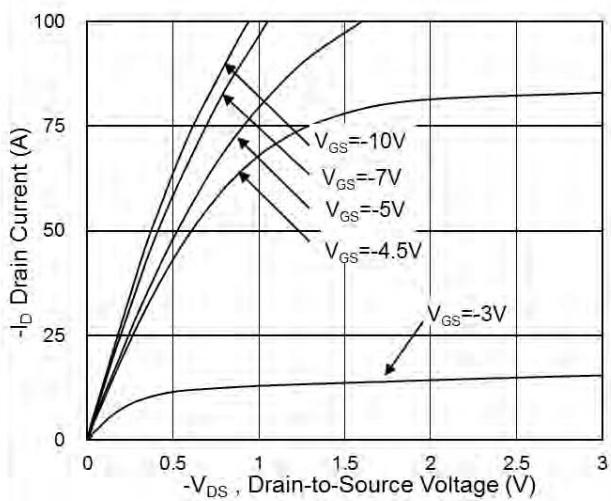


Fig.1 Typical Output Characteristics

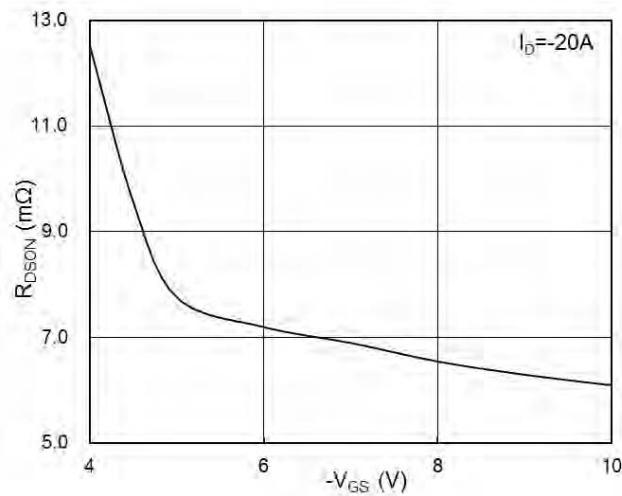


Fig.2 On-Resistance vs. Gate-Source Voltage

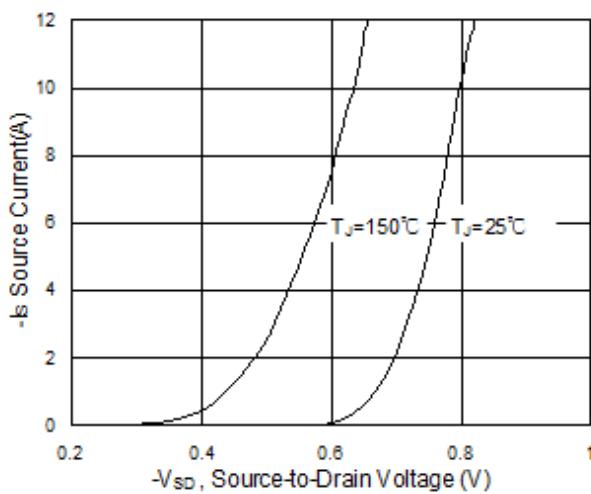


Fig.3 Forward Characteristics of Reverse

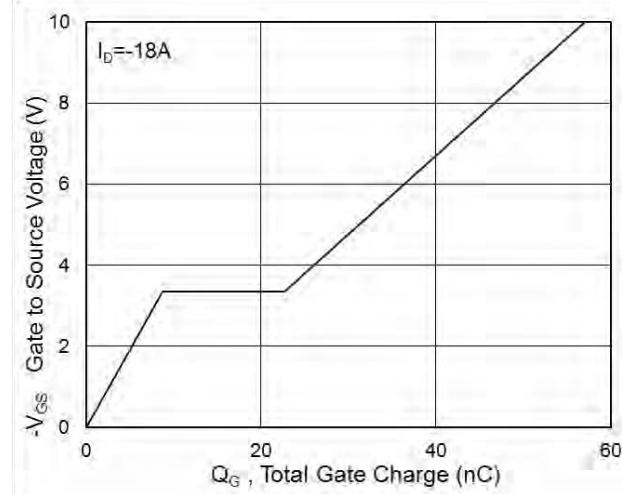


Fig.4 Gate-Charge Characteristics

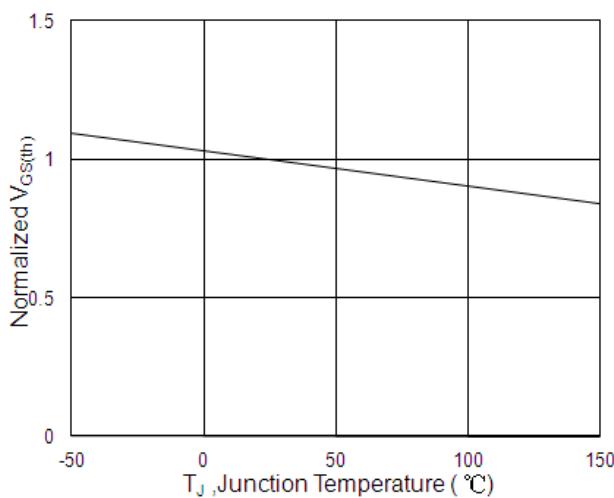


Fig.5 Normalized  $-V_{GS(th)}$  vs.  $T_J$

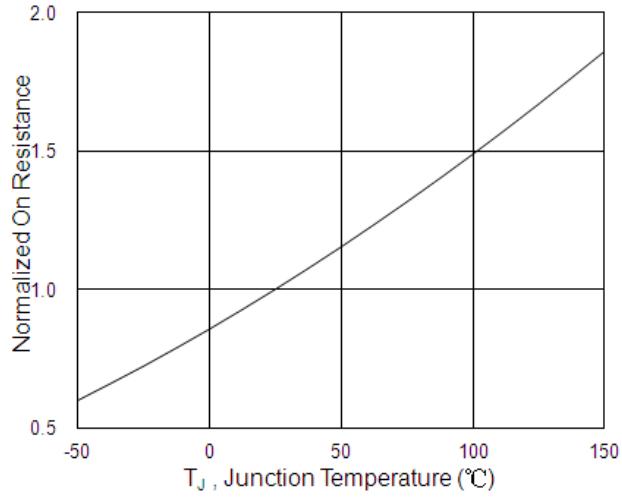


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

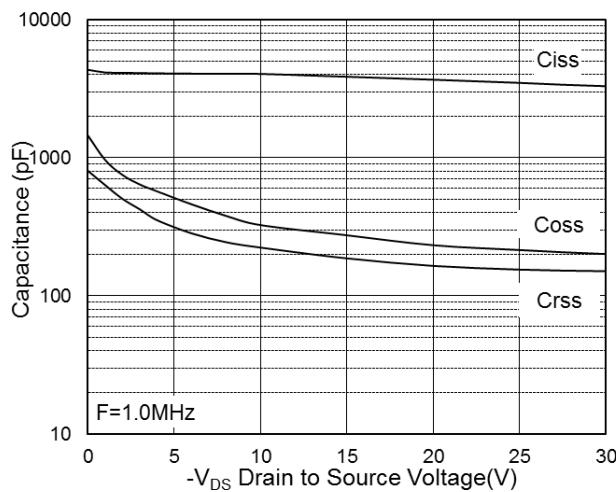


Fig.7 Capacitance

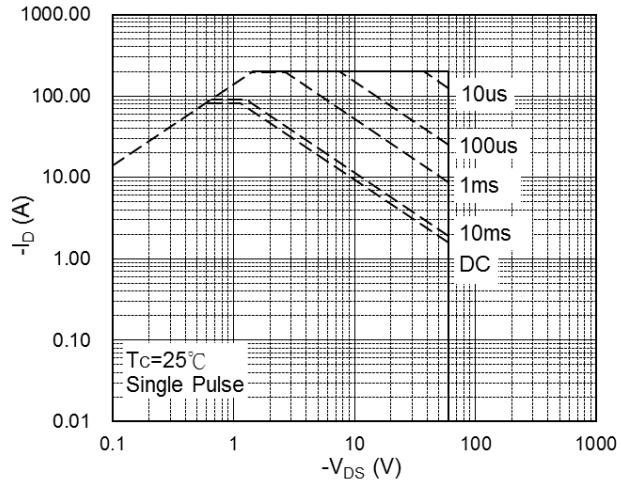


Fig.8 Safe Operating Area

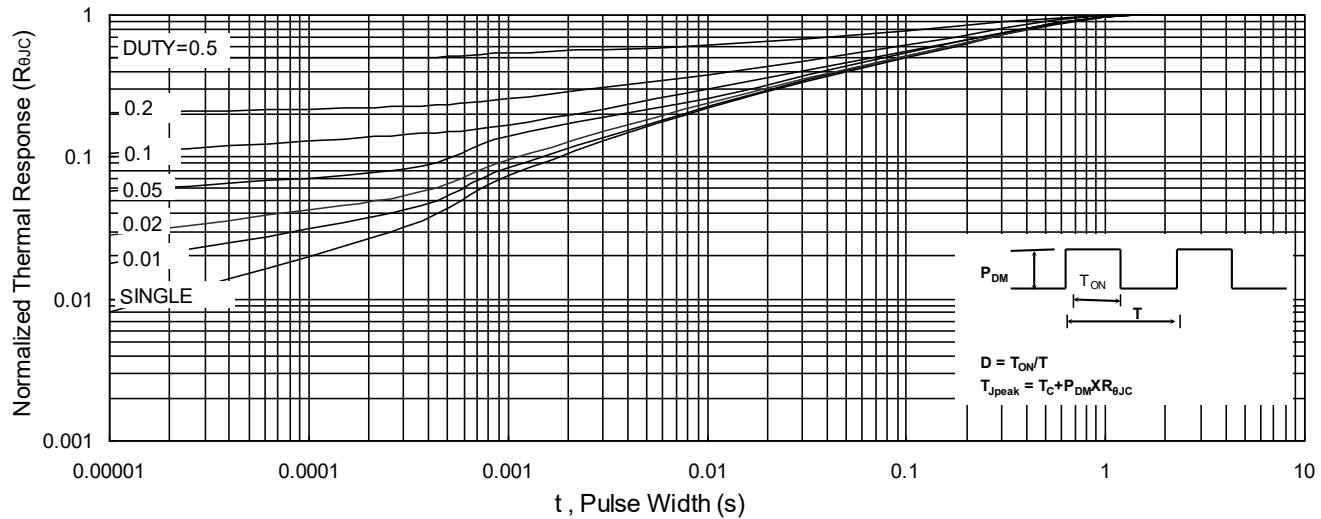


Fig.9 Normalized Maximum Transient Thermal Impedance

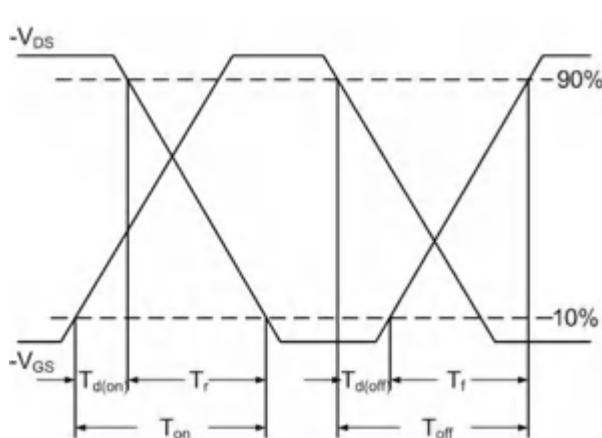


Fig.10 Switching Time Waveform

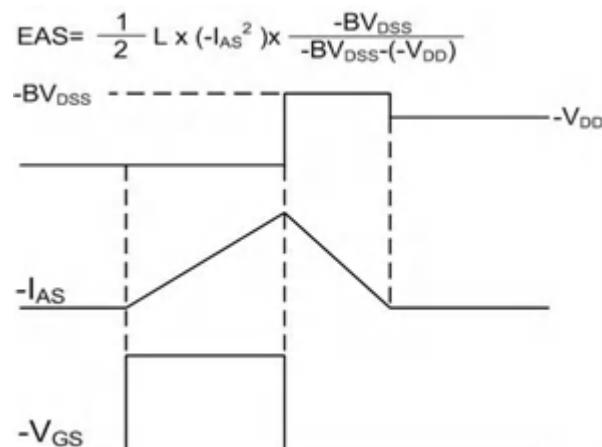
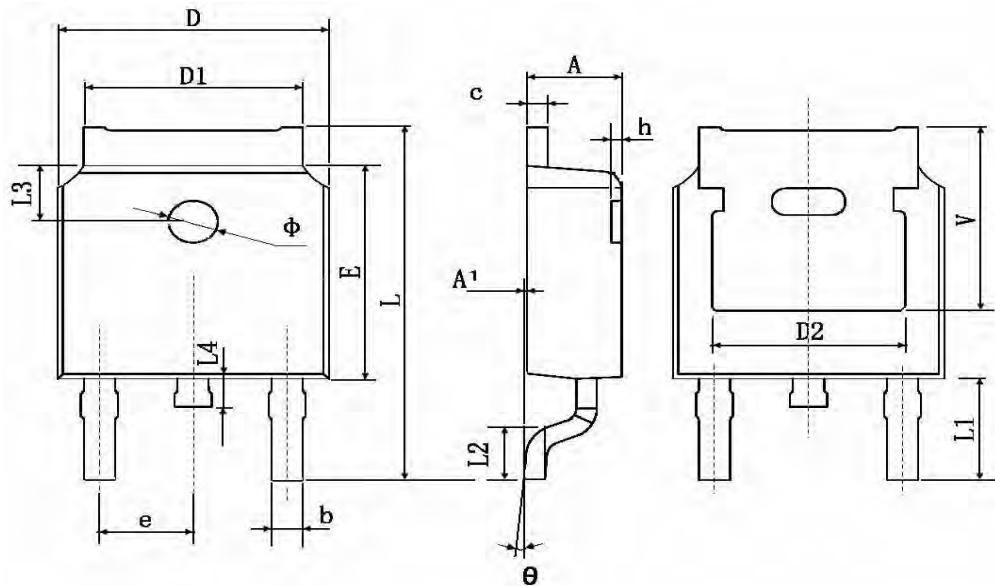


Fig.11 Unclamped Inductive Switching Waveform



## TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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