



UNI-SEMICONDUCTOR CO., LTD

宇力半导体有限公司



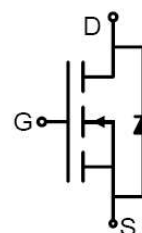
APG250N01 Data Sheet

V 1.1

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Feature

- 100V,40A
 $R_{DS(ON)} < 25m\Omega @ V_{GS}=10V$ (TYP:18m Ω)
 $R_{DS(ON)} < 38m\Omega @ V_{GS}=4.5V$ (TYP:25m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G250N01	APG250N01	TO-220	-	-	1000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a=25^{\circ}\text{C}$)	I_D	40	A
Continuous Drain Current ($T_a=100^{\circ}\text{C}$)	I_D	25	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	160	A
Single Pulsed Avalanche Energy ⁽²⁾	E_{AS}	16	mJ
Power Dissipation	P_D	45	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.5	$^{\circ}\text{C/W}$
Junction Temperature	T_J	150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55~ +150	$^{\circ}\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =100V, V _{GS} = 0V	-	-	1	μA
Gate-body leakage current	I _{GSS}	V _{GS} =± 20V, V _{DS} = 0V	-	-	±100	nA
Gate threshold voltage ⁽³⁾	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.8	2.8	V
Drain-source on-resistance ⁽³⁾	R _{DS(on)}	V _{GS} =10V, I _D =15A	-	18	25	mΩ
		V _{GS} =4.5V, I _D =10A	-	25	38	mΩ
Forward Threshold Voltage	g _{fs}	V _{DS} =10V, I _D =20A	-	22	-	S
Gate Resistance	R _g	V _{DS} =V _{GS} =0V, f =1MHz	-	1.62	-	Ω
Dynamic characteristics						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f =1MHz	-	822	-	pF
Output Capacitance	C _{oss}		-	310	-	
Reverse Transfer Capacitance	C _{rss}		-	23.5	-	
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} =50V, I _D =20A, V _{GS} =10V, R _G =3Ω	-	15	-	ns
Turn-on rise time	t _r		-	3.2	-	
Turn-off delay time	t _{d(off)}		-	30	-	
Turn-off fall time	t _f		-	7.6	-	
Total Gate Charge	Q _g	V _D S=50V, I _D =20A, V _G S=10V	-	22.7	-	nC
Gate-Source Charge	Q _{gs}		-	6.2	-	
Gate-Drain Charge	Q _{gd}		-	5.3	-	
Reverse Recovery Chrage	Q _{rr}	I _F =20A,di/dt=100A/us		59		nC
Reverse Recovery Time	T _{rr}	I _F =20A,di/dt=100A/us		45		ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V _{DS}	V _{GS} =0V, I _S =10A	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I _S		-	-	40	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^{\circ}\text{C}, V_{DD} = 50V, R_G = 25\Omega, L = 0.5Mh$
3. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10$ sec

Typical Performance Characteristics

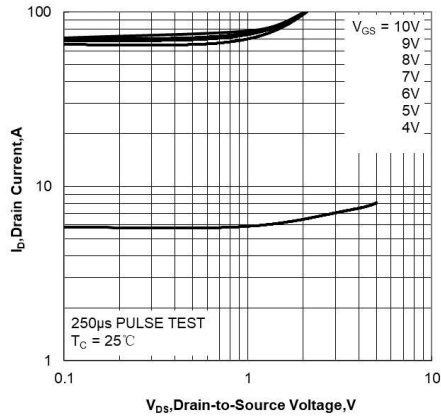


Figure 1. Output Characteristics

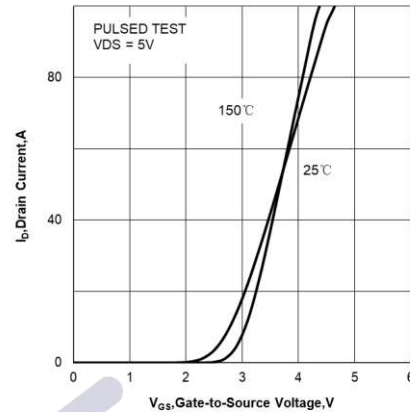


Figure 2. Transfer Characteristics

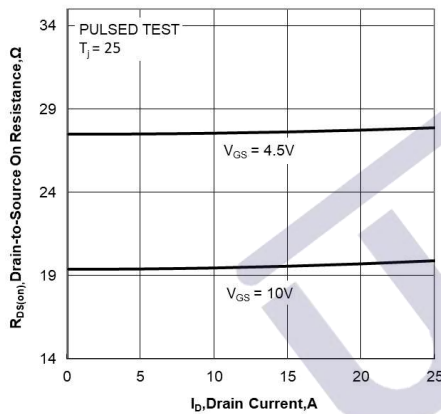
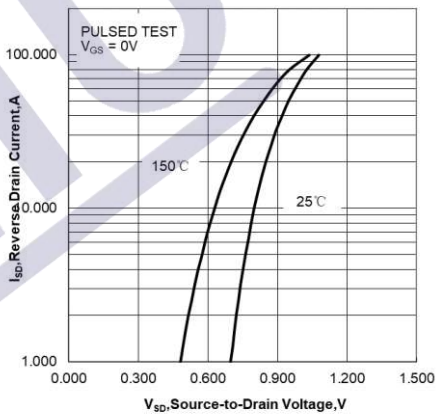
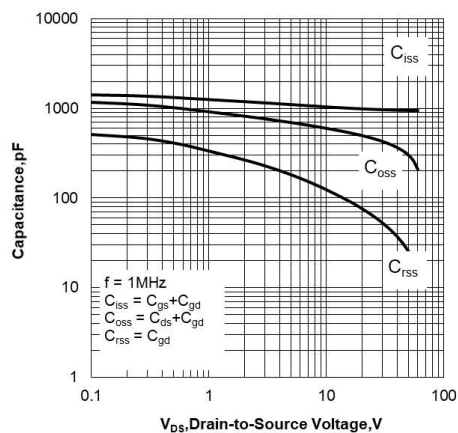
Figure 3. Drain-to-Source On Resistance
vs Drain CurrentFigure 4. Body Diode Forward Voltage
vs Source Current and Temperature

Figure 5. Capacitance Characteristics

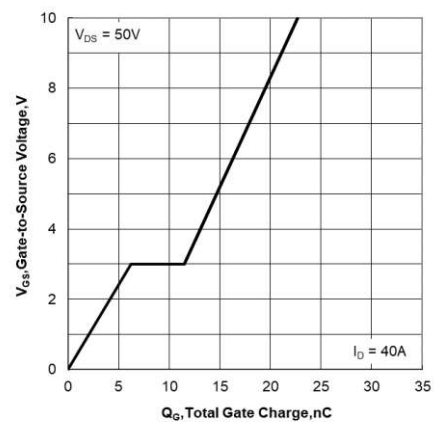


Figure 6. Gate Charge Characteristics

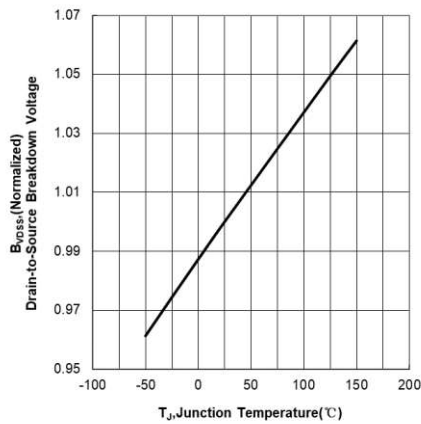


Figure 7. Normalized Breakdown Voltage
vs Junction Temperature

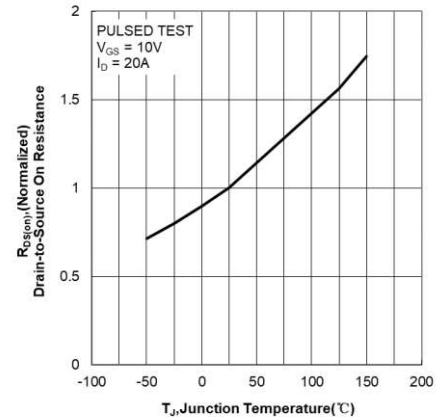


Figure 8. Normalized On Resistance vs
Junction Temperature

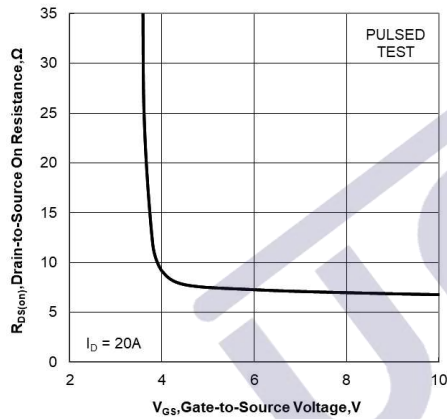


Figure 9. Drain-to-Source On Resistance vs Gate
Voltage and Drain Current

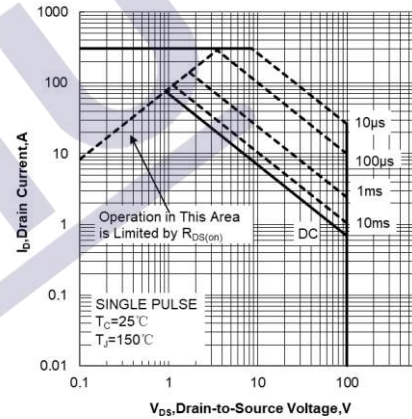


Figure 10. Maximum Safe Operating Area

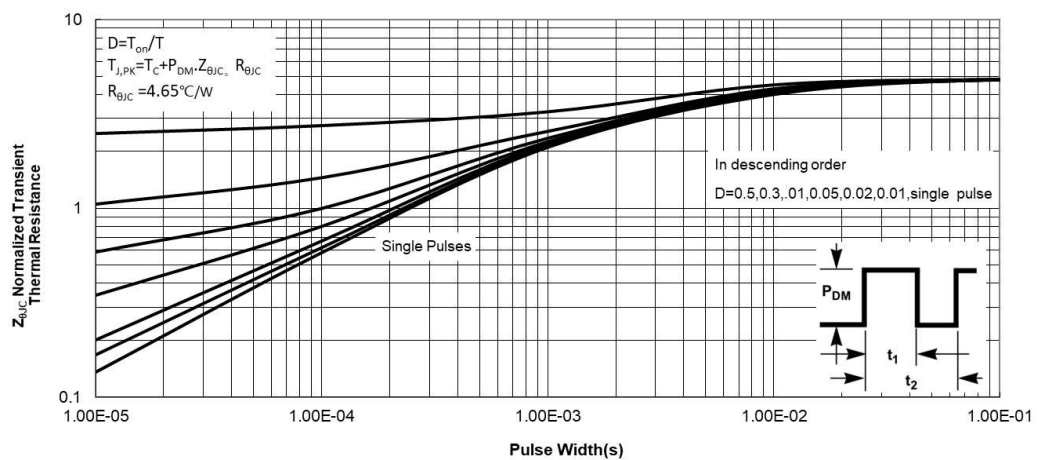
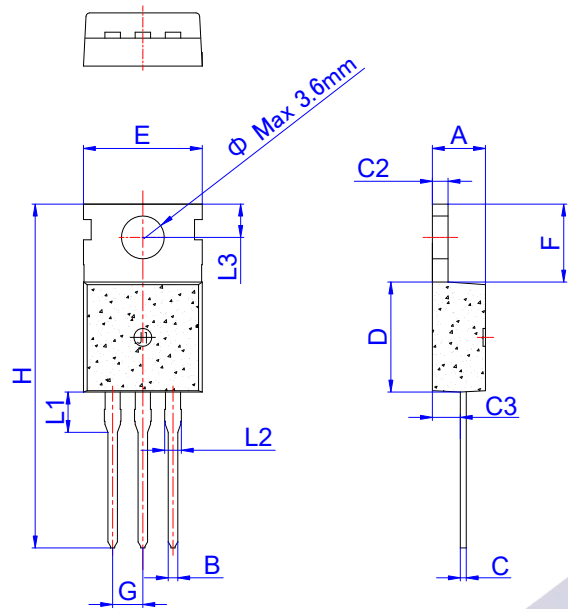


Figure11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TO-220 Package Information



TO-220

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	0.70		0.90	0.028		0.035
C	0.45		0.60	0.018		0.024
C2	1.23		1.32	0.048		0.052
C3	2.20		2.60	0.087		0.102
D	8.90		9.90	0.350		0.390
E	9.90		10.3	0.390		0.406
F	6.30		6.90	0.248		0.272
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.39			0.133	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
Φ		3.6			0.142	

1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2021/08/10	1.1	Layout adjustment

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3.联系我们

浙江宇力微新能源科技有限公司

总部地址：绍兴市越城区斗门街道袍渎路25号中节能科创园45幢4/5楼

电话：0575-85087896（研发部）

传真：0575-88125157

E-mail: htw@uni-semic.com

无锡地址:江苏省无锡市锡山区先锋中路6号中国电子(无锡)数字芯城1#综合楼503室

电 话：0510-85297939

E-mail: zh@uni-semic.com

深圳地址:深圳市宝安区西乡街道南昌社区宝源路泳辉国际商务大厦410

电 话：0755-84510976

E-mail: htw@uni-semic.com