

REALTEK

RTL8372N-CG

4-PORT 2.5G + 2-PORT 10G SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8372N IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

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- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.1	2023/04/19	First release.
0.2	2023/06/29	Modify the operating range of DVDDIO0, update the input power of simulation condition, update Mechanical Dimensions figure, add Thermal Characteristics.

Revision	Release Date	Summary
0.3	2024/01/10	Modify the description of the Power and GND Pins. Modify the pin number of the High Speed Serial Interface Pins. Modify the description of the V_{ih} and V_{il} in chapter 10.5.8. Add description to pin RSV_TEST0. Modify the description of the Table 15. LED Definitions.

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1. General Description

The Realtek RTL8372N-CG (hereafter referred to as the RTL8372N) is a low-power, high-performance and highly integrated quad-port 2.5G, combined with a two-port 10G switch controller. It has an embedded quad-port Ethernet PHY Transceiver that is compatible with 10BASE-T_e, 100Base-TX, 1000BASE-T, and 2.5GBASE-T. The RTL8372N is fully compatible with the IEEE 802.3 standard and provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5e UTP cable.

The RTL8372N uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto Correction, polarity correction, MDI swap, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, RFI protection, loopback diagnostic capability, and error correction are implemented in the RTL8372N to provide robust transmission and reception capabilities.

The RTL8372N supports two SERDES interfaces. SERDES 0 and SERDES 1 support USXGMII/10G-R/HSGMII/2500BASE-X/1000BASE-X/SGMII/100BASE-FX mode to connect a PHY Transceiver, Fiber OE module or external CPU.

The embedded packet storage SRAM in the RTL8372N features superior memory management technology to efficiently utilize memory space. The RTL8372N integrates a 4096-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the Slave I2C interface/Clause 22 MDC/MDIO management Interface/SPI Interface, and each of the entries can be configured as a static entry. The entry aging time is between 0.2 and 13107 seconds. 4K Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The RTL8372N supports a 4096-entry VLAN table and 96-entry Ingress Access Control List (ACL). The ACL function supports L2/L3/L4 in IPv4/IPv6 protocols and performs configurable actions, such as Drop/Permit/Redirect/Copy//Mirror/Logging/Policing/Ingress VLAN assignment/QoS remarking/VLAN tag status assignment. The RTL8372N supports per-port ingress/egress bandwidth control and per-queue egress bandwidth control.

The RTL8372N provides three types of packet scheduling, including SP (Strict Priority), WFQ (Weighted Fair Queuing), and WRR (Weighted Round Robin). Each port has 8 physical queues and each queue provides a leaky-bucket to shape the incoming traffic into the average rate behavior. The Broadcast/Multicast/Unknown-Multicast/Unknown-Unicast storm suppression function can inhibit external and internal malicious attacks.

The RTL8372N supports 1-set of port mirror configurations to mirror ingress and egress traffic. RSPAN are also supported for traffic monitoring purposes. For network management purposes, complete MIB counters are supported to provide forwarding statistics in real time. The Link aggregation function enhances link redundancy and increases bandwidth linearly.

2. Features

- 4-port 2.5G+2-port 10G non-blocking switch architecture
- Embedded 4-port 10M/100M/1000M/2.5GBase-T PHY
- Supports two set SERDES interfaces
 - ◆ SERDES 0 and SERDES 1 supports USXGMII/10G-R/2500BASE-X/1000BASE-X/HSGMII/SGMII/100BASE-FX to connect a PHY transceiver, Fiber OE module or external CPU
- Supports Slave I2C interface/Clause 22 MDC/MDIO management Interface/SPI Interface for external CPU to access configuration register
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode on port 4~port 8)
- Supports up to 12Kbyte jumbo packet length forwarding at wire speed
- Compatible with IEEE 802.3, IEEE 802.3u, and IEEE 802.3ab
- Supports IEEE 802.3az (Energy Efficient Ethernet)
- Supports IEEE 802.3bz (2.5GBASE-T)
- Supports IEEE 802.3 optional ability (Energy Efficient Ethernet and Fast Retrain)
- Integrated 10M BASE-Te and 100M/1000M/2.5GBASE-T IEEE 802.3 compliant transceiver
- Auto-Negotiation with Extended Next Page capability (XNP)
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Configurable MDI port ordering (MDI swap) for easy PCB layout
- Supports power down/link down power saving mode
- Supports IEEE 802.3 Clause 22 MDC/MDIO management interface
- Built-in Wake-on-LAN (WOL)
- Supports Interrupt function
- Supports Baseline Wander Correction
- QoS function
 - ◆ 8 physical queues per port
 - ◆ Priority Assignment based on IEEE 802.1P priority, DSCP value, physical port number, DMAC-based, SMAC-based, Ether-Type-based, CVID, SVID, IPv4 SIP, IPv4 DIP, IPv4/IPv6 TOS field, IPv6 Flow Label, TCP/UDP source/destination port
 - ◆ Strict Priority (SP) and Weighted Fair Queue (WFQ), Weighted Round Robin (WRR) packet scheduling
 - ◆ Supports Fixed and Assured bandwidth control
 - ◆ QoS remarking for 802.1p and DSCP (includes IPv4/IPv6)
 - ◆ Supports average packet rate control leaky-bucket per queue, with 16Kbps steps from 16Kbps to 10Gbps
 - ◆ Supports ingress and egress port bandwidth control with 16Kbps steps from 16Kbps to 10Gbps

- 4096-entry MAC lookup table, supports unicast MAC, multicast MAC and IP look-up
- Supports 4096-entry VLAN table for CLAN and SVLAN
- Supports 96-entry ACL rules
- Supports 8Mbit Packet Buffer
- Supports IEEE802.1x Access Control Protocol
- Supports 16-entry multiple spanning tree
- Supports storm control for Unknown unicast/Unknown multicast/multicast/broadcast
- Supports 4-set link aggregation
- Supports IGMP snooping for IGMPv1/v2/v3 and MLDv1/v2
- MIB Functions
 - ◆ MIB-II (RFC 1213)
 - ◆ Ethernet-like MIB (RFC 3635)
 - ◆ Interface Group MIB (RFC 2863)
 - ◆ RMON (RFC 2819)
 - ◆ Bridge MIB (RFC 1493)
 - ◆ Bridge MIB Extension (RFC 2674)
- Self-Loopback diagnostic capability
- Supports Synchronous Ethernet and Precision Time Protocol (PTP)
- Supports up to 3 parallel LEDs per port to indicate port status
- Supports 25MHz crystal or external OSC
- Integrated MCU
- Supports SPI Flash Interface
- Supports EEPROM Interface
- EPAD DR-QFN 144 package

3. System Applications

3.1. 4-Port 2.5GBASE-T + 1-Port 10G-R + 1-Port 2.5/10G-WiSoC

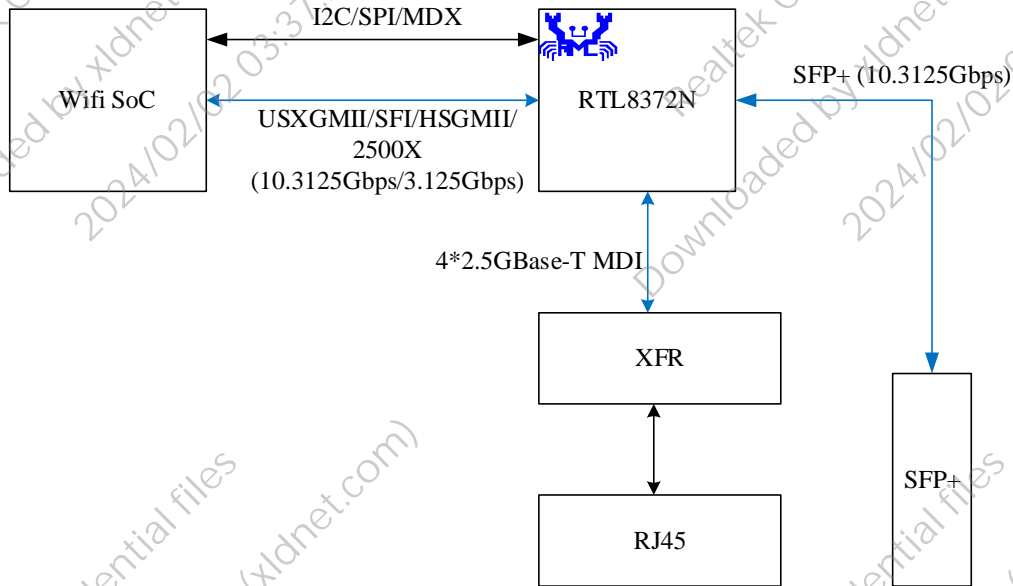


Figure 1. 4-Port 2.5GBASE-T + 1-Port 10G-R + 1-Port 2.5/10G-WiSoC

3.2. 4-Port 2.5GBASE-T+1-Port 10GBASE-T + 1-Port 2.5/10G-WiSoC

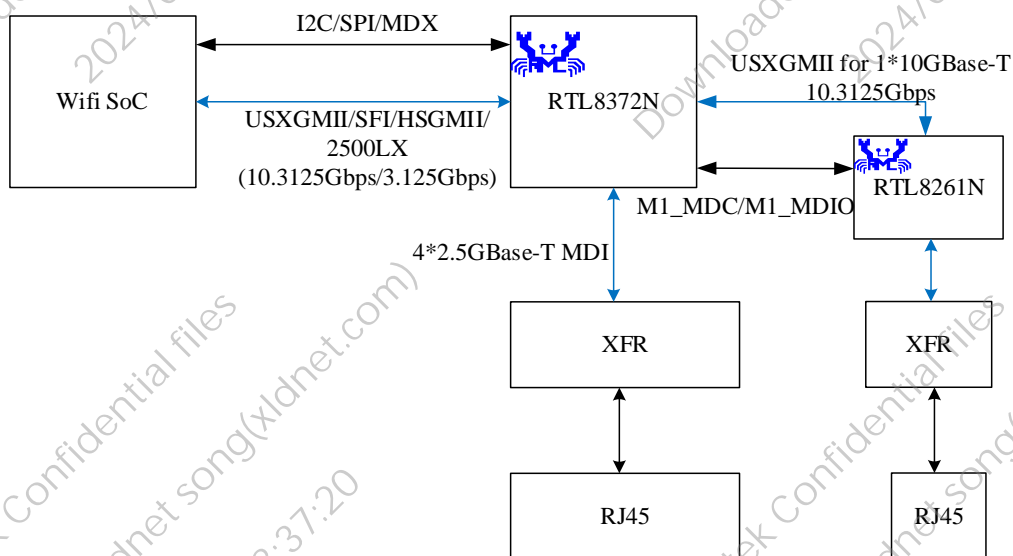


Figure 2. 4-Port 2.5GBASE-T+1-Port 10GBASE-T + 1-Port 2.5/10G-WiSoC

3.3. 4-Port 2.5GBASE-T + 2-Port 10G-R

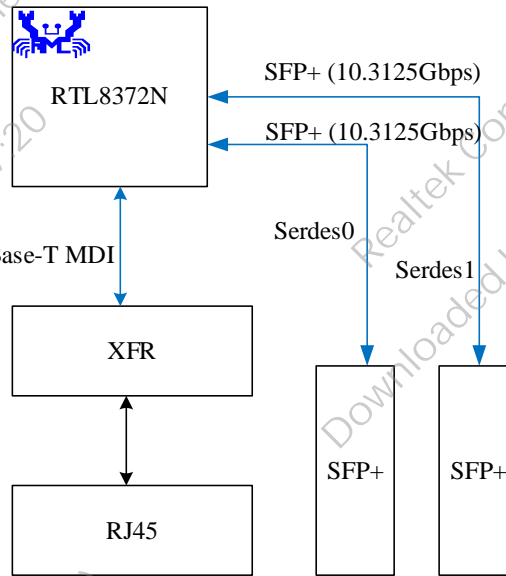


Figure 3. 4-Port 2.5GBASE-T + 2-Port 10G-R

4. Block Diagram

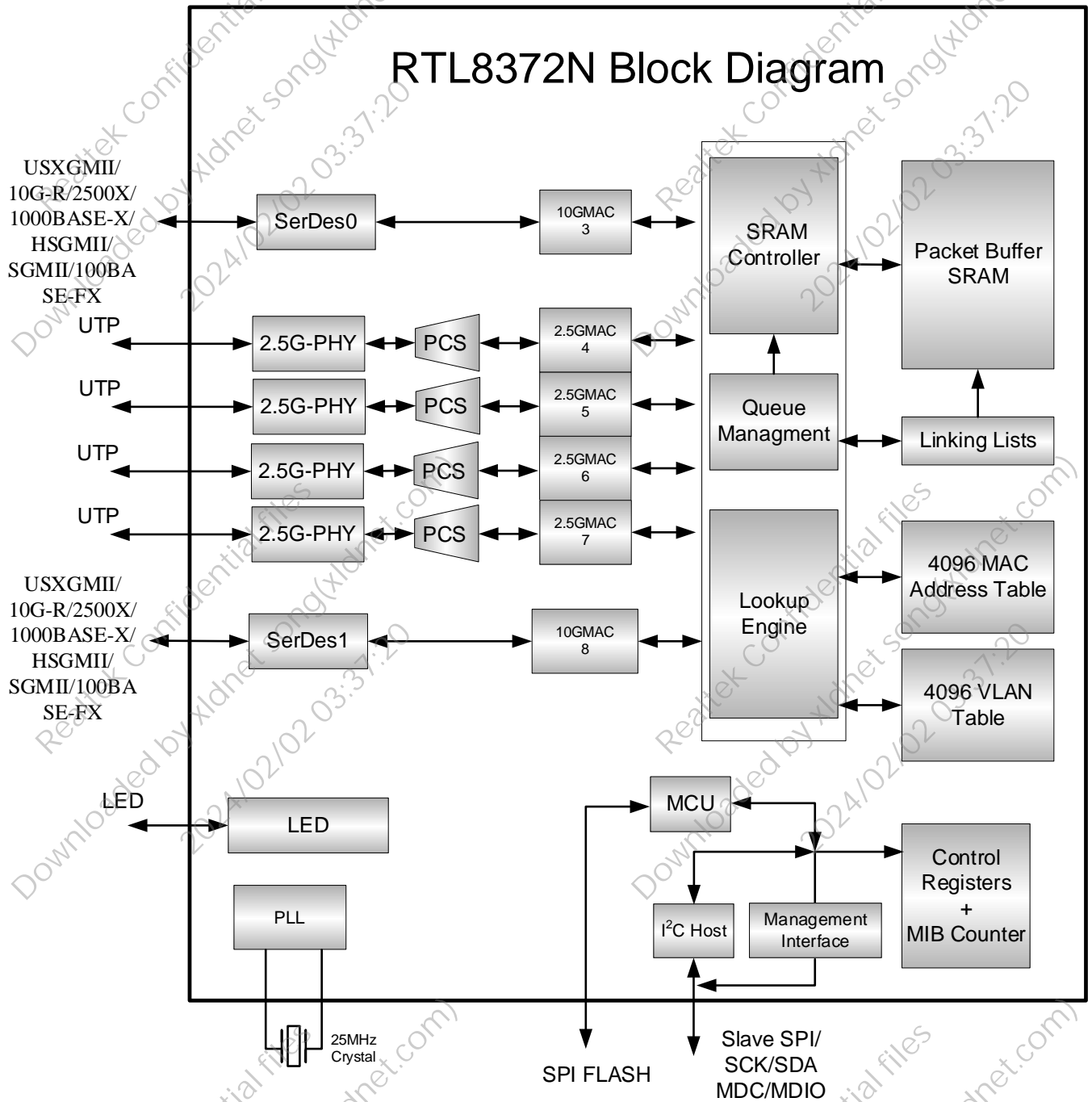


Figure 4. Block Diagram

5. Pin Assignments

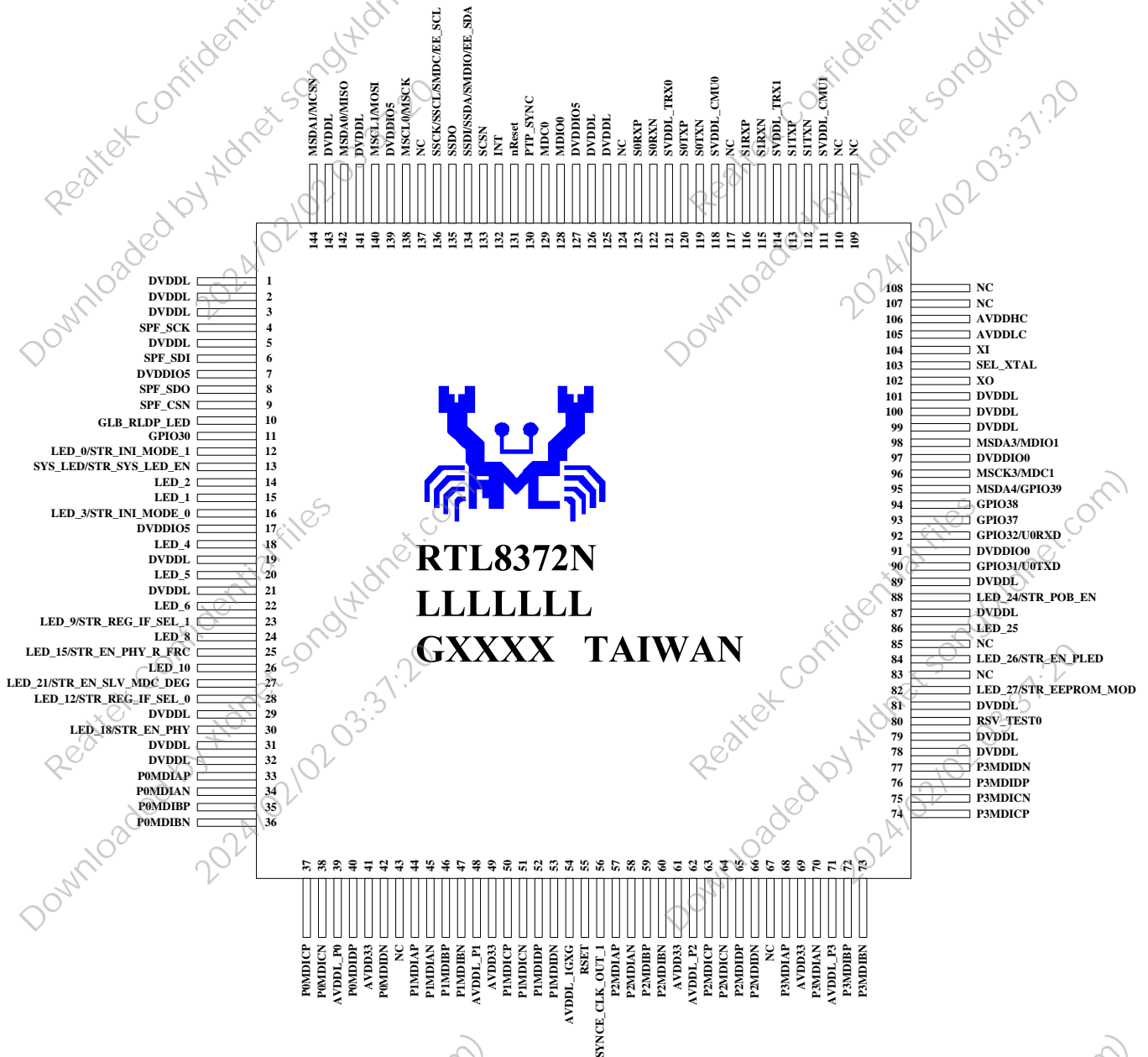


Figure 5. Pin Assignments

5.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 5).

5.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

DP: Digital Power Pin

DG: Digital Ground Pin

SP: SERDES Power Pin

I_{PU}: Input Pin With Pull-Up Resistor;
(Typical Value = 75KΩ)

I_{PD}: Input Pin With Pull-Down Resistor;
(Typical Value = 75KΩ)

I/O_{PU}: I_{PU} and O_{PU}

I_{SPU}: Input Pin With Schmitt Trigger and
Pull-Up Resistor

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

SG: SERDES Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor;
(Typical Value = 75KΩ)

O_{PD}: Output Pin With Pull-Down Resistor;
(Typical Value = 75KΩ)

I/O_{PD}: I_{PD} and O_{PD}

Table 1. Pin Assignments Table

Name	Pin No.	Type
DVDDL	1	DP
DVDDL	2	DP
DVDDL	3	DP
SPF_SCK	4	O _{PU}
DVDDL	5	DP
SPF_SDI	6	I/O _{PU}
DVDDIO5	7	DP
SPF_SDO	8	I/O _{PU}
SPF_CSN	9	I/O _{PU}
GLB_RLDP_LED	10	I/O _{PU}
GPIO30	11	I/O _{PU}
LED_0/STR_INI_MODE_1	12	I/O _{PU}
SYS_LED/STR_SYS_LED_EN	13	I/O _{PU}
LED_2	14	I/O _{PU}
LED_1	15	I/O _{PU}
LED_3/STR_INI_MODE_0	16	I/O _{PU}
DVDDIO5	17	DP
LED_4	18	I/O _{PU}
DVDDL	19	DP
LED_5	20	I/O _{PU}
DVDDL	21	DP
LED_6	22	I/O _{PU}
LED_9/STR_REG_IF_SEL_1	23	I/O _{PD}
LED_8	24	I/O _{PU}
LED_15/STR_EN_PHY_R_FRC	25	I/O _{PU}
LED_10	26	I/O _{PU}
LED_21/STR_EN_SLV_MDC_DEG	27	I/O _{PU}
LED_12/STR_REG_IF_SEL_0	28	I/O _{PD}
DVDDL	29	DP
LED_18/STR_EN_PHY	30	I/O _{PD}
DVDDL	31	DP
DVDDL	32	DP
P0MDIAP	33	AI/O
P0MDIAN	34	AI/O
P0MDIBP	35	AI/O
P0MDIBN	36	AI/O
P0MDICP	37	AI/O
P0MDICN	38	AI/O
AVDDL_P0	39	AP
P0MDIDP	40	AI/O
AVDD33	41	AP
P0MDIDN	42	AI/O
NC	43	-

Name	Pin No.	Type
P1MDIAP	44	AI/O
P1MDIAN	45	AI/O
P1MDIBP	46	AI/O
P1MDIBN	47	AI/O
AVDDL_P1	48	AP
AVDD33	49	AP
P1MDICP	50	AI/O
P1MDICN	51	AI/O
P1MDIDP	52	AI/O
P1MDIDN	53	AI/O
AVDDL_1GXG	54	AP
RSET	55	AO
SYNCE_CLK_OUT_1	56	AI/O
P2MDIAP	57	AI/O
P2MDIAN	58	AI/O
P2MDIBP	59	AI/O
P2MDIBN	60	AI/O
AVDD33	61	AP
AVDDL_P2	62	AP
P2MDICP	63	AI/O
P2MDICN	64	AI/O
P2MDIDP	65	AI/O
P2MDIDN	66	AI/O
NC	67	-
P3MDIAP	68	AI/O
AVDD33	69	AP
P3MDIAN	70	AI/O
AVDDL_P3	71	AP
P3MDIBP	72	AI/O
P3MDIBN	73	AI/O
P3MDICP	74	AI/O
P3MDICN	75	AI/O
P3MDIDP	76	AI/O
P3MDIDN	77	AI/O
DVDDL	78	DP
DVDDL	79	DP
RSV_TEST0	80	I _{PU}
DVDDL	81	DP
LED_27/STR_EEPROM_MOD	82	I/O _{PU}
NC	83	-
LED_26/STR_EN_PLED	84	I/O _{PU}
NC	85	-
LED_25	86	I/O _{PU}

Name	Pin No.	Type
DVDDL	87	DP
LED_24/STR_POB_EN	88	I/OPU
DVDDL	89	DP
GPIO31/U0TXD	90	I/OPU
DVDDIO0	91	DP
GPIO32/U0RXD	92	I/OPU
GPIO37	93	I/OPU
GPIO38	94	I/OPU
MSDA4/GPIO39	95	I/OPU
MSCK3/MDC1	96	OPU
DVDDIO0	97	DP
MSDA3/MDIO1	98	I/OPU
DVDDL	99	DP
DVDDL	100	DP
DVDDL	101	DP
XO	102	AO
SEL_XTAL	103	IPU
XI	104	AI
AVDDLC	105	AP
AVDDHC	106	AP
NC	107	-
NC	108	-
NC	109	-
NC	110	-
SVDDL_CMU1	111	SP
S1TXN	112	AO
S1TXP	113	AO
SVDDL_TRX1	114	SP
S1RXN	115	AI

Name	Pin No.	Type
S1RXP	116	AI
NC	117	-
SVDDL_CMU0	118	SP
S0TXN	119	AO
S0TXP	120	AO
SVDDL_TRX0	121	SP
S0RXN	122	AI
S0RXP	123	AI
NC	124	-
DVDDL	125	DP
DVDDL	126	DP
DVDDIO5	127	DP
MDIO0	128	I/OPU
MDC0	129	OPU
PTP_SYNC	130	I/OPD
nReset	131	ISPU
INT	132	I/OPU
SCSN	133	IPU
SSDI/SSDA/SMDIO/EE_SDA	134	I/OPU
SSDO	135	OPU
SSCK/SSCL/SMDC/EE_SCL	136	I/OPU
NC	137	-
MSCL0/MSCK	138	I/OPU
DVDDIO5	139	DP
MSCL1/MOSI	140	I/OPU
DVDDL	141	DP
MSDA0/MISO	142	I/OPU
DVDDL	143	DP
MSDA1/MCSN	144	I/OPU

6. Pin Descriptions

6.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P0MDIAP/N	33	AI/O	-	Port 0 Media Dependent Interface A~D. For 2.5GBase-T and 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.
	34			
P0MDIBP/N	35			
	36			
P0MDICP/N	37			
	38	AI/O	-	Each of the differential pairs has an internal 100-ohm termination resistor.
P0MDIDP/N	40			
	42			
P1MDIAP/N	44			
	45			
P1MDIBP/N	46	AI/O	-	Port 1 Media Dependent Interface A~D. For 2.5GBase-T and 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.
	47			
P1MDICP/N	50			
	51			
P1MDIDP/N	52			
	53	AI/O	-	Each of the differential pairs has an internal 100-ohm termination resistor.
P2MDIAP/N	57			
	58			
P2MDIBP/N	59			
	60			
P2MDICP/N	63	AI/O	-	Port 2 Media Dependent Interface A~D. For 2.5GBase-T and 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.
	64			
P2MDIDP/N	65			
	66			
	66			
P3MDIAP/N	68	AI/O	-	Port 3 Media Dependent Interface A~D. For 2.5GBase-T and 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-Te operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.
	70			
P3MDIBP/N	72			
	73			
P3MDICP/N	74			
	75	AI/O	-	Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIDP/N	76			
	77			
	77			
	77			

6.2. High Speed Serial Interface Pins

Table 3. High Speed Serial Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
S0TXP/N	120 119	AO	-	USXGMII/10G-R/2500BASE-X/1000BASE-X/HSGMII/SGMII/100BASE-FX Output Pins: 1.25GHz/3.125GHz/10.3125GHz Differential serial interface to transmit data. These pins must be pulled low with a 1K ohm resistor when not used.
S0RXP/N	123 122	AI	-	USXGMII/10G-R/2500BASE-X/1000BASE-X/HSGMII/SGMII/100BASE-FX Input Pins: 1.25GHz/3.125GHz/10.3125GHz Differential serial interface to receive data. These pins must be pulled low with a 1K ohm resistor when not used.
S1TXP/N	113 112	AO	-	USXGMII/10G-R/2500BASE-X/1000BASE-X/HSGMII/SGMII/100BASE-FX Output Pins: 1.25GHz/3.125GHz/10.3125GHz Differential serial interface to transmit data. These pins must be pulled low with a 1K ohm resistor when not used.
S1RXP/N	116 115	AI	-	USXGMII/10G-R/2500BASE-X/1000BASE-X/HSGMII/SGMII/100BASE-FX Input Pins: 1.25GHz/3.125GHz/10.3125GHz Differential serial interface to receive data. These pins must be pulled low with a 1K ohm resistor when not used.

6.3. General Purpose Interfaces

Table 4. General Purpose Interfaces

Pin Name	Pin No.	Type	Drive (mA)	Description
GPIO30	11	I/OPU	4	General Purpose Input/Output. Provides configurable I/O ports that can be configured for either input or output.
GPIO31/U0TXD	90	I/OPU	4	
GPIO32/U0RXD	92	I/OPU	4	
GPIO37	93	I/OPU	4	
GPIO38	94	I/OPU	4	
MSDA4/ GPIO39	95	I/OPU	4	

6.4. UART Interface

Table 5. UART Interface

Pin Name	Pin No.	Type	Drive (mA)	Description
GPIO31/U0TXD	90	I/OPU	4	UART0 Interface Transmit Data.
GPIO32/U0RXD	92	I/OPU	4	UART0 Interface Receive Data.

6.5. Management Interface Pins

Table 6. Management Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SCSN	133	IPU	4	SPI slave mode Chip Selection Input pin.

Pin Name	Pin No.	Type	Drive (mA)	Description
SSCK/SSCL/SMDC/EE_SCL	136	I/OPU	4	SPI slave mode Serial Clock Input pin. Slave I2C Interface Clock for external CPU to access DUT. Slave MII Management Interface Clock. Master I2C Interface Clock for EEPROM auto-download. (Selected via the hardware strapping REG_IF_SEL_0 & REG_IF_SEL_1).
SSDI/SSDA/SMDIO/EE_SDA	134	I/OPU	4	SPI slave mode Serial Data Input pin. Slave I2C Interface Data for external CPU to access DUT. Slave MII Management Interface Data. Master I2C Interface Data for EEPROM auto-download. (Selected via the hardware strapping REG_IF_SEL_0 & REG_IF_SEL_1).
SSDO	135	OPU	4	SPI slave mode Serial Data Output pin.
MDC0	129	OPU	4	Data Clock of Serial Management Interface(SMI Master 0).
MDIO0	128	I/OPU	4	Data I/O Serial Management Interface(SMI Master 0).
MSCK3/MDC1	96	OPU	4	Data Clock of Serial Management Interface(SMI Master 2) Master I2C Interface Clock.
MSDA3/MDIO1	98	I/OPU	4	Data I/O Serial Management Interface(SMI Master 2) Master I2C Interface Data.
MSDA4/GPIO39	95	I/OPU	4	Master I2C Interface Data.
MSCL0/MSCK	138	I/OPU	4	Master I2C Interface Clock. Master SPI Interface Clock.
MSDA0/MISO	142	I/OPU	4	Master I2C Interface Data. Master SPI Interface Data Output.
MSCL1/MOSI	140	I/OPU	4	Master I2C Interface Clock. Master SPI Interface Data Input.
MSDA1/MCSN	144	I/OPU	4	Master I2C Interface Data. Master SPI Chip Select Signal.
INT	132	I/OPU	4	Interrupt Output for External CPU.

6.6. SPI FLASH Interface Pins

Table 7. SPI FLASH Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SPF_CSN	9	OPU	4	SPI FLASH chip select signal.
SPF_SDO	8	I/OPU	4	SPI Serial FLASH Serial Data Output (RTL8372N input pin).
SPF_SDI	6	I/OPU	4	SPI Serial FLASH Serial Data Input (RTL8372N output pin).
SPF_SCK	4	OPU	4	SPI FLASH Clock.

6.7. LED Pins

Table 8. LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_0/ STR_INI_MODE_1	12	I/OPU	4	Port 3 LED0 Output Signal. LED0 indicates information is defined by register or EEPROM.
LED_1	15	I/OPU	4	Port 3 LED1 Output Signal. LED1 indicates information is defined by register or EEPROM.
LED_2	14	I/OPU	4	Port 3 LED2 Output Signal. LED2 indicates information is defined by register or EEPROM.
LED_3/ STR_INI_MODE_0	16	I/OPU	4	Port 4 LED0 Output Signal. LED3 indicates information is defined by register or EEPROM.
LED_4	18	I/OPU	4	Port 4 LED1 Output Signal. LED4 indicates information is defined by register or EEPROM.
LED_5	20	I/OPU	4	Port 4 LED2 Output Signal. LED5 indicates information is defined by register or EEPROM.
LED_6	22	I/OPU	4	Port 5 LED0 Output Signal. LED6 indicates information is defined by register or EEPROM.
LED_8	24	I/OPU	4	Port 5 LED1 Output Signal. LED8 indicates information is defined by register or EEPROM.
LED_9/ STR_REG_IF_SEL_1	23	I/OPD	4	Port 5 LED2 Output Signal. LED9 indicates information is defined by register or EEPROM.
LED_10	26	I/OPU	4	Port 6 LED0 Output Signal. LED10 indicates information is defined by register or EEPROM.
LED_12/ STR_REG_IF_SEL_0	28	I/OPD	4	Port 6 LED1 Output Signal. LED12 indicates information is defined by register or EEPROM.
LED_15/ STR_EN_PHY_R_FRC	25	I/OPU	4	Port 6 LED2 Output Signal. LED15 indicates information is defined by register or EEPROM.
LED_18/STR_EN_PHY	30	I/OPD	4	Port 7 LED0 Output Signal. LED18 indicates information is defined by register or EEPROM.
LED_21/STR_EN_SLV MDC_DEG	27	I/OPU	4	Port 7 LED1 Output Signal. LED21 indicates information is defined by register or EEPROM.
LED_24/STR_POB_EN	88	I/OPU	4	Port 7 LED2 Output Signal. LED24 indicates information is defined by register or EEPROM.
LED_25	86	I/OPU	4	Port 8 LED0 Output Signal. LED25 indicates information is defined by register or EEPROM.
LED_26/ STR_EN_PLED	84	I/OPU	4	Port 8 LED1 Output Signal. LED26 indicates information is defined by register or EEPROM.
LED_27/ STR_EEPROM_MOD	82	I/OPU	4	Port 8 LED2 Output Signal. LED_27 indicates information is defined by register or EEPROM.
SYS_LED/ STR_SYS_LED_EN	13	I/OPU	4	System LED. SYS_LED indicates information is defined by register or EEPROM.
GLB_RLDP_LED	10	I/OPU	4	RLDP LED. GLB_RLDP_LED indicates information is defined by register or EEPROM.

Note: LED_0 - LED_6, LED_8 - LED_10, LED_12, LED_15, LED_18, LED_21, LED_24 - LED_27 can be arbitrarily configured as Px_LEDy.

6.8. PTP Interface

Table 9. PTP Interface

Pin Name	Pin No.	Type	Drive (mA)	Description
PTP_SYNC	130	I/O _{PD}	4	Timer GPIO's output enable.

6.9. Configuration Strapping Pins

Table 10. Configuration Strapping Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SYS_LED/ STR_SYS_LED_EN	13	I/O _{PU}	4	When enable system LED, the LED change to system LED pin. 0b'0: Disable system LED 0b'1: Enable system LED <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
LED_0/ STR_INI_MODE_1	12	I/O _{PU}	4	Select Initialization Mode. 0b'00: Disable Internal CPU & Disable Autoload
LED_3/ STR_INI_MODE_0	16	I/O _{PU}	4	0b'01: EEPROM patch Switch & disable internal CPU 0b'10: Internal CPU boot from EEPROM 0b'11: Internal CPU boot from SPI FLASH <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
LED_9/ STR_REG_IF_SEL_1	23	I/O _{PD}	4	Select switch core register access interface: 0b'00: Slave I2C
LED_12/ STR_REG_IF_SEL_0	28	I/O _{PD}	4	0b'01: Slave SPI 0b'10: Slave MDC/MDIO Clause 22, and ID=0 0b'11: Slave MDC/MDIO Clause 22, and ID=29 <i>Note: These pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
LED_15/ STR_EN_PHY_R_FRC	25	I/O _{PU}	4	0b'0: Normal 0b'1: Force R for impedance not match environment. <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
LED_18/STR_EN_PHY	30	I/O _{PD}	4	Enable Embedded PHY. 0b'1: Enable embedded PHY 0b'0: Disable embedded PHY <i>Note1: Only valid for Internal xPHY.</i> <i>Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_21/ STR_EN_SLV_MDC_DEG	27	I/OPU	4	Enable slave MDC/MDIO Clause 22 Interface deglitch function. 0b'0: Disable 0b'1: Enable <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
LED_27/ STR_EEPROM_MOD	82	I/OPU	4	Select EEPROM Auto-Load Address Byte Size. 0b0: 8bit address type EEPROM, ex 24C16 0b1: 16bit address type EEPROM, ex 24C32 <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
LED_26/STR_EN_PLED	84	I/OPU	4	Parallel LED Output Enable: 0b'1: Enable 0b'0: Disable
LED_24/STR_POB_EN	88	I/OPU	4	Power On Light Enable. 0b'1: Enable 0b'0: Disable <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
RSV_TEST0	80	IPU	4	<i>Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset.</i>

6.10. Miscellaneous Pins

Table 11. Miscellaneous Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
XO	102	AO	-	25MHz/50MHz Crystal Clock Output Pin. 25MHz/50MHz +/-50ppm tolerance crystal output.
XI	104	AI	-	25MHz/50MHz Crystal Clock Input Pin. 25MHz/50MHz +/-50ppm tolerance crystal reference input. When either using an oscillator or driving an external 25MHz clock from another device, XO should be kept floating.
SEL_XTAL	103	IPU	-	XI Clock Input Frequency Selection. Pull Up: XI Input Frequency is 25MHz. Pull Down: XI Input Frequency is 50MHz. <i>Note: This pin must be kept floating, or pulled low via an external 4.7k ohm resistor upon power on or reset.</i>
RSET	55	AO	-	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
nRESET	131	ISPU	4	System Reset Input Pin.
NC	43, 67, 83, 85, 107, 108, 109, 110, 117, 124, 137	-	-	No Connection.

6.11. Power and GND Pins

Table 12. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO5	7, 17, 127, 139	DP	Digital I/O High Voltage Power for LED (not include LED_24 ~ LED_27) and I2C, slave SPI, RESET, INTERRUPT, and MDC0/ MDIO0. Analog High Voltage Power for SERDES.
DVDDIO0	91, 97	DP	Digital I/O High Voltage Power for LED_24 ~ LED_27, UART0 and MDC1/MDIO1.
SVDDL_CMU0	118	SP	Analog Low Voltage Power for SERDES0.
SVDDL_CMU1	111	SP	Analog Low Voltage Power for SERDES1.
SVDDL_TRX0	121	SP	Analog Low Voltage Power for SERDES0.
SVDDL_TRX1	114	SP	Analog Low Voltage Power for SERDES1.
AVDDL_C	105	AP	XTAL Low Voltage Power.
AVDDHC	106	AP	XTAL High Voltage Power.
DVDDL	1, 2, 3, 5, 19, 21, 29, 31, 32, 78, 79, 81, 87, 89, 99, 100, 101, 125, 126, 141, 143	DP	Digital Low Voltage Power.
AVDDL_P0	39	AP	Analog Low Voltage Power.
AVDDL_P1	48	AP	Analog Low Voltage Power.
AVDDL_P2	62	AP	Analog Low Voltage Power.
AVDDL_P3	71	AP	Analog Low Voltage Power.
AVDDL_1GXG	54	AP	Analog Low Voltage Power.
AVDD33	41, 49, 61, 69	AP	Analog High Voltage Power.

7. Physical Layer Functional Overview

7.1. MDI Interface

The RTL8372N embeds four 10/100/1000/2500M Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 2.5GBase-T, 1000Base-T, 100Base-TX, and 10Base-Te. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 2.5GBase-T and 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

7.2. 2.5GBase-T Transmit Function

The 2.5GBase-T transmit function performs 64B/65B coding, scrambling, and LDPC encoding. After LDPC framing, each 4 bits are grouped to a PAM16 symbol through gray code mapping scheme. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT-5e cable at 200MBaud/s through a D/A converter.

7.3. 2.5GBase-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, RFI cancellation, de-skew, and PAM16 decoding. Each 2048-bit-wide data is passed through a LDPC decoder and is sent to the XGMII interface. The RX MAC retrieves the packet data from the internal receive XGMII interface and sends it to the packet buffer manager.

7.4. 1000Base-T Transmit Function

The 1000Base-T transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

7.5. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

7.6. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.7. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.8. 10Base-Te Transmit Function

The output 10Base-Te waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.9. 10Base-Te Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.10. Auto-Negotiation for UTP

The RTL8372N obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8372N advertises full capabilities (2500Full, 1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.11. Crossover Detection and Auto Correction

The RTL8372N automatically determines whether it needs to crossover between pairs (see Table 13) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8372N automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 13. Media Dependent Interface Pin Mapping

Pairs	MDI				MDI Crossover			
	2.5GBase-T	1000Base-T	100Base-TX	10Base-Te	2.5GBase-T	1000Base-T	100Base-TX	10Base-Te
A	A	A	TX	TX	B	B	RX	RX
B	B	B	RX	RX	A	A	TX	TX
C	C	C	Unused	Unused	D	D	Unused	Unused
D	D	D	Unused	Unused	C	C	Unused	Unused

7.12. Polarity Correction

The RTL8372N automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-Te modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-Te mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-Te link is up. The polarity becomes unlocked when the link is down.

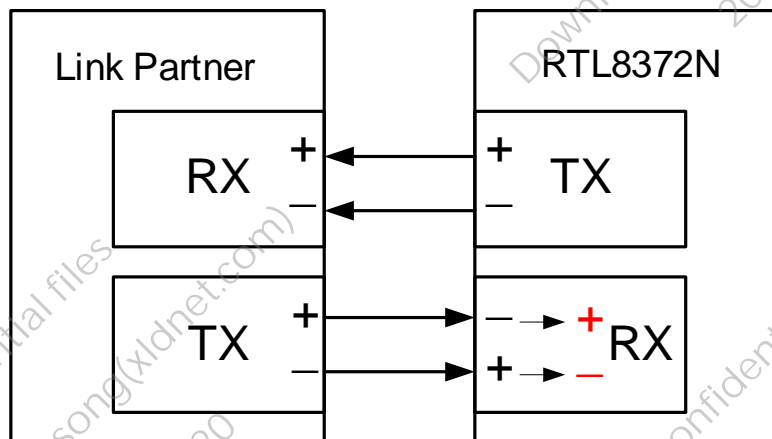


Figure 6. Conceptual Example of Polarity Correction

8. General Function Description

8.1. *Hardware Reset and Software Reset*

8.1.1. Hardware Reset

A hardware reset forces the RTL8372N to start the initial power-on sequence. First hardware will strap pins to give all default values when the 'nRESET' signal terminates. Next the configuration is auto-loaded from EEPROM (if EEPROM is detected), and then the complete SRAM BIST (Built-In Self-Test) process is run.

8.1.2. Software Reset

The RTL8372N supports software reset. Reset source is the signal that will trigger the reset command to the chip. The reset signal is low active.

8.2. *Layer 2 Learning and Forwarding*

The RTL8372N MAC address table consists of an 4096-entry look-up table. The RTL8372N supports IVL/SVL (Both Independent and Shared VLAN Learning).

8.2.1. Forwarding

When the VLAN egress filtering option is enabled, a received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded.

By default, the received broadcast/multicast frame will flood to VLAN member ports only, except for the source port.

IP multicast data packets involve multicast address table lookup and forwarding operations. If the table lookup returns a hit, the data packet is forwarded to member ports according to forwarding table setting. If the multicast address is not stored in the address table (i.e., lookup miss), according to a 2-bit action configuration the packet is dropped, trapped to the CPU, flooded to particular ports, or forward to specific port only.

8.2.2. Learning

The RTL8372N features a Layer 2 table (4096 entries). It uses a 4-way hash structure to store L2 entries. Each entry can be recorded in three formats, L2 Unicast entry, L2 Multicast entry, and SIP+DIP entry.

The L2 Unicast hash key is {MAC, FID/VID}, Multicast hash key is {MAC, FID/VID}, and the IPV4 Multicast hash key is {DIP, SIP}.

8.2.3. Address Table Aging

In a dynamic network topology, address aging allows the contents of the address table to always be the most recent and correct. A learned source address entry will be cleared (aged out) if the address learning process does not update it within an aging time period. The aging timer of the MAC address lookup table can be configured to between 0.2~13107 seconds (default value is approximately 300s).

8.3. *Reserved Multicast Address Handling*

The RTL8372N supports Reserved Multicast Address (RMA) as defined in the IEEE 802.1 standard. For each RMA, the actions include: trap to CPU, drop, normal forward, or forward but not trap to CPU port. The action priority is higher than the results of a L2 Table lookup. Default actions are shown in Table 14.

Table 14. Reserved Multicast Address Default Actions

Name	Address	Default
Bridge Group Address	01-80-C2-00-00-00	Forward
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01	Drop
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02	Drop
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03	Forward
Reserved	01-80-C2-00-00-04 ~ 01-80-C2-00-00-07, 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C, 01-80-C2-00-00-0F	Forward
Provider Bridge Group Address	01-80-C2-00-00-08	Forward
Provider Bridge GVRP Address	01-80-C2-00-00-0D	Forward
LLDP IEEE Std 802.1AB Link Layer Discovery Protocol Multicast Address	01-80-C2-00-00-0E	Forward
All LANs Bridge Management Group Address	01-80-C2-00-00-10	Forward
Load Server Generic Address	01-80-C2-00-00-11	Forward
Loadable Device Generic Address	01-80-C2-00-00-12	Forward
Reserved	01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F	Forward
Generic Address for All Manager Stations	01-80-C2-00-00-18	Forward
Generic Address for All Agent Stations	01-80-C2-00-00-1A	Forward
GMRP	01-80-C2-00-00-20	Forward
GVRP	01-80-C2-00-00-21	Forward
Reserved for use by Multiple Registration Protocol (MRP) applications	01-80-C2-00-00-22 - 01-80-C2-00-00-2F	Forward
CDP(Cisco Discovery Protocol)	01-00-0C-CC-CC-CC	Forward
Cisco Shared Spanning Tree Protocol	01-00-0C-CC-CC-CD	Forward
LLDP	(01:80:c2:00:00:0e or 01:80:c2:00:00:03 or 01:80:c2:00:00:00) && ethertype = 0x88CC	Forward

8.4. IEEE 802.3x Flow Control

The RTL8372N supports IEEE 802.3x full duplex flow control. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the results of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

8.5. Half Duplex Backpressure

There are two mechanisms for half-duplex backpressure: collision-based and carrier-based.

8.5.1. Collision-Based Backpressure (Jam Mode)

If the input buffer is ready to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The reschedule procedure is:

- The RTL8372N will drive TXEN to high and send a 12-byte Jam signal (pattern is preamble + SFD + 4bytes 0xAA). Then the RTL8372N will drive TXEN to low
- When the link partner receives the Jam signal, it will feedback a 4-byte signal (pattern is [CRC value] ^ 0x01 or [00, 00, 00, 01]) according to preamble + SFD is fully exported or not, then the RTL8372N will drive RXDV to low
- The link partner waits for a random back-off time then re-sends the packet. The timing is shown in the Figure 7 below

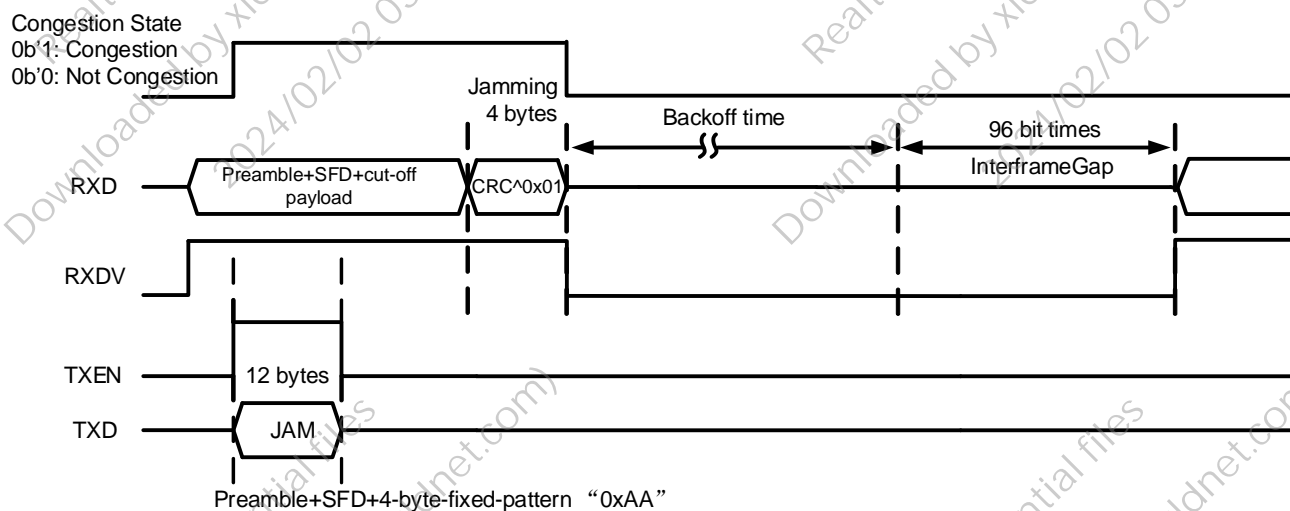


Figure 7. Collision-Based Backpressure Signal Timing

8.5.2. Carrier-Based Backpressure (Defer Mode)

If the input buffer is about to overflow, this mechanism will send a 0xAA pattern to defer the other station's transmission. The RTL8372N will continuously send the defer signal until the input buffer overflow is resolved.

8.6. *Illegal Frame Filtering*

Illegal frames such as CRC error packets, runt packets (length < 64 bytes), and oversize packets (length > maximum length) will be discarded by the RTL8372N. The maximum TX and RX length of each port can be set to different values.

8.7. *IEEE 802.1p and IEEE 802.1Q (VLAN)*

The RTL8372N ports are divided into uplink port and downlink port according to register configuration in VLAN module. There are four types of packets forwarded between ports: downstream packet, upstream packet, customer stream packet and service stream packet.

The RTL8372N supports 4096-entry VLAN table. CVID decision module can be configured as ACL ingress VID, IEEE 802.1Q tag based VLANs, and port-based VLANs. The RTL8372N has a global register to decide whether to turn on the ingress filter and egress filter of the whole CVLAN system. In addition, per port has a bit that controls whether packets received from this port are filtered out by the CVLAN ingress filter. SVLAN module always executes ingress & egress filtering.

The RTL8372N features an accept frame type function: packets from an ingress port will be accepted or dropped based on the checking result that packets whether have VLAN tag.

8.8. *Layer 2 Traffic Suppression (Storm Control)*

The RTL8372N supports the storm filter based on RX and TX for each port. The storm types are broadcast storm, known multicast storm, unknown multicast storm, and unknown Destination Address (DA) unicast storm. Each storm of per port will point to a meter (one of 64 groups of shared meters) through which the purpose of speed restriction can be achieved.

8.9. *Loop Detection*

The RTL8372N supports the Realtek Loop Detection Protocol (RLDP) to determine network loop existence. When the loop is detected, the LED corresponding to the looped port will blinking in a specific way. At the same time, the loop event flag will be set.

The Loop Detection Protocol can be divided into two modes. One is caused by the mapping changes of port and Switch MAC Address (SA), called SA moving mode, and the other is to send the loop detection packet regularly, called Periodically checking mode.

8.10. Bandwidth Control

8.10.1. Input Bandwidth Control

The RTL8372N has input bandwidth control ability per port. If the rate of received packets is faster than the Ingress Rate Limit of this port, the switch will send a pause frame to the link partner or drop packets according to its ingress flow control setting.

8.10.2. Output Bandwidth Control

The RTL8372N has output bandwidth control per port, and supports Weighted Fair-Queuing(WFQ) and Shared(Shaped) Round-Robin(SRR) scheduling algorithm to schedule bandwidth other than guarantee bandwidth.

8.11. Wake-On-LAN (WOL)

The RTL8372N can monitor the network for a Magic Packet, and notify the MAC via the interrupt when such a packets occurs. Then the system can be restored to a normal state to process incoming jobs.

A Magic Packet Wake-up occurs only when the following conditions are met:

- The received Magic Packet does not contain a CRC error
- The Magic Packet pattern matches; i.e., 6 * 0xff + 16 * DID (Destination ID) in any part of a valid Ethernet packet

8.12. Interrupt

In configuration registers, the RTL8372N has a global interrupt enable register. When this bit is disabled, all interrupts will not be sent to CPU or external interrupt output pin. The Interrupt output active mode can be configured via register configuration.

When any event that needs to be notified to the CPU occurs, the RTL8372N will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has happened interrupt.

8.13. Priority Decision and Remarking

The RTL8372N identifies the priority of packets based on several types of Quality of Service (QOS) priority information:

- Port-based Priority Assignment
- Dot1Q-Based Priority Assignment
- ACL-based Priority Assignment
- DSCP-based Priority Assignment

- SVLAN-based Priority Assignment
- RSPAN-based Priority Assignment

8.13.1. Priority Selection

The RTL8372N has two Priority arbitration weight tables to decide which type of priority should be applied when multiple types of priority exist. Each port can select its Priority arbitration weight table.

8.13.2. Port-Based Priority Assignment

Port-based priority assignment specifies a 3-bit priority for each physical port. When a packet is received from a physical port, it is assigned the 3-bit Port-based priority of that physical port.

8.13.3. IEEE 802.1Q-Based Priority Assignment

In IEEE 802.1Q-based priority assignment, when a packet is VLAN-tagged or priority-tagged, the 3-bit priority is specified by tag. When a packet is untagged, it is deemed no the 802.1Q-based priority. When the priority comes from a packet, the 1Q-based priority is acquired by mapping 3-bit tag priority to 3-bit priority though a configurable Dot1Q-Based Priority remapping table.

8.13.4. ACL-Based Priority Assignment

When a packet hits the ACL entry and the ACL-Based priority of the packet is assigned according to priority action, a 3-bit ACL based priority will be obtained.

8.13.5. DSCP-Based Priority Assignment

The RTL8372N has a table to map 6-bit DSCP values to 3-bit dscp-based priority. The table has 64 entries, and per entry is 3-bit. The table is implemented with register.

8.13.6. SVLAN-Based Priority Assignment

For downlink packets, if there is a SVLAN Tag, the priority in the stag is taken as the SVLAN-Based priority value.

8.13.7. RSPAN-Based Priority Assignment

The internal priority of RSPAN traffic will refer to the priority in RSPAN tag and use this priority as the user priority. The RTL8372N provides a mapping table from RSPAN tag priority to internal priority.

8.13.8. Remarking

RTL8372N Remarking can be divided into 1P remarking, STAG remarking, and DSCP remarking. For 1P remarking, there is a register configuration to decide whether to execute 1P remarking. The S-Priority of STAG will not be affected by 1P remarking. ACL and per port setting could determine whether a packet will execute DSCP remarking.

8.14. Packet Scheduling (SRR and WFQ)

The RTL8372N has eight queues per port. The Packet Scheduler controls the multiple traffic classes (i.e., controls the packet sending sequence of the priority queue). The RTL8372N has two scheduling algorithms: Shared (Shaped) Round-Robin (SRR) and Weighted Fair-Queuing (WFQ). Note that the Strict Priority queue is the highest priority of all queues, and overrides WFQ & WRR. A larger strict priority queue ID indicates the priority is higher.

The Scheduler operates as follows:

- Weighted Fair-Queuing (WFQ): Byte-count
- Shared (Shaped) Round-Robin (SRR): Packet-count

Note that WFQ and SRR cannot exist at the same time.

8.15. Port Mirror

The RTL8372N supports one set of Port Mirror function for all ports. If a frame meets the TX and RX mirroring port conditions, the RTL8372N duplicates the packet to the monitor port. The RTL8372N also supports RSPAN mirror and Sample mirror. If the sample rate is greater than 0, one mirrored packet is actually sent to the monitor port every n packets matching the mirror condition.

8.16. Management Information Base (MIB)

The RTL8372N MIB (Management Information Base) counters include:

- RFC 1213 – TCP/IP-based MIB-II
- RFC 3635 – Ethernet-like MIB
- RFC 2863 – Interface Group MIB
- RFC 2819 – RMON(Remote Network Monitoring) MIB
- RFC 1493 – Bridge MIB
- RFC 2674 – Bridge MIB Extension

8.17. LED Indicators

The RTL8372N supports parallel LEDs for each port. The RTL8372N supports up to 3-LEDs per port for 2.5G port and 10G port. Each pin may have different indicator information (defined in Table 15). Refer to section 6.7 LED Pins, page 14 for pin details. The RTL8372N provides power on and reset LED blinking function.

Table 15. LED Definitions

LED Status	Description
LED Off	LED pin output disable.
Dup/Col	Duplex/Collision, Indicator. Blinking when collision occurs.
Link/Act	Link, Activity Indicator. Link/Act Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.
Link	Link Indicator.
Spd10G	10Gbps Speed Indicator.
Spd2.5G	2.5Gbps Speed Indicator.
Spd1000	1000Mbps Speed Indicator.
Spd100	100Mbps Speed Indicator.
Spd10	10Mbps Speed Indicator.
Spd10G/Act	10Gbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd2.5G/Act	2.5Gbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd10G(5G)/Act	5/10Gbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd5G(2.5G)/Act	2.5/5Gbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd2.5G(1G)/Act	1/2.5Gbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd1000(100)/Act	100/1000Mbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd1000(10)/Act	10/1000Mbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.
Spd100(10)/Act	10/100Mbps Speed/Activity Indicator. Blinking when the corresponding port is transmitting or receiving.

The LED pin also supports pin strapping configuration functions. The LED pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset.

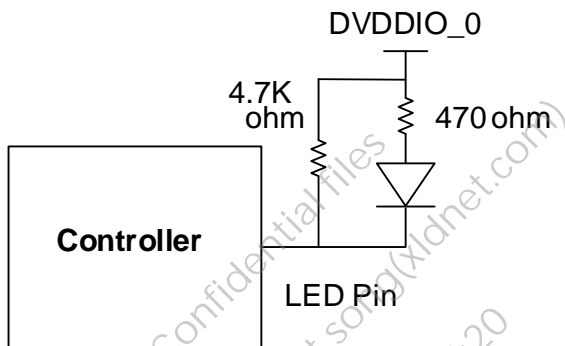
If the pin input is pulled high upon reset, the pin output is active low after reset. If the pin input is pulled down upon reset, the pin output is active high after reset. For details refer to Figure 8 and Figure 9. Typical values for pull-up/pull-down resistors are 4.7KΩ.

The PnLED1 can be combined with PnLED0 or PnLED2 or PnLED3 as a Bi-color LED.

LED_ PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

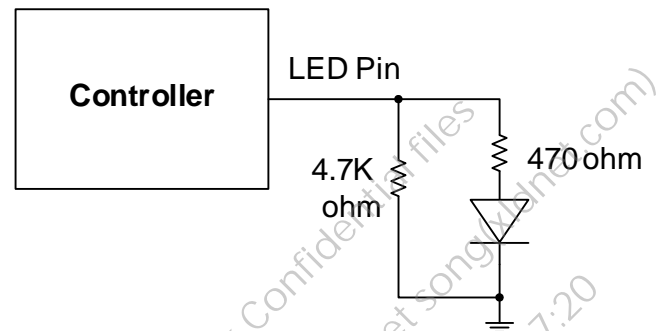
- P0LED1 should be pulled up upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled up upon reset. In this configuration, the output of these pins is active low after reset
- P0LED1 should be pulled down upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

Pull-Up



LED Pins Output Active Low

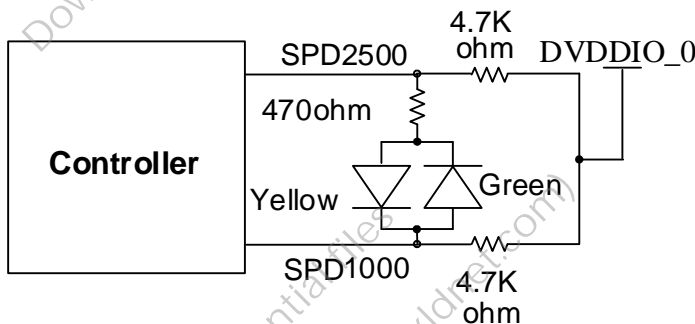
Pull-Down



LED Pins Output Active High

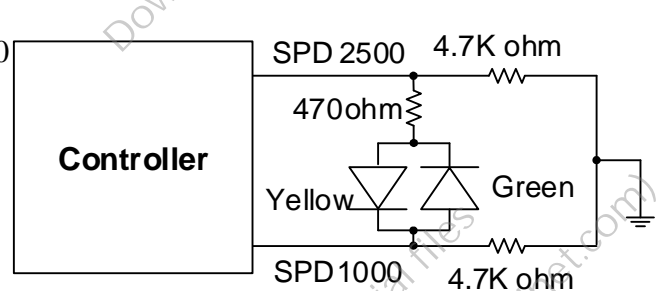
Figure 8. Pull-Up and Pull-Down of LED Pins for Single-Color LED in Parallel Mode

Pull-Up



LED Pins Output Active Low

Pull-Down



LED Pins Output Active High

Figure 9. Pull-Up and Pull-Down of LED Pins for Bi-Color LED in Parallel Mode

8.18. EEPROM Configuration

The EEPROM can be divided into two sizes: 1Kb~16Kb and 32Kb~128Kb. Using the small size EEPROM will reduce the time required to load code, as well as the cost. The address size of the small size EEPROM is 8 bits, while the larger EEPROM size is 16 bits (addressable space up to 64K). The small and large size EEPROM address timing waveform is different, and the auto-load size is shown in the register.

8.19. Precision Time Protocol (PTP)

Precision Time Protocol (PTP) stands for a series of IEEE specifications, such as IEEE 1588 Ver.2, that synchronize the time of day or a standard time across a network system. The PTP protocol is typically used in Audio Video Bridging (AVB) applications, industrial and factory automation applications, or test and measurement systems.

The fundamental concept of PTP is timing-stamping specified PTP frames with high precision as close to the transmission media as possible.

The PTP core consist of three main blocks:

- Packet Time Stamping
- Synchronized PTP Clock
- Time Application Interface (TAI)

By combining the above functions, the RTL8372N provides complete and accurate support for applications in a time-synchronous system.

8.20. IEEE 802.3az Energy Efficient Ethernet (EEE)

The RTL8372N supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100 Mbps, 1000 Mbps, IEEE 802.3az-2016 EEE at 2.5GBASE-T and 10GBASE-T. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported.

8.21. Realtek Cable Tester

The RTL8372N features the Realtek Cable Tester (RTCT). The RTCT function could be used to detect short, open or impedance mismatch in each differential pair.

9. Interface Descriptions

9.1. I2C Master for EEPROM Auto-load

The EEPROM interface of the RTL8372N uses the serial bus I2C to read the Serial EEPROM. When the RTL8372N is powered up, it drives SCK and SDA to read the configuration/code data from the EEPROM by strapping configuration.

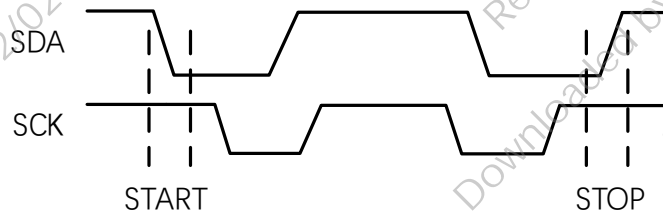


Figure 10. I2C Start/Stop State Waveform

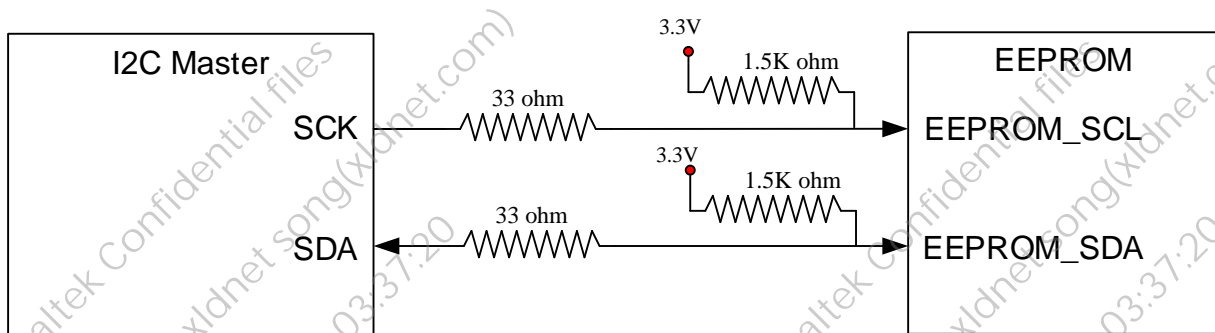


Figure 11. I2C Master for EEPROM Auto-load Interface Connection Example

The EEPROM can be divided into two sizes: 1Kb~16Kb and 32Kb~128Kb. The address of the small size EEPROM is 8-bits, however the larger EEPROM has word-high addressing and word-low addressing, and it is 16-bits (two bytes).

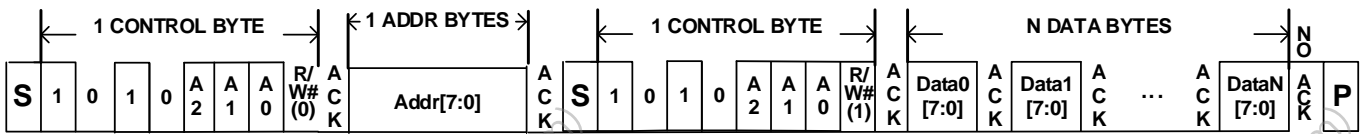


Figure 12. Small Size (1Kb~16Kb) EEPROM Read

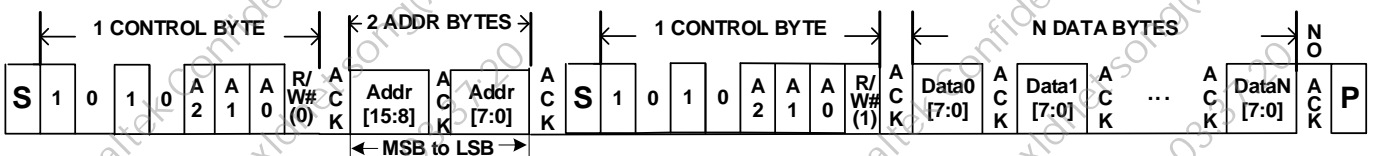


Figure 13. Large Size (32Kb~128Kb) EEPROM Read

9.2. I2C Master Interface for External Slave I2C Device

The RTL8372N supports the master I2C interface to access external slave I2C devices, such as POE / SFP / SFP +. The master I2C interface adopts standard mode and supports random read, random write, sequential read and sequential write. The supported frequency of the master I2C interface includes 50KHz, 100KHz, 400KHz and 2.5MHz.

9.3. I2C Slave Interface for External CPU

When EEPROM auto-load is completed, the RTL8372N registers can be accessed through I2C and I2C works in slave mode. It has two I/O pins (i.e., SDA and SCK). SDA is the access data signal, and SCK is the clock signal. The drive mode of pad is expected to be open drain in this slave mode. The I2C Slave Interface supports standard modes.

The single random read/write data sequence is shown in Figure 14 and Figure 15. Write and read can be divided into little endian and big endian according to the order of data.

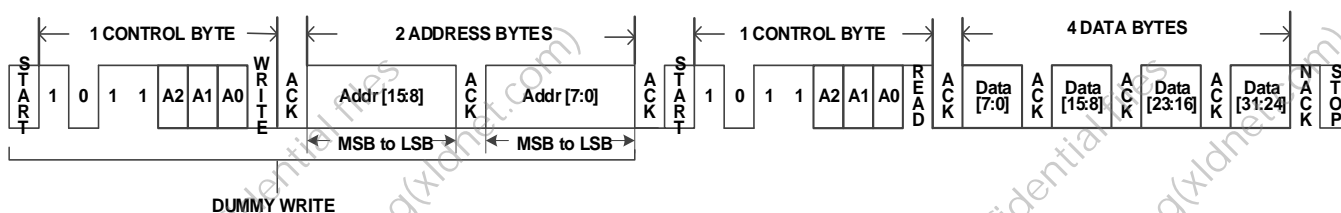


Figure 14. I2C Single Random Read (Little Endian)

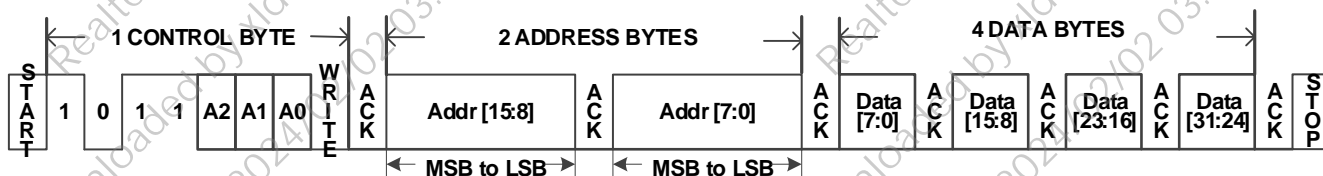


Figure 15. I2C Single Random Write (Little Endian)

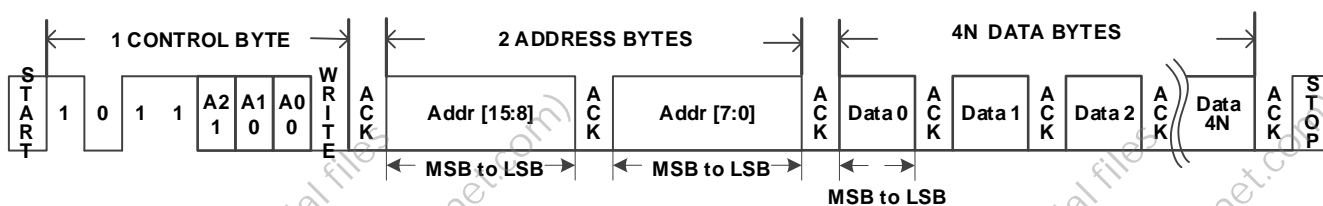
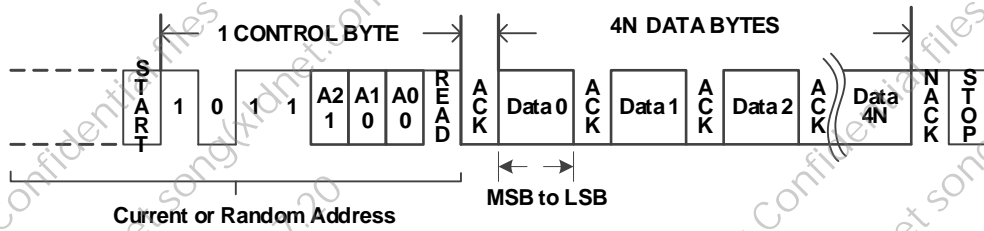
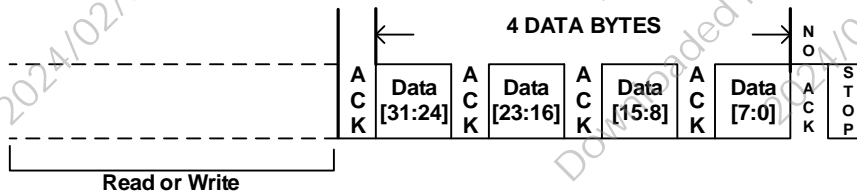
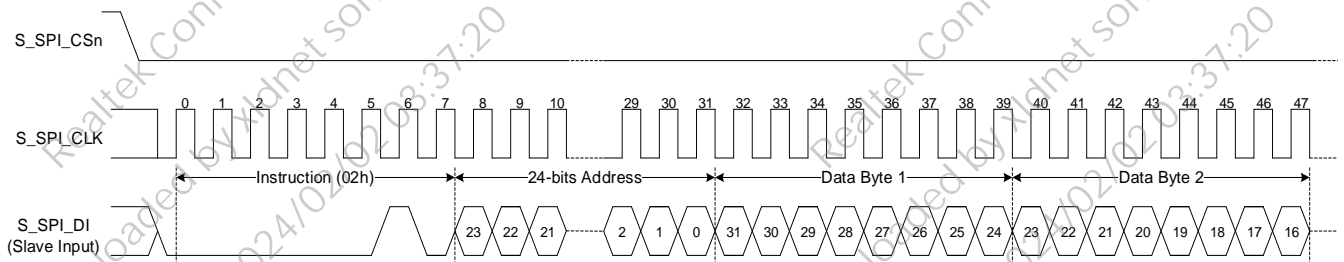
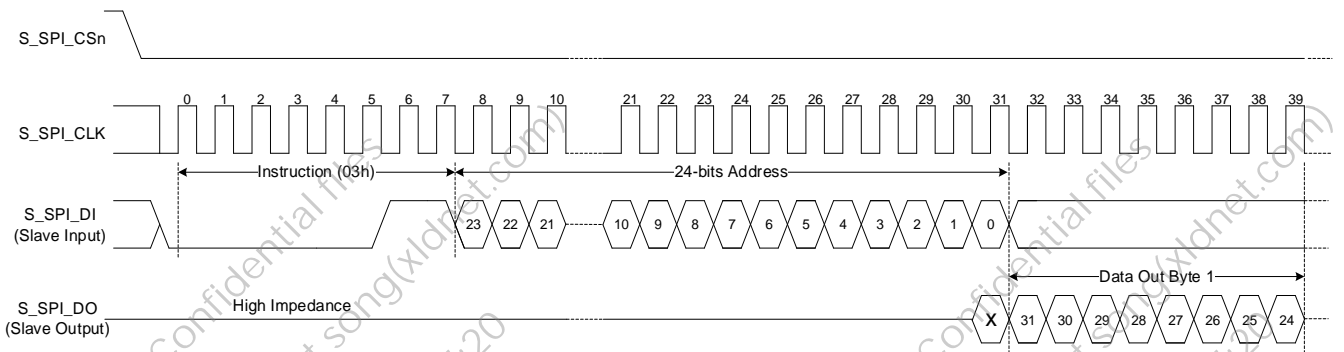


Figure 16. I2C Sequential Write (Little Endian)


Figure 17. I2C Sequential Read (Little Endian)

Figure 18. Big Endian

9.4. SPI Slave for External CPU

The RTL8372N supports a SPI-Slave Management Interface that can be enabled via Strapping Pin Configuration. An external CPU can configure or manage the RTL8372N internal register through the Slave SPI Interface.


Figure 19. Slave SPI for External CPU Access Write Command

Figure 20. Slave SPI for External CPU Access Read Command

9.5. Master SPI Interface

The RTL8372N supports the Master SPI interface to access external SPI devices (i.e., PSE and Flash) by changing register configuration.

According to the planning of SPI Master, when the SPI Master drives the Address field, it is executed in the order of high byte first like Addr[31:24] → Addr[23:16] → Addr[15:8] → Addr[7:0]. The device memory address width can be set to 0 ~ 4byte via the register configuration. During write Data, data is executed in low byte order, such as Data[7:0] → Data[15:8]... → Data[n]. In the process of reading data, the SPI master will also fill the received data into the register of data [7:0] → data [15:8]... → data [n].

The master SPI interfaces is connected to two different sets of pins, which are used to connect FLASH and PSE respectively.

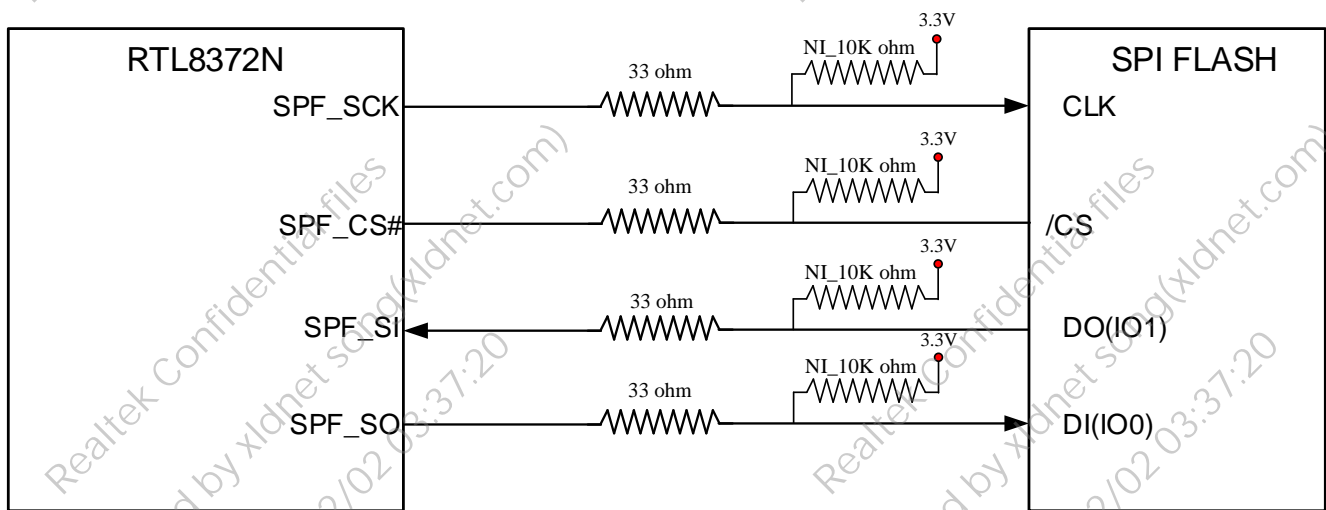


Figure 21. SPI FLASH Interface Connection Example

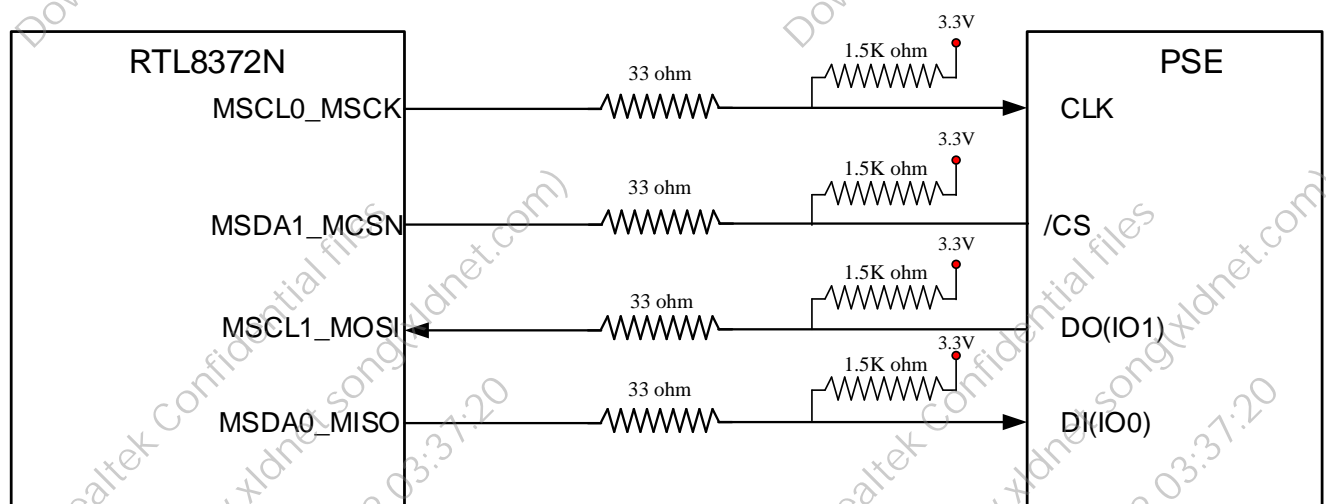


Figure 22. Master SPI Interface for PSE Connection Example

9.6. External PHY Register Access Interface

The RTL8372N support MDC/MDIO master mode. The Master (RTL8372N) can access the Slave (external PHY) registers via the MDC/MDIO interface.

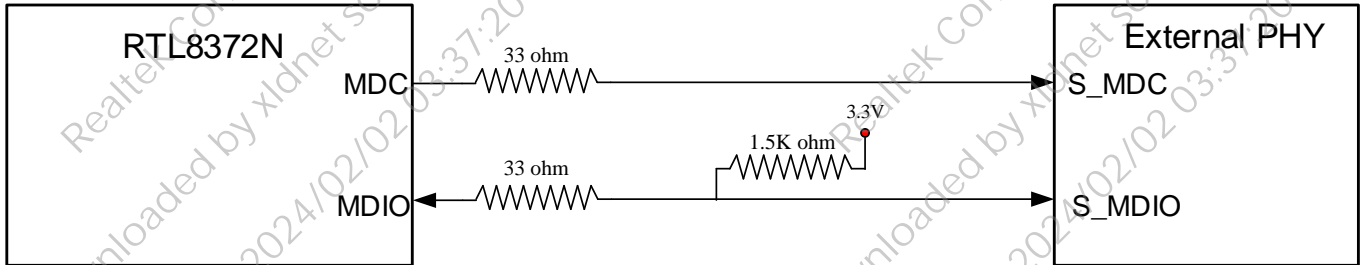


Figure 23. SMI (MDC/MDIO) Interface Connection Example

Table 16. SMI (MDC/MDIO) Access Format

	Management Frame Fields							IDLE
	PRE	ST	OP	PHYAD	DEVAD	TA	ADDRESS /DATA	
Address	1...1	00	00	AAAAA	EEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	AAAAA	EEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	AAAAA	EEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	AAAAA	EEEE	Z0	DDDDDDDDDDDDDDDD	Z

9.7. Slave SMI Interface for External CPU Access

The RTL8372N registers can be accessed via Slave MDC and MDIO via an external CPU (Decided by Strapping configuration).

Table 17. Slave SMI Access Format

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1.....1	01	10	A ₄ A ₃ A ₂ A ₁ A ₀	R ₄ R ₃ R ₂ R ₁ R ₀	Z0	D ₁₅D ₀	Z
Write	1.....1	01	01	A ₄ A ₃ A ₂ A ₁ A ₀	R ₄ R ₃ R ₂ R ₁ R ₀	10	D ₁₅D ₀	Z

Note: By default, a slave needs a 32-bit Preamble (PRE) for accessing a slave via the Slave SMI interface. An External CPU can configure the Slave to enable the preamble suppression function.

9.8. SERDES Interface

The RTL8372N supports two SERDES interfaces. SERDES 0 and SERDES 1 supports USXGMII(10G-SXGMII mode)/HSGMII/SGMII to connect PHY transceiver, 10G-R/2500BASE-X/1000BASE-X/100BASE-FX to connect Fiber OE module.

9.8.1. USXGMII 10G-SXGMII Mode

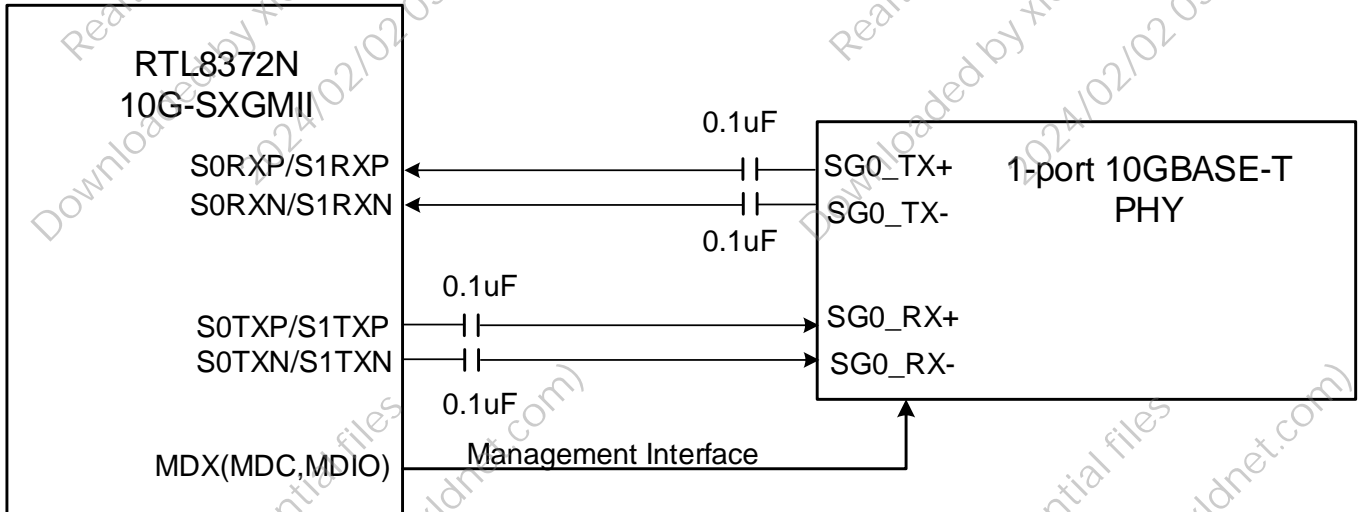


Figure 24. Signal Diagram of USXGMII 10G-SXGMII Mode of the GMAC3/GMAC8

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 18. Absolute Maximum Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+120	°C
DVDDIO0, DVDDIO5, AVDD33, AVDDHC	GND-0.3	+3.63	V
DVDDL, AVDDL, SVDDL_CMU0, SVDDL_CMU1, SVDDL_TRX0, SVDDL_TRX1, AVDDL_P0, AVDDL_P1, AVDDL_P2, AVDDL_P3, AVDDL_1GXG	GND-0.3	+1.05	V

10.2. Operating Range

Table 19. Recommended Operating Range

Parameter	Min	Typ.	Max	Units	
Ambient Operating Temperature TA	0	-	70	°C	
Junction Temperature	-	-	115	°C	
AVDD33, AVDDHC	3.14	3.3	3.46	V	
DVDDIO0	3.3V	3.14	3.3	3.46	V
	2.5V	2.38	2.5	2.62	V
	1.8V	1.7	1.8	1.9	V
DVDDIO5	3.14	3.3	3.46	V	
DVDDL, AVDDL, SVDDL_CMU0, SVDDL_CMU1, SVDDL_TRX0, SVDDL_TRX1, AVDDL_P0, AVDDL_P1, AVDDL_P2, AVDDL_P3, AVDDL_1GXG	0.92	0.95	0.98	V	

10.3. Thermal Characteristics

10.3.1. Assembly Description

Table 20. Assembly Description

Package	Type	DOFU QFN
	Dimension (L×W)	11 × 11 mm ²
	Thickness	1.25 mm
PCB	PCB Dimension (L×W)	76.2 × 114.3 mm ²
	PCB Thickness	1.6 mm
	Number of Cu Layer-PCB	4-Layer: - L1 Copper Coverage: 20% - L2 Copper Coverage: 90% - L3 Copper Coverage: 90% - L4 Copper Coverage: 20%

10.3.2. Simulation Conditions

Table 21. Simulation Conditions

Input Power	3.3W
Test Board (PCB)	4L
Control Condition	Air Flow = 0 m/s

10.3.3. Thermal Performance of DOFU QFN on PCB Under Still Air Convection

Table 22. Thermal Performance of DOFU QFN on PCB Under Still Air Convection

Chip Mode	PCB Layer	External Heat Sink	θ_{JB}	θ_{JC}	θ_{JA}	Ψ_{JT}	Ψ_{JB}
RTL8372N	4L	With	7.7	4.6	10.3	4.2	4.4
		Without			20.6	0.3	7.4

Note:

θ_{JB} : Junction to board thermal resistance

θ_{JC} : Junction to case thermal resistance

θ_{JA} : Junction to ambient thermal resistance

Ψ_{JT} : Junction-to-top-center thermal characterization parameter

Ψ_{JB} : Junction-to-board thermal characterization parameter

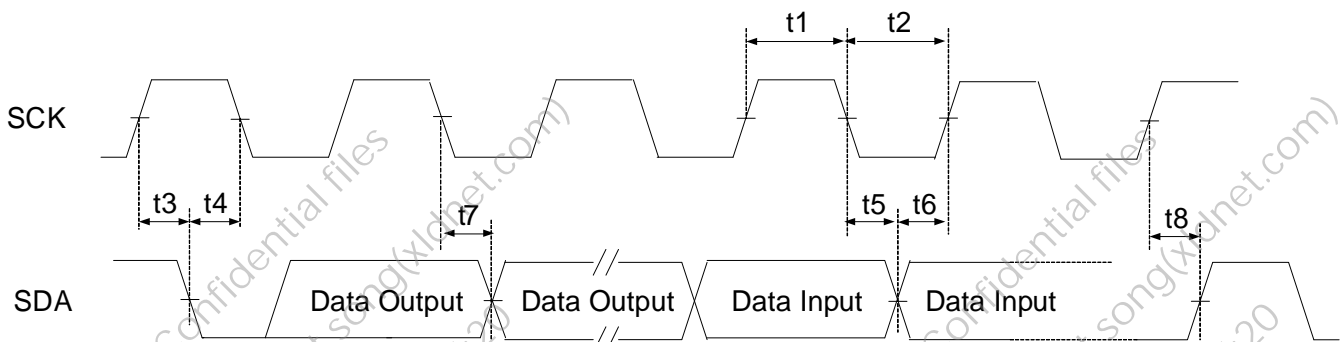
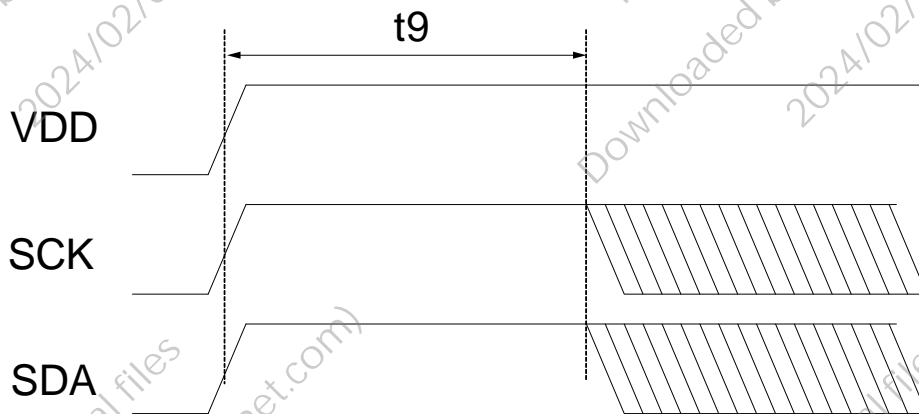
10.4. DC Characteristics

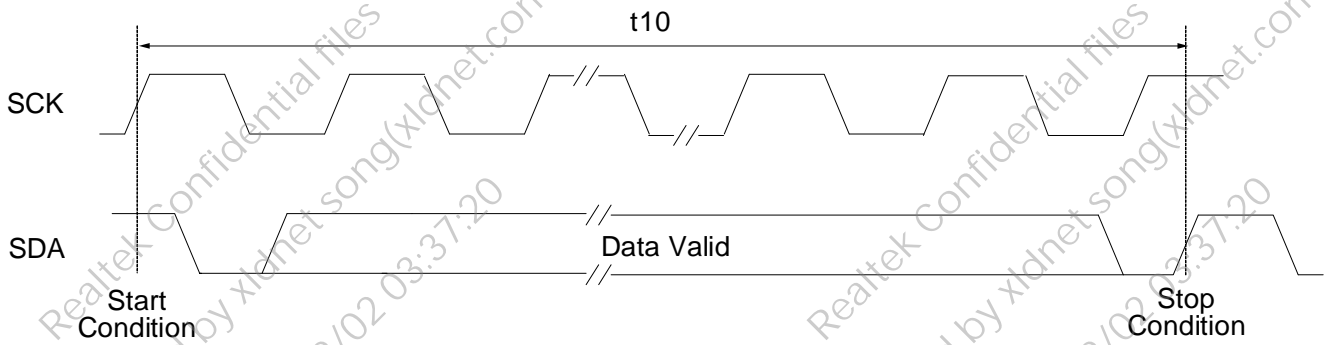
Table 23. DC Characteristics

Parameter	SYM	Min	Typ.	Max	Unit	Note
VDDIO = 3.3V						
TTL Input High Voltage	V_{ih}	2.0	-	-	V	-
TTL Input Low Voltage	V_{il}	-	-	0.8	V	-
Output High Voltage	V_{oh}	2.4	-	$V_{DD33}+0.3$	V	-
Output Low Voltage	V_{ol}	-0.3	-	0.4	V	-

10.5. AC Characteristics

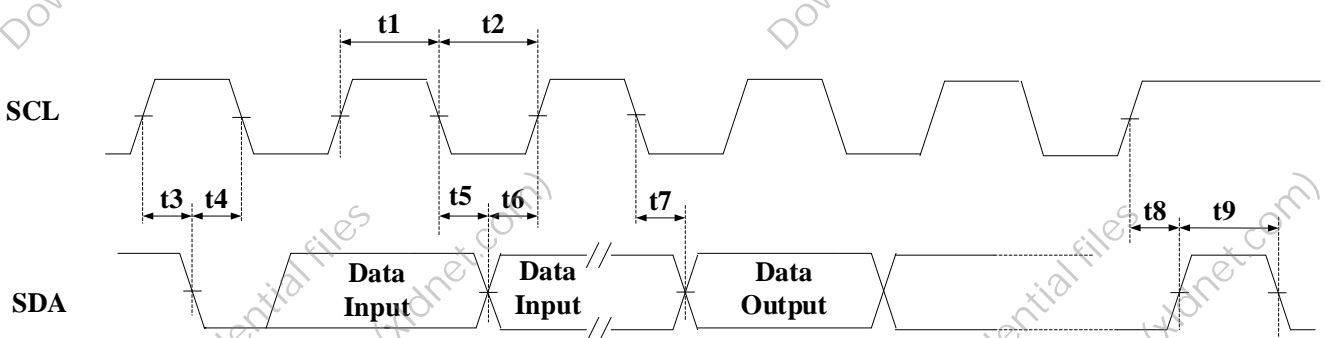
10.5.1. I2C Master for EEPROM Timing


Figure 25. I2C Master Mode Timing

Figure 26. SCK/SDA Power on Timing


Figure 27. EEPROM Auto-Load Timing
Table 24. Master I2C for EEPROM Auto-load Timing Characteristics

Symbol	Description	Type	Min	Typ.	Max	Units
Fsck	SCK Frequency.	O	-	1	-	MHz
Tsck	SCK Cycle.	O	-	1.00	-	us
t1	SCK High Time.	O	0.45	0.50	-	us
t2	SCK Low Time.	O	0.45	0.50	-	us
t3	START Condition Setup Time.	O	0.45	0.50	-	us
t4	START Condition Hold Time.	O	0.45	0.50	-	us
t5	Data Input Hold Time.	I	20	-	-	ns
t6	Data Input Setup Time.	I	20	-	-	ns
t7	Data Output Delay.	O	0.15	0.25	0.40	us
t8	STOP Condition Setup Time.	O	0.45	0.50	-	us
t9	SCK/SDA Active from Reset Ready.	O	-	-	-	-
t10	EEPROM Auto-Load Timing.	O	-	-	-	-
tBUF	Time the bus free before new START.	O	1.25	1.50	-	us

10.5.2. I2C Slave Interface Timing


Figure 28. I2C Slave Mode for External CPU Access Interface Timing Characteristics
Table 25. Slave I2C Timing Characteristics

Symbol	Description	Min	Typ.	Max	Units
Fscl	SCL Frequency.	-	-	2.5	MHz
t1	SCL High Time.	60	-	-	ns
t2	SCL Low Time.	120	-	-	ns
t3	START Condition Setup Time.	120	-	-	ns
t4	START Condition Hold Time.	120	-	-	ns
t5	Data Hold Time.	11	-	-	ns
t6	Data Setup Time.	11	-	-	ns
t7	Data to Clock Output Delay.	0	-	54	ns
t8	STOP Condition Setup Time.	120	-	-	ns
t9	Bus Free Time between STOP and START.	120	-	-	ns

10.5.3. SPI FLASH Interface Timing Characteristics

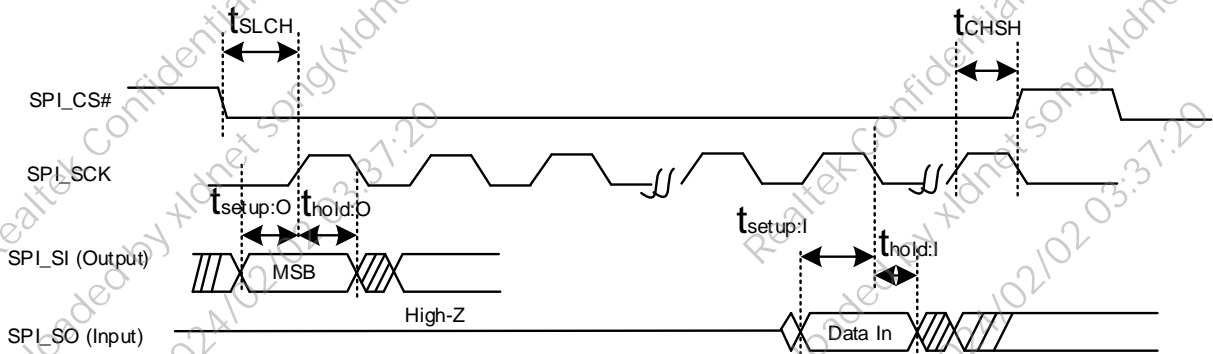


Figure 29. SPI FLASH Timing Characteristics

Table 26. SPI FLASH AC Timing

Symbol	Description	Type	Min	Typ.	Max	Units
$F_{SPI_SCK}^*$	Clock Period of the SPI_SCK.	O	-	62.5	-	MHz
Duty	Duty Cycle of the SPI_SCK.	O	45	50	55	%
t_{SLCH}	CS# Active Setup Time.	O	6	-	-	ns
t_{CHSH}	CS# Active Hold Time.	O	6	-	-	ns
$t_{setup:O}$	Data Output Setup Time.	O	3.3	-	-	ns
$t_{hold:O}$	Data Output Hold Time.	O	6	-	-	ns
$t_{setup:I}$	Data Input Setup Time.	I	6.5	-	-	ns
$t_{hold:I}$	Data Input Hold Time.	I	0	-	-	ns
t_{SHSL}	SPI_CS Deselect Time.	O	-	-	-	ns

* Test Condition: $F_{SPI_SCK}=62.5MHz$

10.5.4. SPI Master Controller Interface Characteristics

The RTL8372N SPI Master Controller Interface supports the register configuration to select data sampling at the clock rising edge or data sampling at the clock falling edge.

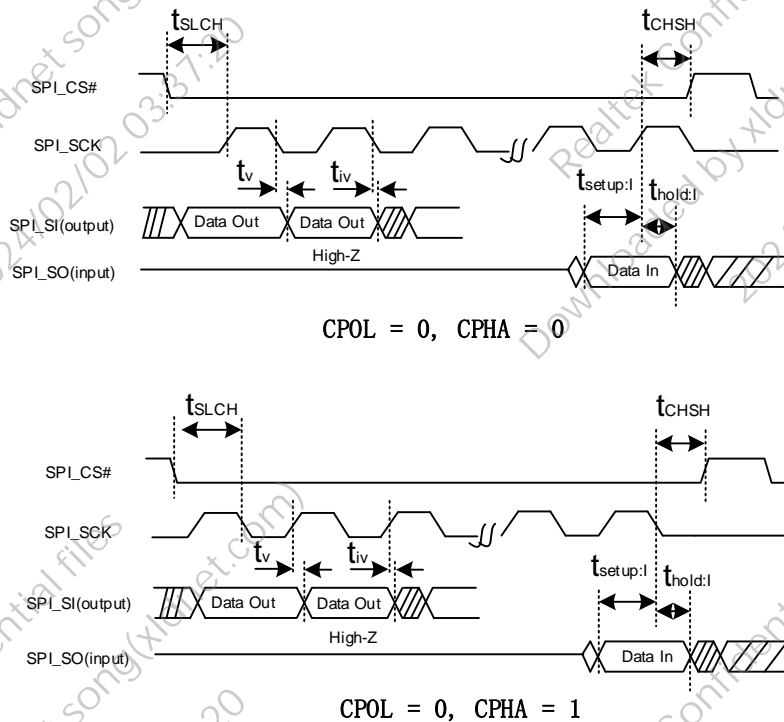


Figure 30. SPI Master Controller Interface Characteristics

Table 27. SPI Master Controller Interface AC Timing

Symbol	Description	Min	Typ.	Max	Units
T	Clock Period of the SPI_SCK.	36	-	996	ns
Duty	Duty Cycle of the SPI_SCK.	45	50	55	%
tSLCH	CS# Active Setup Time.	18	-	-	ns
tCHSH	CS# Active Hold Time.	18	-	-	ns
tv	Data Output Valid Time.	-	-	6	ns
tiv	Data Output Invalid Time.	-1.347	-	-	ns
tsetup:l	Data Input Setup Time.	18	-	-	ns
thold:l	Data Input Hold Time.	6	-	-	ns

10.5.5. Slave SPI for External CPU Access Interface Timing Characteristics

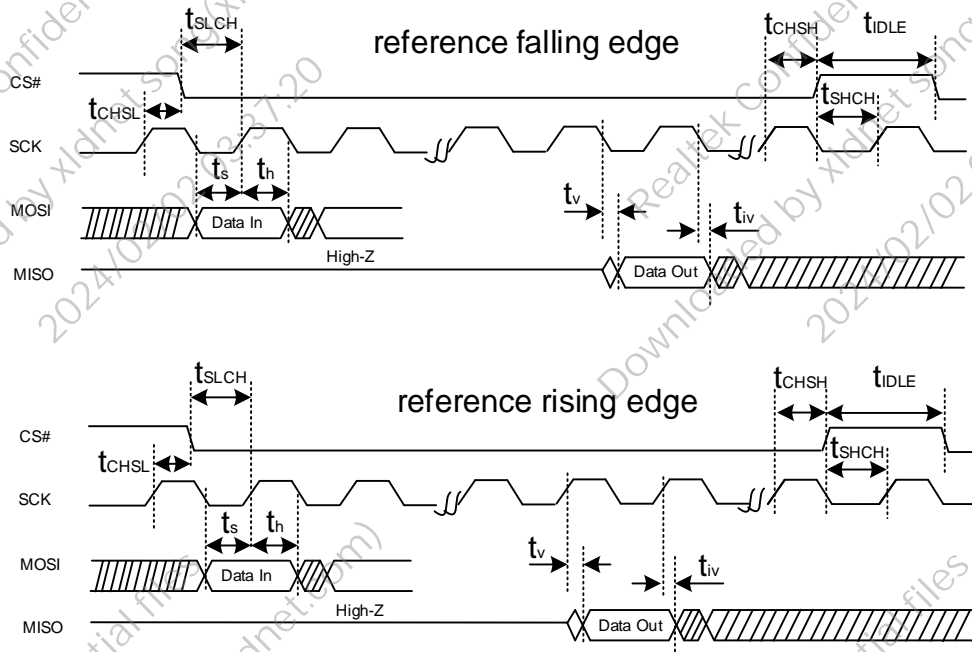


Figure 31. Slave SPI for External CPU Access Interface Timing Characteristics

Table 28. Slave SPI Timing Characteristics

Symbol	Description	Min	Typ.	Max	Units	
f _{SCK}	Clock Frequency of the SPI_SCK.	Reference falling edge	-	-	-	MHz
		Reference rising edge	-	-	13.5	MHz
T _{SCK}	Clock Period of the SPI_SCK.	Reference falling edge	-	-	-	ns
		Reference rising edge	74	-	-	ns
t _s	Data Input Setup Time.	12	-	-	ns	
t _h	Data Input Hold Time.	12	-	-	ns	
t _v	SCK to MISO Valid.	-	-	11	ns	
t _{iv}	SCK to MISO Invalid.	0	-	-	ns	
t _{SLCH}	CS# Active Setup Time.	18	-	-	ns	
t _{CHSH}	CS# Active Hold Time.	18	-	-	ns	
t _{SHCH}	CS# Not Active Setup Time.	18	-	-	ns	
t _{CHSL}	CS# Not Active Hold Time.	18	-	-	ns	
t _{IDLE}	CS# High Time.	18	-	-	ns	

10.5.6. SMI(MDC/MDIO) Timing Characteristics

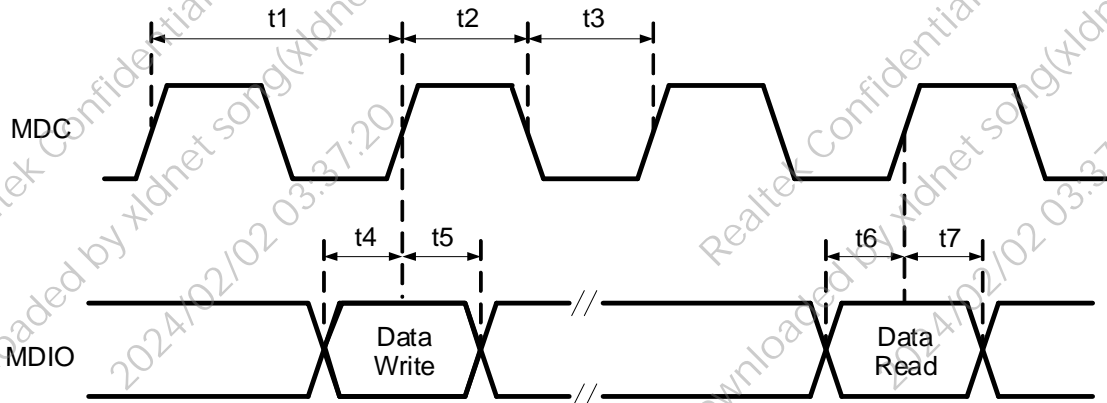


Figure 32. MDIO Sourced by Master (RTL8372N)

Table 29. SMI (MDC/MDIO) Timing Characteristics

Symbol	Description	Type	Min	Typ.	Max	Units
t1	MDC Clock Period.	O	-	400	-	ns
t2	MDC High Time.	O	-	200	-	ns
t3	MDC Low Time.	O	-	200	-	ns
t4	MDIO to MDC Rising Setup Time (Write data).	O	-	179	-	ns
t5	MDIO to MDC Rising Hold Time (Write data).	O	-	221	-	ns
t6	MDIO to MDC Rising Setup Time (Read data).	I	24	-	-	ns
t7	MDIO to MDC Rising Hold Time (Read data).	I	0	-	-	ns

10.5.7. Slave SMI(MDC/MDIO) for External CPU Access Interface Timing Characteristics

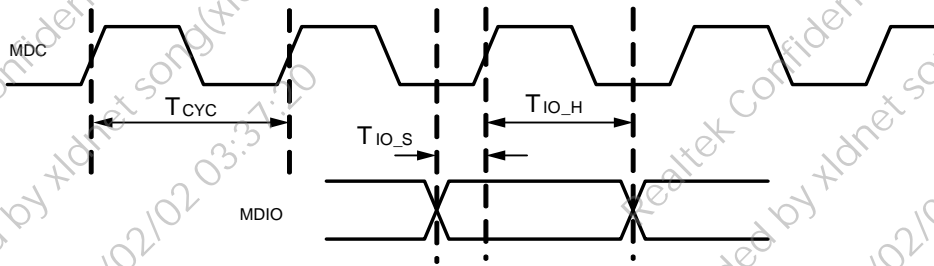


Figure 33. MDIO Sourced by Master (External CPU)

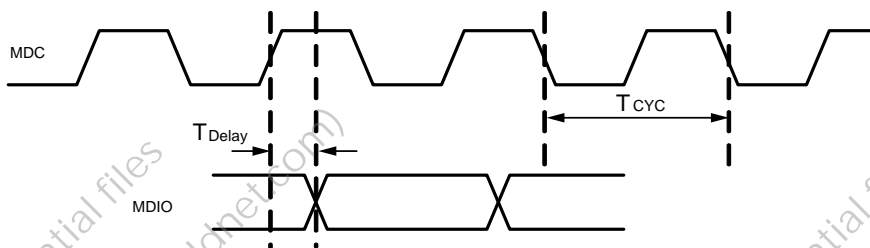


Figure 34. MDIO Sourced by Slave (RTL8372N)

Table 30. Slave SMI (MDC/MDIO) Timing Characteristics

Symbol	Description	I/O	Min	Typ.	Max	Units
T _{CYC}	MDC Clock Period.	I	100	400	-	ns
T _{IO_S}	MDIO to MDC Rising Setup Time (Write Data).	I	11.5	-	-	ns
T _{IO_H}	MDIO to MDC Rising Hold Time (Write Data).	I	24	-	-	ns
T _{Delay}	Clock to Data Delay Time (Read Data).	O	10	-	70	ns

10.5.8. Clock Characteristics

Table 31. Crystal Characteristics

Symbol	Description/Condition	Min	Typ.	Max	Unit
F _{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F _{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type.	-50	-	+50	ppm
F _{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
V _{ih}	Input High Voltage.	2.0	-	-	V
V _{il}	Input Low Voltage.	-	-	0.8	V

10.5.9. SGMII/1000Base-X Characteristics

Table 32. SGMII/1000Base-X Differential Transmitter Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	799.92	800	800.08	ps	$800\text{ps} \pm 100\text{ppm}$
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mV	-
Eye Mask	T_Y2	-	-	500	mV	-
Output Differential Voltage	$V_{\text{TX-DIFFp-p}}$	300	700	1000	mV	-
Minimum TX Eye Width	$T_{\text{TX-EYE}}$	0.7	-	-	UI	-
Output Jitter	$T_{\text{TX-JITTER}}$	-	-	0.3	UI	$T_{\text{TX-JITTER-MAX}} = 1 - T_{\text{TX-EYE-MIN}} = 0.30\text{UI}$
Data dependent jitter	-	-	0.0875	-	UI	-
Output Rise Time	$T_{\text{TX-RISE}}$	0.125	-	0.25	UI	20% ~ 80%
Output Fall Time	$T_{\text{TX-FALL}}$	0.125	-	0.25	UI	20% ~ 80%
Output impedance	R_{TX}	40	-	140	ohm	single-end
AC Coupling Capacitor	C_{TX}	80	100	120	nF	-
Transmit Length in PCB	L_{TX}	-	-	10	inch	-

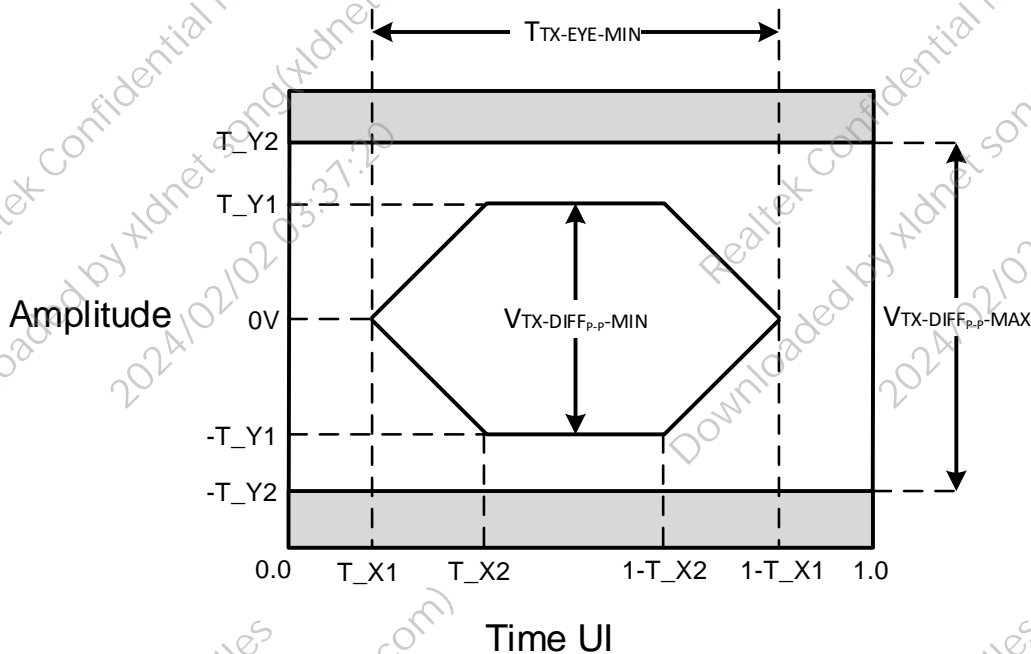
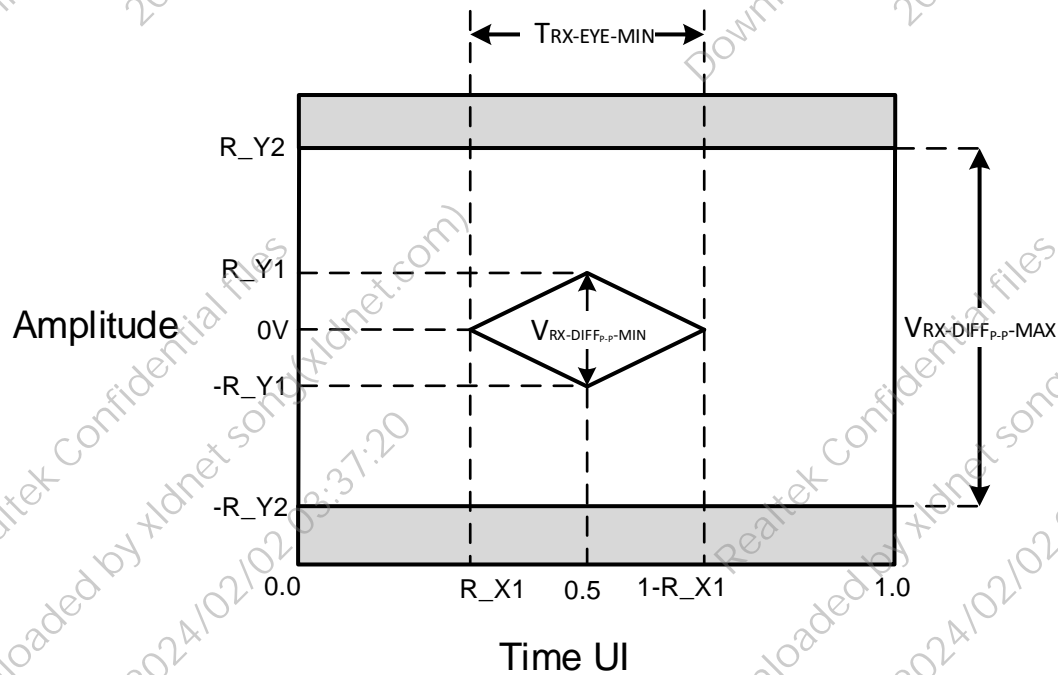

Figure 35. SGMII/1000Base-X Differential Transmitter Eye Diagram

Table 33. SGMII/1000Base-X Differential Receiver Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	799.92	800	800.08	ps	$800\text{ps} \pm 100\text{ppm}$
Eye Mask	R_X1	-	-	0.15	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	600	mV	-
Input Differential Voltage	$V_{\text{RX-DIFF-P}}$	200	-	1200	mV	-
Minimum RX Eye Width	$T_{\text{RX-EYE}}$	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{\text{RX-JITTER}}$	-	-	0.6	UI	$T_{\text{RX-JITTER-MAX}} = 1 - T_{\text{RX-EYE-MIN}} = 0.6\text{UI}$
Differential Resistance	R_{RX}	80	100	120	ohm	-


Figure 36. SGMII/1000Base-X Differential Receiver Eye Diagram

10.5.10. HSGMII/2500 Base-X Characteristics

Table 34. HSGMII/2500Base-X Differential Transmitter Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask	T_X1	-	-	0.175	UI	-
Eye Mask	T_X2	-	-	0.39	UI	-
Eye Mask	T_Y1	200	-	-	mV	-
Eye Mask	T_Y2	-	-	600	mV	-
Output Differential Voltage	V _{TX-DIFFp-p}	500	-	1200	mV	-
Output Jitter	TJ	T _{TX-JITTER}	-	0.35	UI	-
	DJ		-	0.165	UI	-
Minimum TX Eye Width	T _{TX-EYE}	0.65	-	-	UI	-
Output Rise Time	T _{TX-RISE}	0.125	-	-	UI	20% ~ 80%
Output Fall Time	T _{TX-FALL}	0.125	-	-	UI	20% ~ 80%
Differential Resistance	R _{TX}	80	100	120	ohm	-
AC Coupling Capacitor	C _{TX}	80	100	120	nF	-
Transmit Length in PCB	L _{TX}	-	-	10	inch	-

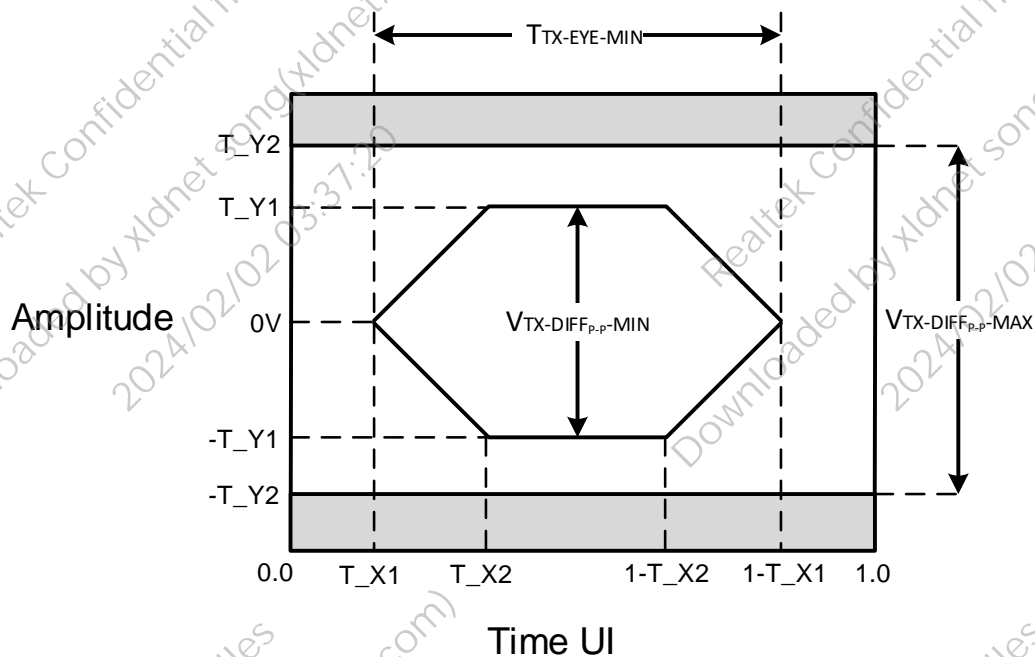
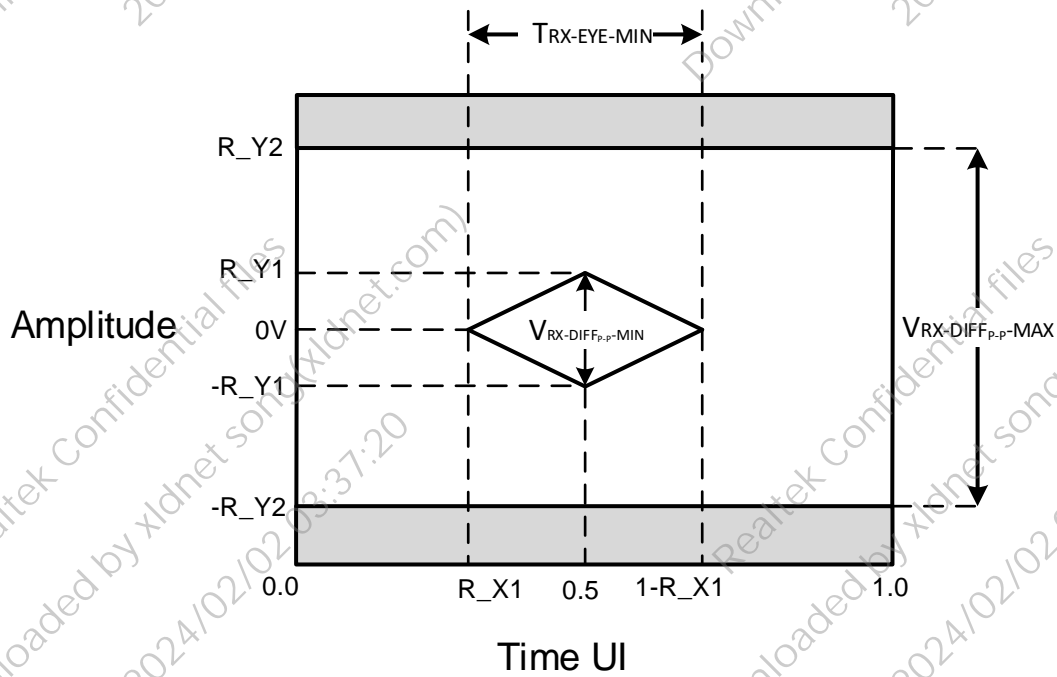

Figure 37. HSGMII/2500Base-X Differential Transmitter Eye Diagram

Table 35. HSGMII/2500Base-X Differential Receiver Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	319.968	320	320.032	ps	$320\text{ps} \pm 100\text{ppm}$
Eye Mask	R_X1	-	-	0.275	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	800	mV	-
Input Differential Voltage	$V_{\text{RX-DIFFP-P}}$	200	-	1200	mV	-
Minimum RX Eye Width	$T_{\text{RX-EYE}}$	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{\text{RX-JITTER}}$	-	-	0.6	UI	$T_{\text{RX-JITTER-MAX}} = 1 - T_{\text{RX-EYE-MIN}} = 0.6\text{UI}$
Differential Resistance	R_{RX}	80	100	120	ohm	-


Figure 38. HSGMII/2500Base-X Differential Receiver Eye Diagram

10.5.11. USXGMII Characteristics

Table 36. USXGMII Differential Transmitter Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	-	97	-	ps	-
Output Differential Voltage	$V_{TX-DIFFp-p}$	400	-	1200	mV	-
Total Jitter	T_J	-	-	0.28	UIpp	-
Transmitter output impedance on chip	R_{TX}	-	100	-	ohm	-

Table 37. USXGMII Differential Receiver Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	-	97	-	ps	-
Input Differential Voltage	$V_{RX-DIFFp-p}$	200	-	1200	mV	-
Receiver input impedance on chip	R_{RX}	-	100	-	ohm	-

10.5.12. 10G-R Characteristics

Table 38. 10G-R Differential Transmitter Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	-	97	-	ps	-
Output Differential Voltage	$V_{TX-DIFFp-p}$	400	-	900	mV	-
Total Jitter	T_J	-	-	0.28	UIpp	-
Transmitter output impedance on chip	R_{TX}	-	100	-	ohm	-

Table 39. 10G-R Differential Receiver Characteristics

Parameter	SYM	Min	Typ.	Max	Units	Notes
Unit Interval	UI	-	97	-	ps	-
Input Differential Voltage	$V_{RX-DIFFp-p}$	200	-	950	mV	-
Receiver input impedance on chip	R_{RX}	-	100	-	ohm	-

10.6. Power and Reset Characteristics

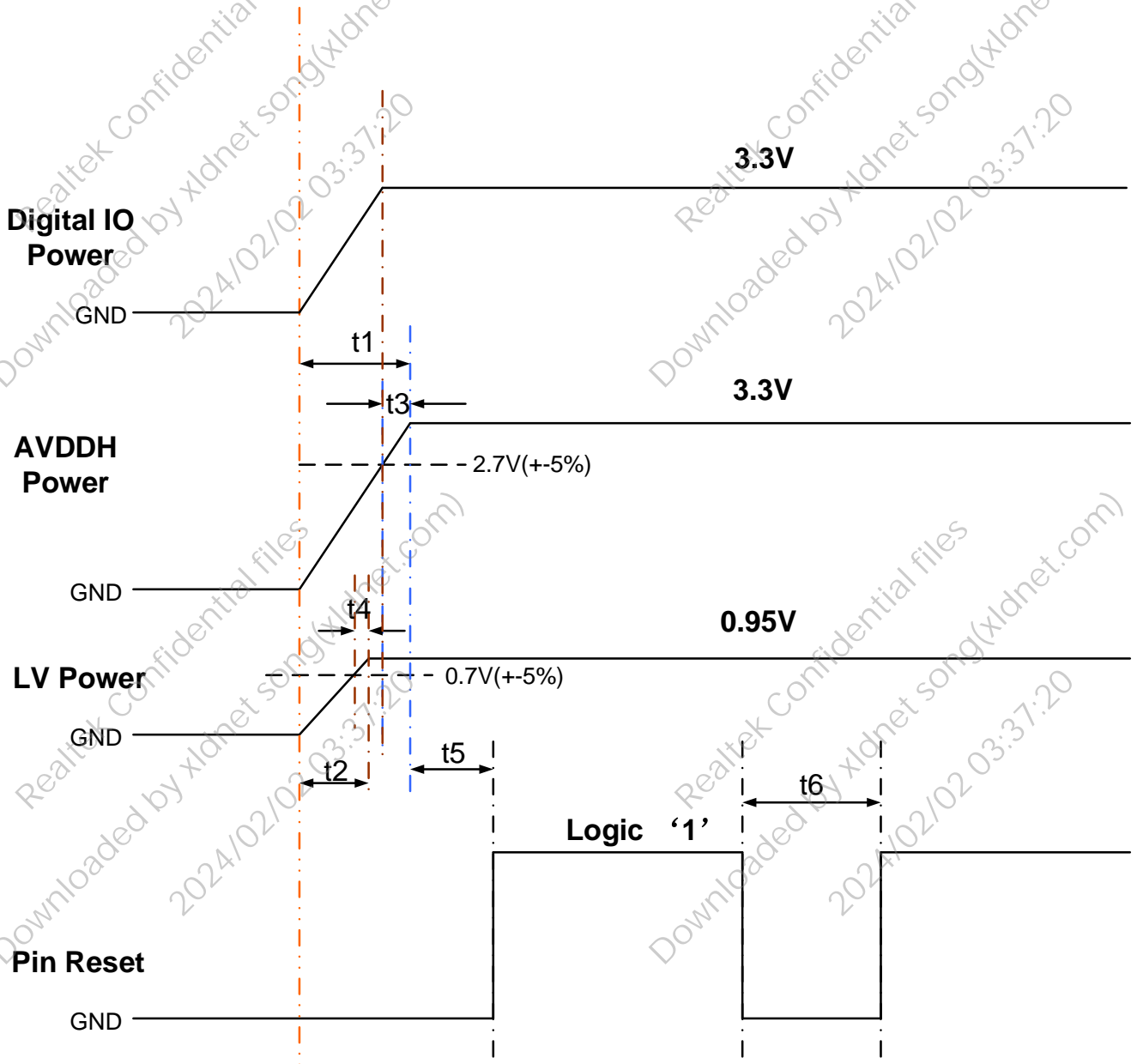


Figure 39. Power and Reset Characteristics

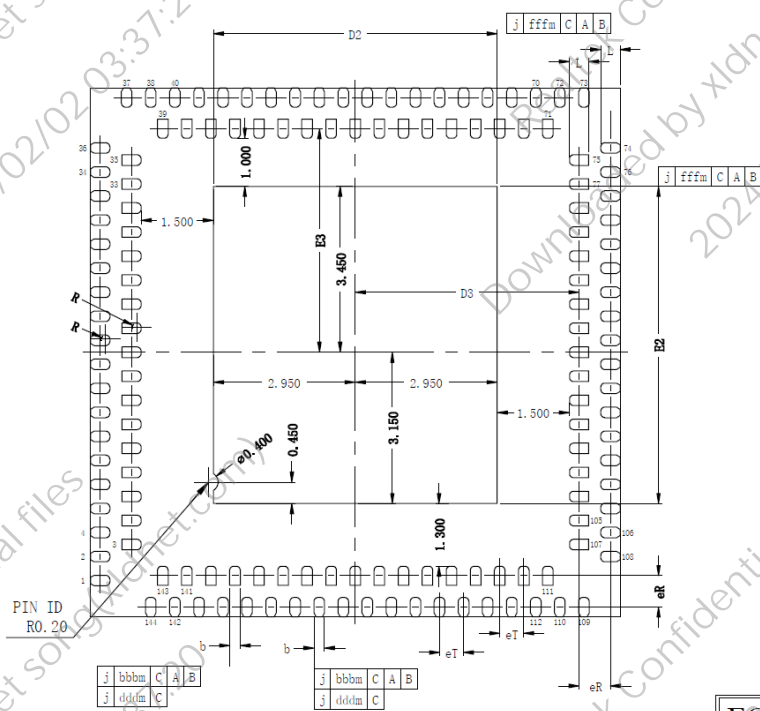
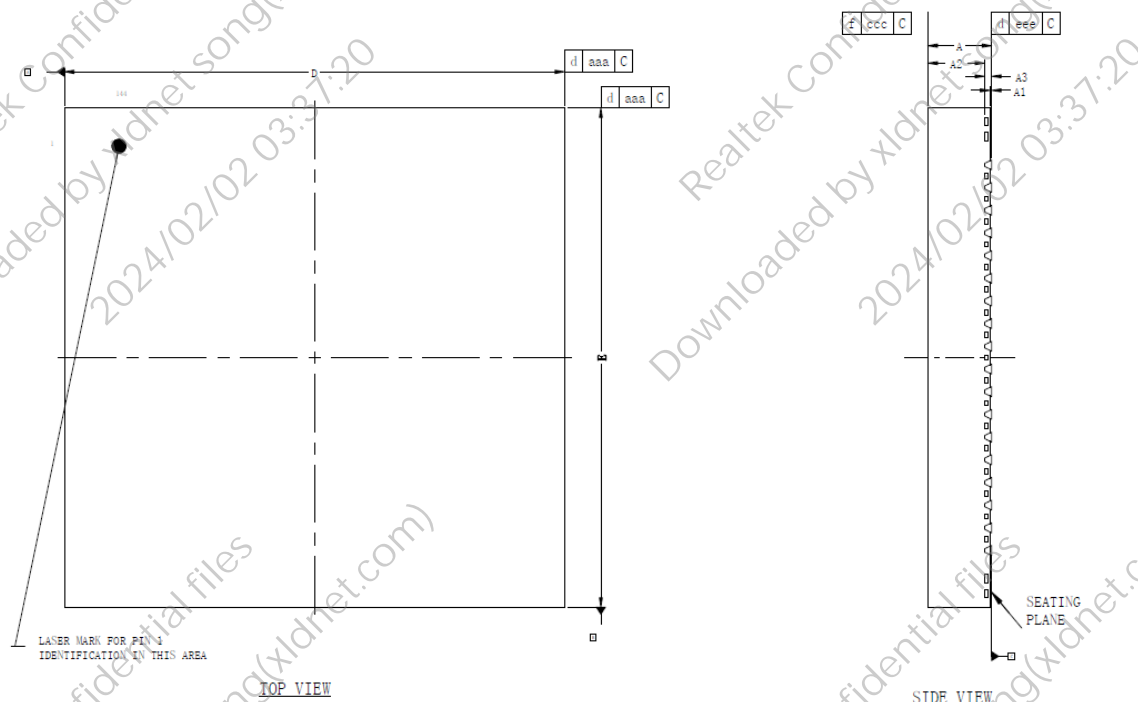
Table 40. Power and Reset Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typ.	Max	Units
AVDDH Power Rising Time	t1	AVDDH power rise settling time.	I	0.1	-	-	ms
LV Power Rising Time	t2	DVDDL and AVDDL power rise settling time.	I	0.1	-	-	ms
HV Power Ready Time after more than HV POR threshold	t3	The duration from HV power more than HV POR threshold to HV power ready.	I	-	-	10	ms
LV Power Ready Time after more than LV POR threshold	t4	The duration from LV power more than LV POR threshold to LV power ready.	I	-	-	10	ms
Reset Delay Time	t5	The duration from 'all power steady' to the reset signal released to high.	I	10.5	-	-	ms
Reset Low Time	t6	The duration of reset signal remaining low time before issuing a reset to RTL8372N.	I	10.5	-	-	ms

Note 1: The time point when the digital IO domain power is ready shall not be later than the latest ready one of AVDDH Power and LV Power

11. Mechanical Dimensions

Thermally Enhanced DOFU QFN 11x11mm² 144L Outline.



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.500	-	-	0.059
A1	0.000	-	0.050	0.000	-	0.002
A2	-	1.250	1.300	-	0.049	0.051
A3	0.152 REF.			0.006 REF.		
b	0.180	0.220	0.300	0.007	0.009	0.012
D	11 BSC			0.433 BSC		
D2	5.800	5.900	6.000	0.228	0.232	0.236
D3	4.550	4.650	4.750	0.179	0.183	0.187
E	11 BSC			0.433 BSC		
E2	6.500	6.600	6.700	0.256	0.260	0.264
E3	4.550	4.650	4.750	0.179	0.183	0.187
L	0.300	0.400	0.500	0.012	0.016	0.020
eT	0.500 BSC			0.020 BSC		
eR	0.650 BSC			0.026 BSC		
R	0.090	-	-	0.004	-	-
TOLERANCES OF FORM AND POSITION						
aaa	0.150			0.006		
bbb	0.100			0.004		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm)

Note 2: REFERENCE DOCUMENT: JEDEC MO-220

12. Ordering Information

Table 41. Ordering Information

Part Number	Package
RTL8372N-CG	DOFU QFN 11 x 11mm ² 144L 'Green' Package

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