1. DESCRIPTION

The XAPE4259 RF switch is designed tocover a broad range of applications from 10 MHzthrough 3000 MHz. This reflective switch integrateson-board CMOS control logic with a low voltageCMOS-compatible control interface, and can becontrolled using either single-pin or complementarycontrol inputs. Using a nominal +3-volt power supplyvoltage, a typical input 1dB compression point of +32.5 dBm can be achieved.

2. FEATURES

- Single-pin or complementary CMOSlogic control inputs
- Low insertion loss:
  - 0.35 dB @ 1000 MHz
  - 0.5 dB @ 2000 MHz
- Isolation of 30 dB @ 1000 MHz
- High ESD tolerance of 2 kV HBM
- Typical input 1 dB compression pointof +32.5 dBm
- 1.8V minimum power supply voltage

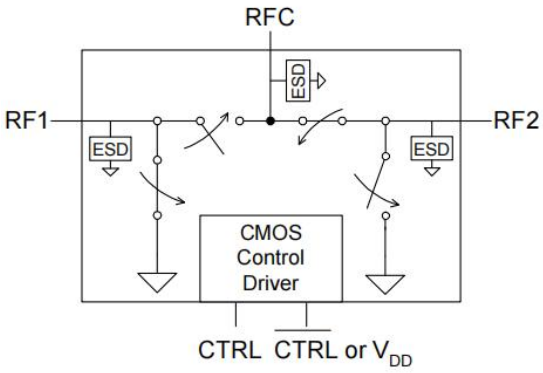


Figure 1.Functional Diagram

Table 1.Electrical Specifications @ +25 °C,V_{DD} = 3V (Z_S = Z_L = 50Ω)

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operation frequency[1]		10		3000	MHz
Insertion loss[3]	1000 MHz 2000 MHz		0.35 0.50	0.45 0.60	dB dB
Isolation	1000 MHz 2000 MHz	29 19			dB dB
Return loss[3]	1000 MHz 2000 MHz	21 24	22 27		dB dB
'ON' switching time	50% CTRL to 0.1 dB of final value, 1 GHz		1.50		us
'OFF' switching time	50% CTRL to 25 dB isolation, 1 GHz		1.50		us
Video feedthrough[2]			15		mVpp
Input 1dB compression point	1000 MHz @ 2.3–3.3V 1000 MHz @ 1.8–2.3V 2500 MHz @ 2.3–3.3V 2500 MHz @ 1.8–2.3V	31.5 29.5 28.5 28	32.5 30.5 30.5 29		dBm dBm dBm dBm
Input IP3	1000 MHz, 20 dBm input power		55		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.
2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.
3. A tuning capacitor must be added to the application board to optimize the insertion loss and return loss performance. See Figure 6 for details

3. PIN CONFIGURATIONS AND FUNCTIONS

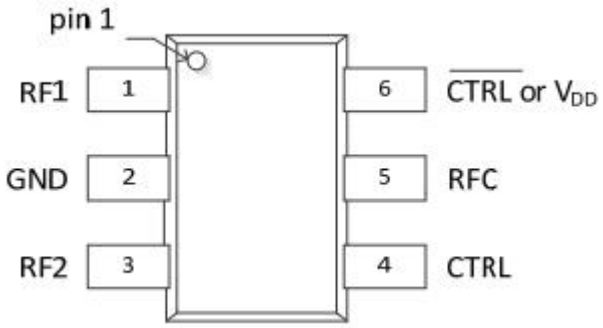


Figure 2. Pin Configuration (Top View)

Table 2. Pin Functions

Pin No.	PIN Name	Description
1	RF1	RF port 1.
2	GND	Ground connection. Traces should bephysically short and connected to groundplane for best performance.
3	RF2	RF port 2.
4	CTRL	Switch control input, CMOS logic level.
5	RFC	RF common.
6	$\overline{CTRL}$ or V_{DD}	This pin supports two interface options:Single-pin control mode. A nominal 3-volt supply connection is required. Complementary-pin control mode. Acomplementary CMOS control signal toCTRL is supplied to this pin. Bypassingon this pin is not required in this mode.

Note:* All RF pins must be DC blocked with an external series capacitor or held at O VDC.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Power supply voltage	1.8	3.0	3.3	V
I_{DD} Power supply current (V_{DD} = 3V, V_{CNTL} = 3V)		9	20	μA
Control voltage high	0.7× V_{DD}			V
Control voltage low			0.3× V_{DD}	V

4. Switching Frequency

The XAPE4259 has a maximum 25 kHz switching rate.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+0.3	V
T_{ST}	Storage temperature range	-65	150	℃
T_{OP}	Operating temperature range	-40	85	℃
P_{IN}	Input power (50Ω)		+34*	dBm
V_{ESD}	ESD Voltage (HBM,ML_STD 883 Method 3015.7)		2000	V
	ESD Voltage (MM,JEDEC, JESD22-A114-B)		100	V

Note*:To maintain optimum device performance, do not exceed Max Pn at desired operating frequency (see Figure 4).

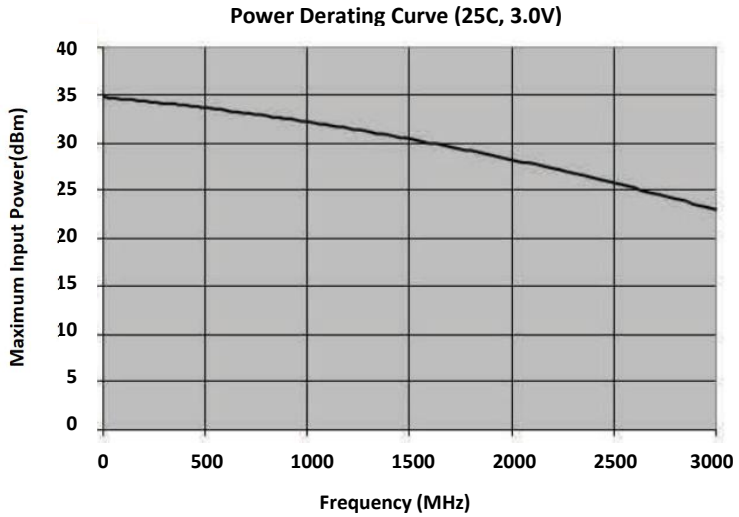


Figure 3.Maximum Input Power

5. Latch-Up Avoidance

Unlike conventional CMOS devices, Soi+Cmos devices are immune to latch-up.

6. Electrostatic Discharge (ESD) Precautions

When handling this **Soi+Cmos** device, observe thesame precautions that you would use with other ESD-sensitive devices. Although this device containscircuitry to protect it from damage due to ESD,precautions should be taken to avoid exceeding thespecified rating.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 ($\overline{CTRL}$ or VoD)= Low Pin 4 (CTRL) = High	RFC to RF1
Pin 6 ($\overline{CTRL}$ or VoD) = High Pin 4 (CTRL) = Low	RFC to RF2

7. Thermal Data

- Psi-JT (Ψ_{JT}), junction top-of-package, is a thermalmetric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).
- Ψ_{JT} = (TJ -TT)/P
- Where
- Ψ_{JT} = junction-to-top of package characterization parameter, °C/W
- T_J = die junction temperature, °C
- T_T = package temperature (top surface, in thecenter), °C
- P = power dissipated by device, Watts

Table 7.Thermal Data

Parameter	Typ	Unit
Maximum junction temperature, T_{JMAX} (RF input power, CW = 31.5 dBm, +85 °C ambient)	99	°C
Ψ_{JT}	37	°C/W
θ_{JA},junction-to-ambient thermal resistance	104	°C/W

8. EVALUATION KIT

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's XAPE4259. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5.

This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. he board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device V_{DD} or $\overline{CTRL}$ input. J7-1 is connected to the device CTRL input.

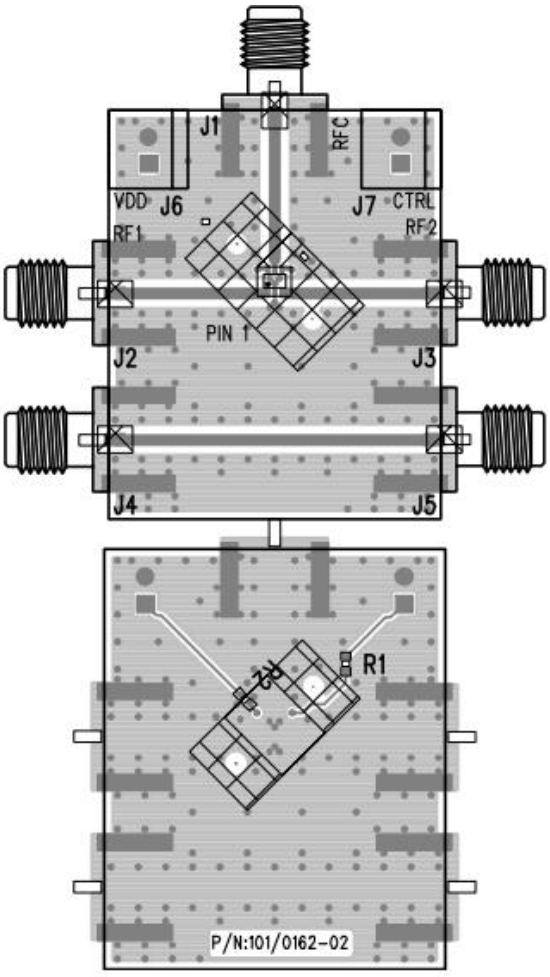
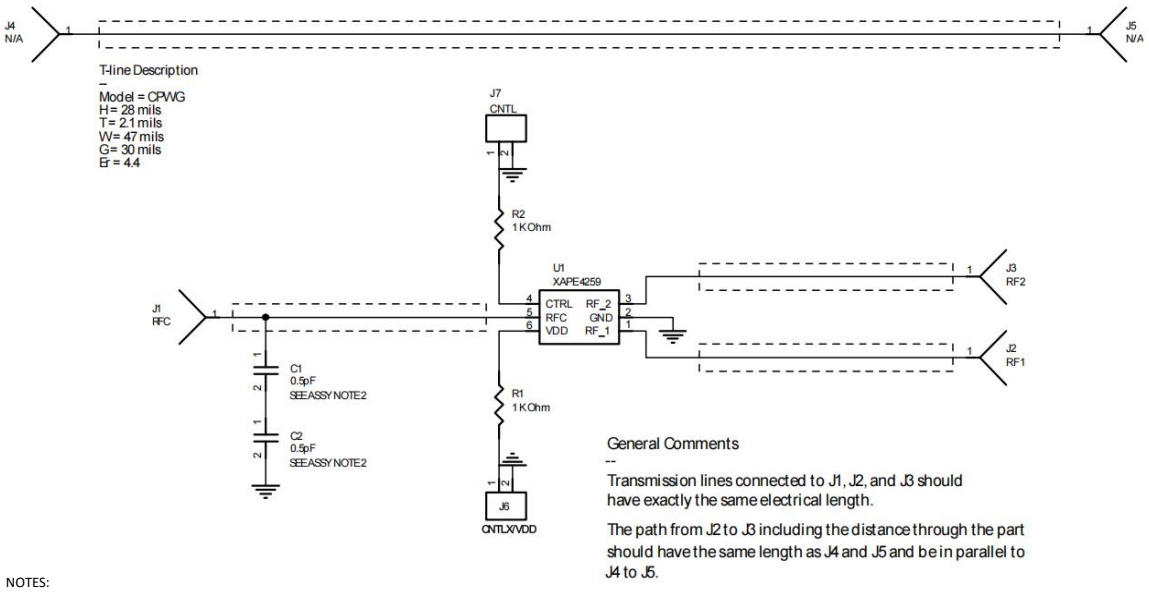


Figure 5. Evaluation Board Layout



NOTES:

1. ADD TWO 0.5PF CAPS IN SERIES TO BE SHUNTED ON THE J1 SMA INPUT
   SOLDER C1 SIDE 1 TO THE RF TRACE CLOSE TO THE J1 PIN.
   SOLDER C1 SIDE 2 TO C2 SIDE 1.
   SOLDER C2 SIDE 2 TO GROUND.

Figure 6. Evaluation Board Schematic

9. TYPICAL PERFORMANCE DATA @-40°C to 85°C (Unless Otherwise Noted)

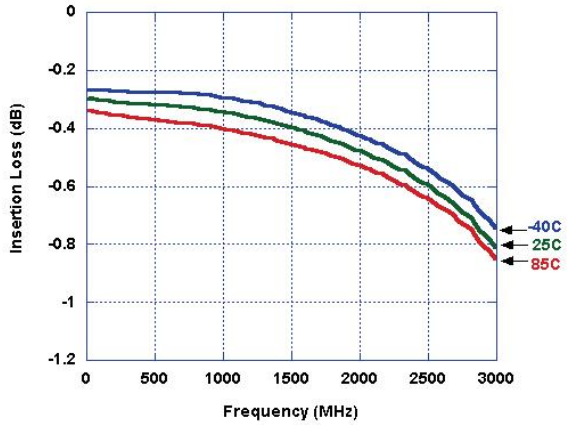


Figure 7. Insertion Loss

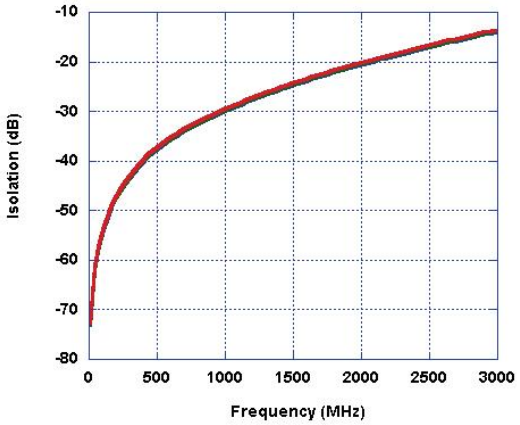


Figure 8. Isolation – Input to Output

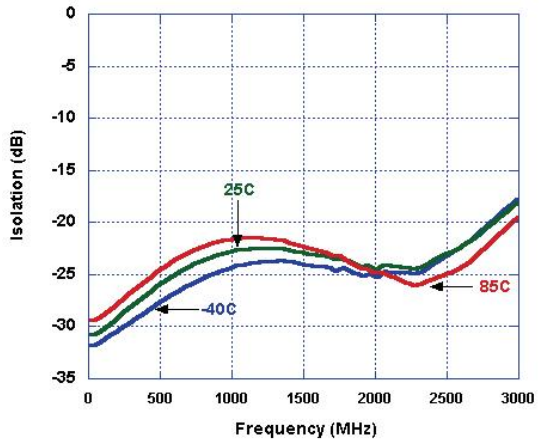


Figure 9. Isolation – Output to Output

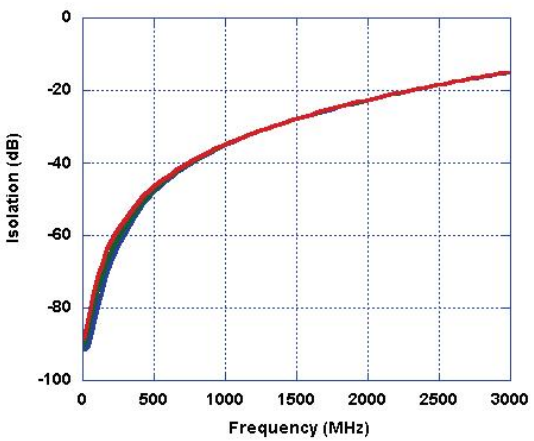


Figure 10. Return Loss (Input)

Typical Performance Data @ VDD = 2.3V, T = 25 °C

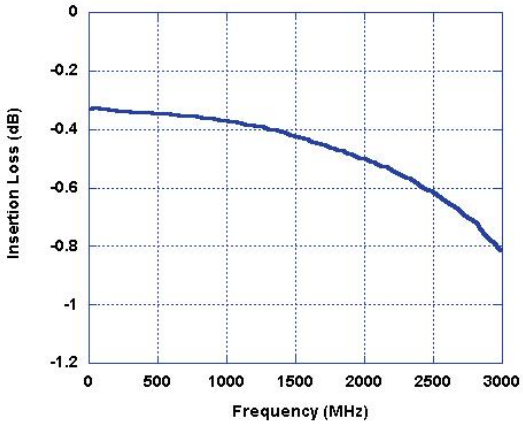


Figure 11. Insertion Loss

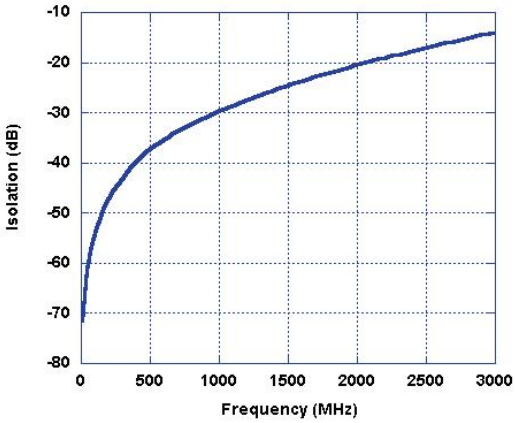


Figure 12. Isolation – Input to Output

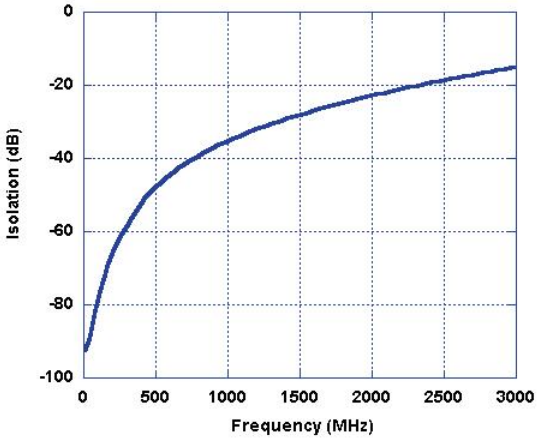


Figure 13. Isolation – Output to Output

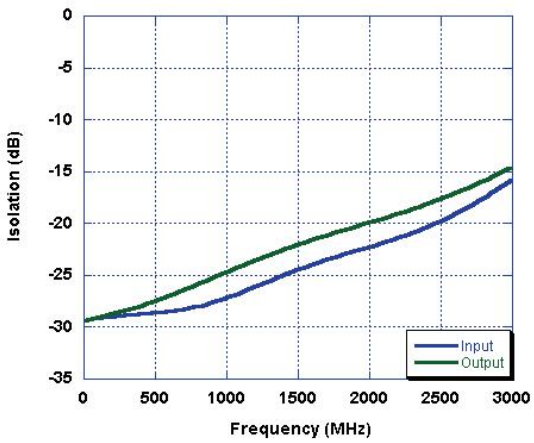


Figure 14. Return Loss (Input and Output)

10.ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XAPE4259-S63	。259	SOT363	2.10*1.22	-40 to +85	MSL3	T&R	3000

11.DIMENSIONAL DRAWINGS