



Descriptions

The NE5532DR is a dual operational amplifier IC designed for improved tone control and is well suited for audio applications. Its noise-free, high gain bandwidth, high output current, and low distortion ratio make it suitable not only for acoustic electronic components of audio preamplifiers and active filters, but also for industrial measurement tools. It is also suitable for headphone amplifiers with high output currents, and can be applied to general purpose portable integrated power amplifiers to appropriately bias input low voltage sources in low voltage single supply applications.

Feature

- Operating voltage($\pm 2V \sim \pm 18V$)
- Low input noise voltage (Typical value $0.8\mu V_{rms}$)
- Wide gain bandwidth product (Typical value $15MHz$)
- Low distortion (Typical value 0.0005%)
- Rate of conversion (Typical value $5V/\mu s$)
- Bipolar technique

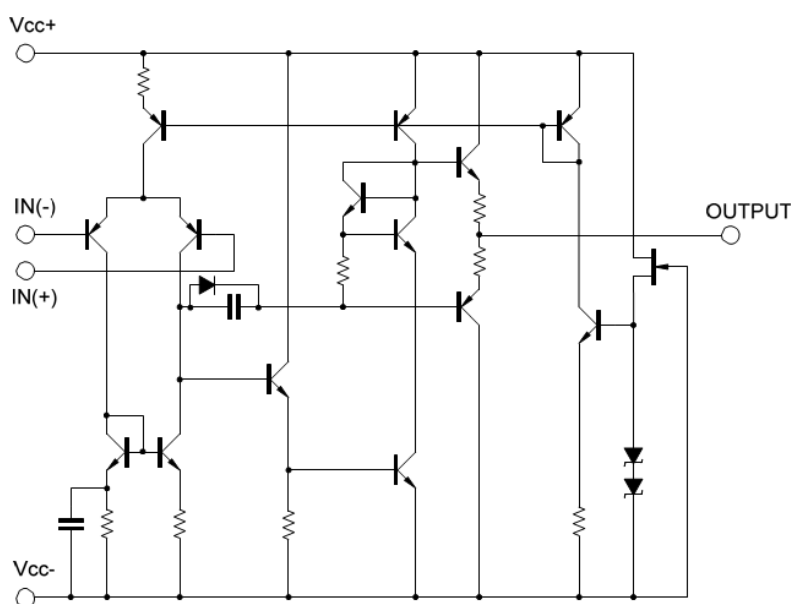
Applications

- Audio Preamplifiers
- Active Filters
- Headphone Amplifiers
- Industrial Measurement Equipment

Ordering Information

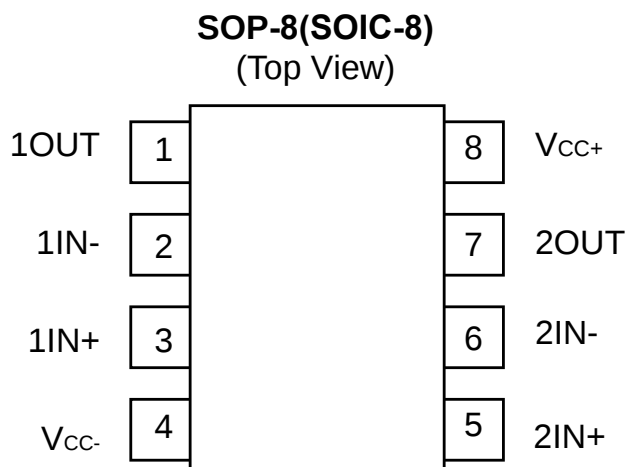
Product Model	Package Type	Packing	Packing Qty
NE5532DR	SOP-8(SOIC-8)	Tape	4000Pcs/Reel

Internal Block Diagram (1/2)





Pin Configurations



Pin Description

Pin	Symbol	I/O	Pin Description
1	1OUT	O	Output
2	1IN-	I	Inverting input
3	1IN+	I	Noninverting input
4	V _{CC-}	—	Negative supply
5	2IN+	I	Noninverting input
6	2IN-	I	Inverting input
7	2OUT	O	Output
8	V _{CC+}	—	Positive supply



Absolute Maximum Ratings

($T_A=25^{\circ}\text{C}$, not otherwise specified.)

Parameters	Symbol	Scope of scope	Unit of work
Supply voltage	V_{CC+}/V_{CC-}	± 18	V
Input voltage	V_{in}	± 15	V
Differential input voltage	$V_{I(DIFF)}$	± 30	V
Current of output	I_{OUT}	± 50	mA
Power consumption		440	mW
Temperature of junction	T_J	125	$^{\circ}\text{C}$
Operating temperature	T_{OPR}	$-40 \sim +85$	$^{\circ}\text{C}$
Temperature of storage	T_{STG}	$-40 \sim +125$	$^{\circ}\text{C}$

Note: Exceeding the limit parameters listed may lead to permanent damage inside the chip, and long-term operation under the limit conditions will affect the reliability of the chip.

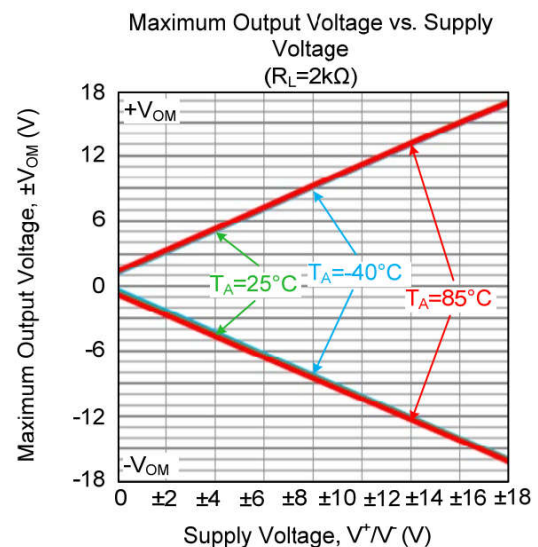
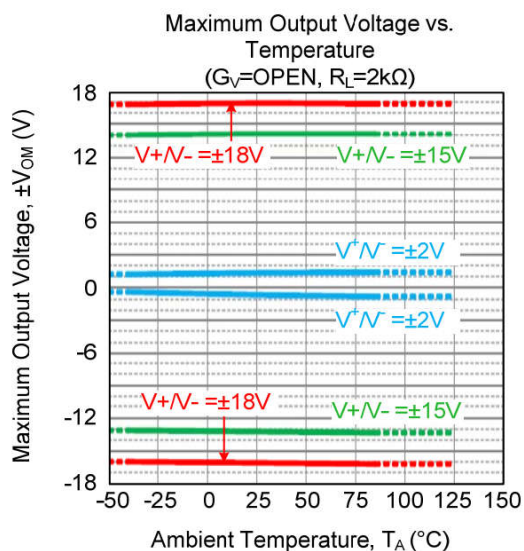
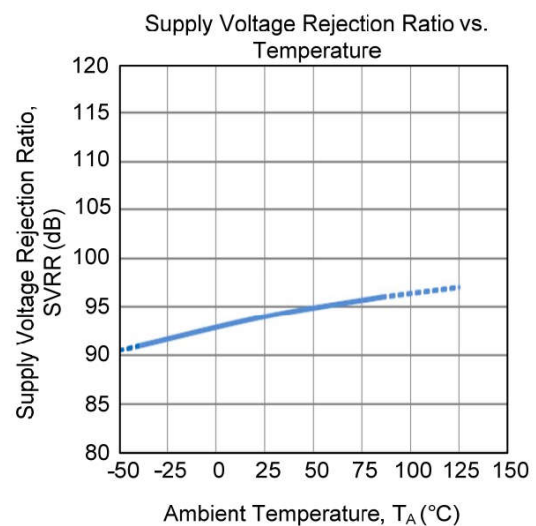
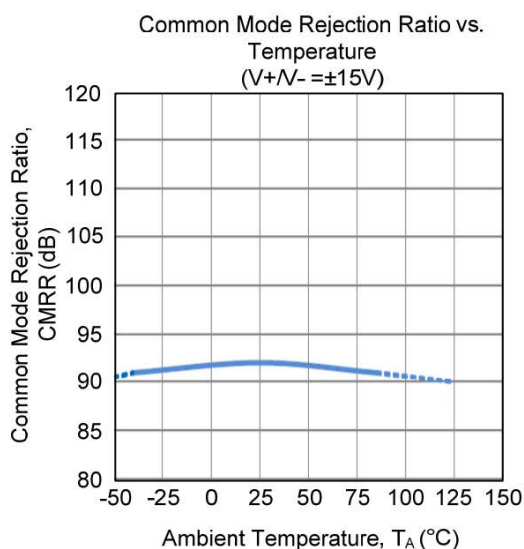
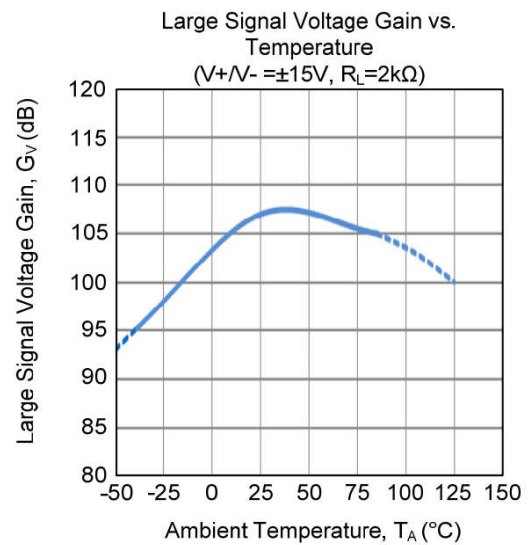
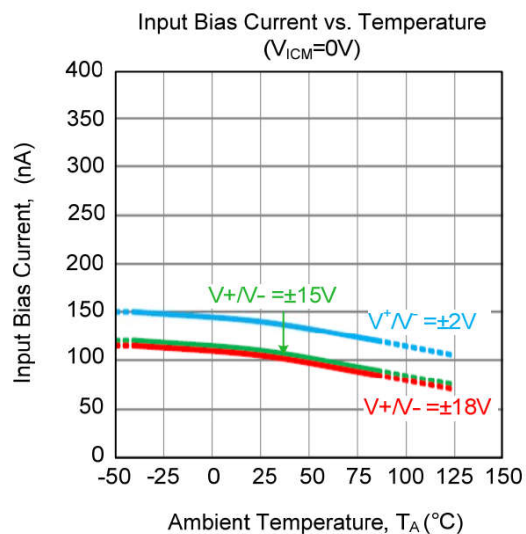
DC Electrical Characteristics

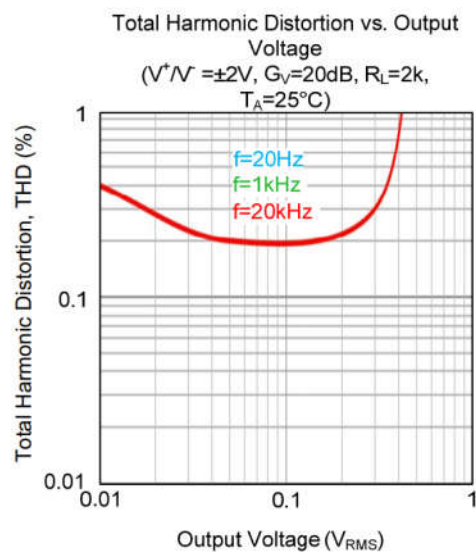
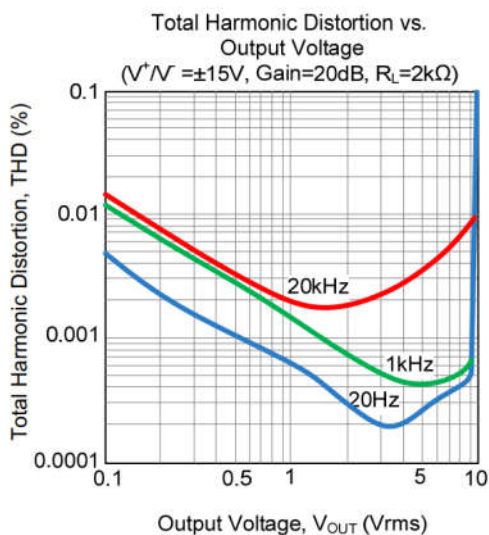
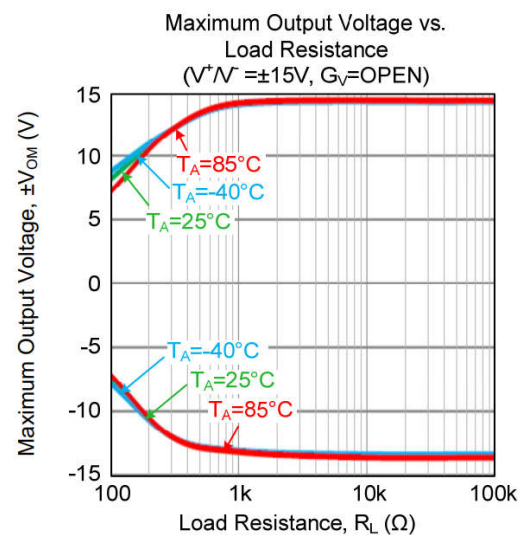
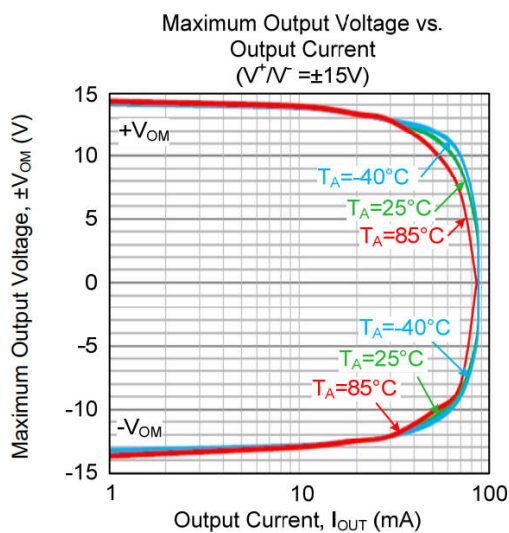
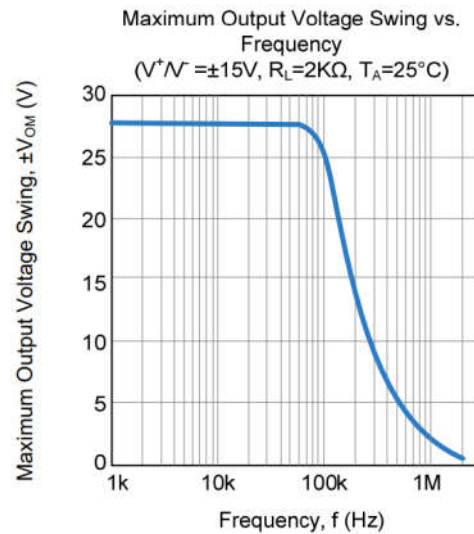
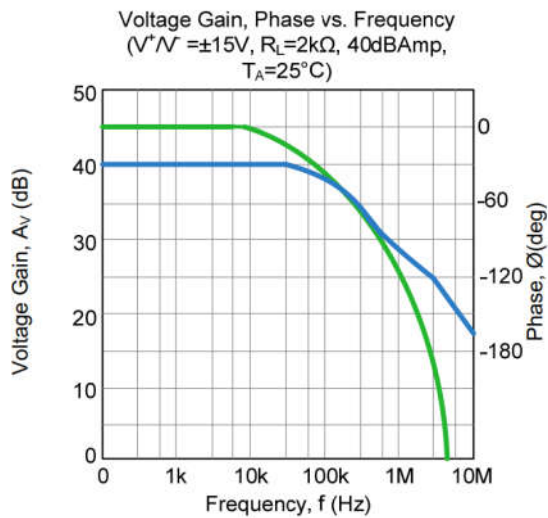
($V_{+}/V_{-}=\pm 15\text{V}$, $T_A=25^{\circ}\text{C}$, Unless otherwise stated.)

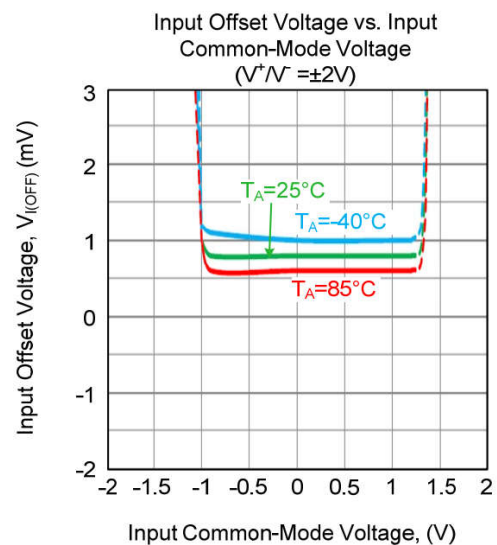
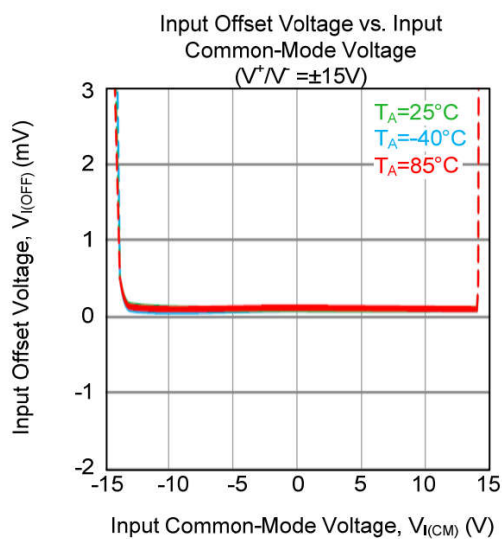
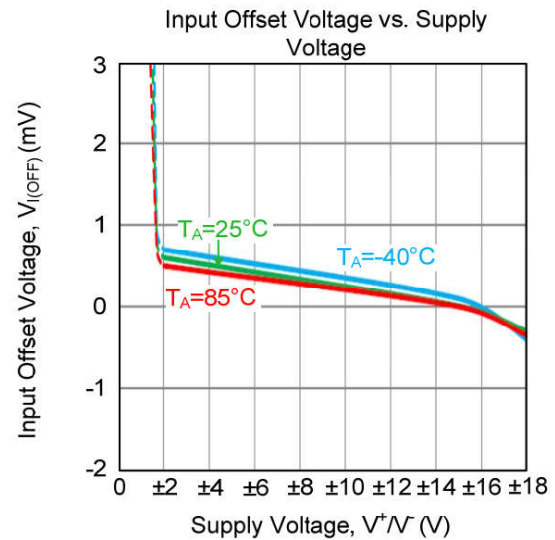
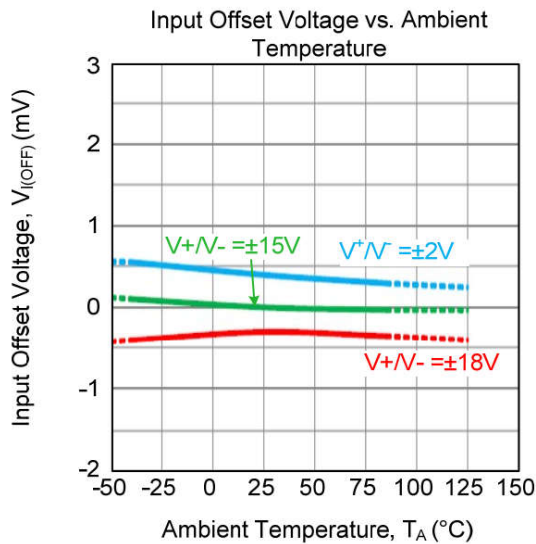
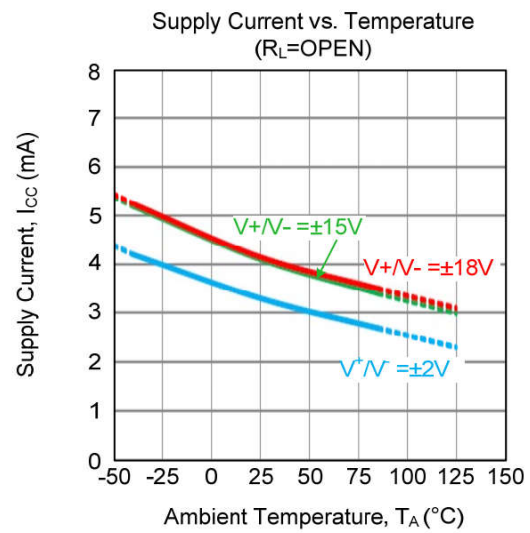
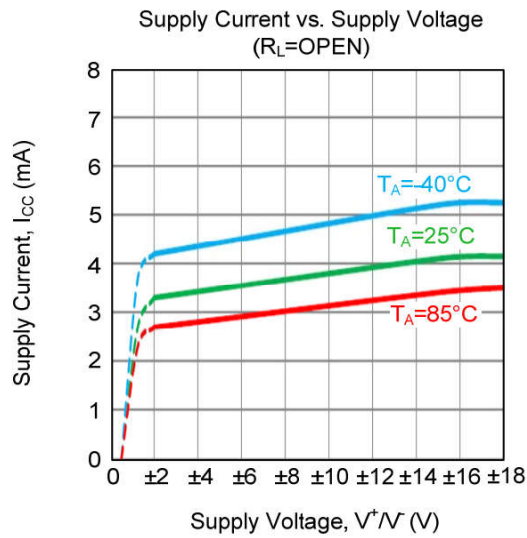
Parameters	Symbol	Condition of test	Min	Typ	Max	Unit
Input bias voltage	$V_{I(OFF)}$	$R_S \leq 10\text{k}\Omega$		0.5	3	mV
Input bias voltage	$I_{I(OFF)}$			5	200	nA
Input bias current	$I_{I(BIAS)}$			100	500	nA
Large signal voltage gain	G_v	$V_{OUT}=\pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	90	110		dB
Output voltage swing	V_{OM}	$R_L \geq 2\text{k}\Omega$	± 12	± 13.5		V
Input the common mode voltage	$V_{I(CM)}$		± 12	± 13.5		V
Common mode inhibition ratio	CMRR	$R_S \leq 10\text{k}\Omega$	80	110		dB
Supply voltage rejection ratio	SVR	$R_S \leq 10\text{k}\Omega$	80	110		dB
Current of operation	I_{CC}			6	9	mA
Rate of conversion	SR	$R_L \geq 2\text{k}\Omega$		5		V/ μs
Gain bandwidth product	GB	$f=10\text{KHz}$		15		MHz
Total harmonic distortion	THD	$G_v=20\text{dB}$, $V_{OUT}=5\text{V}$, $R_L=2\text{k}\Omega$, $f=1\text{KHz}$		0.0005		%
Input noise voltage	eN	$R_{IAA} R_S=2.2\text{ k}\Omega$, 30kHz LPF		0.8		μVrms

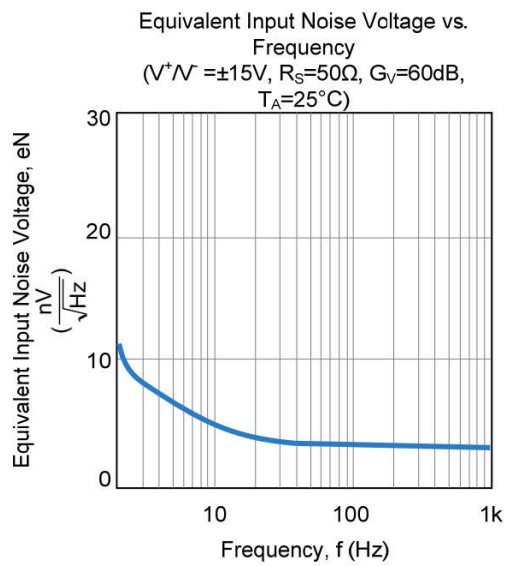
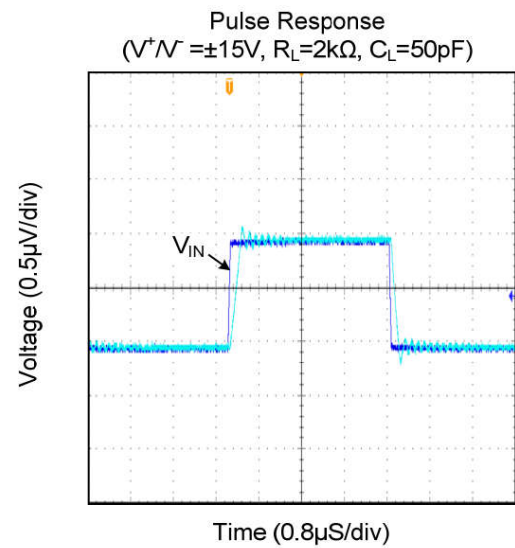
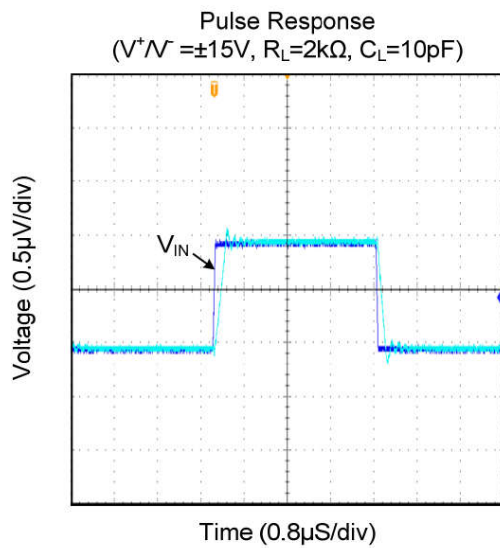


Typical characteristics





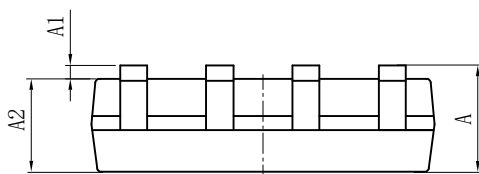
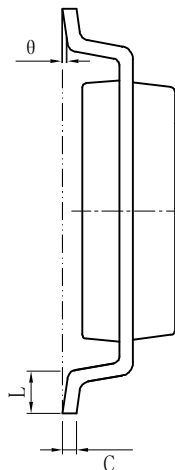
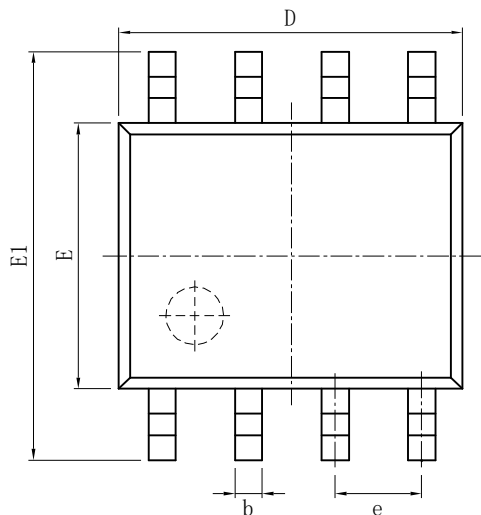






Package Information

SOP-8(SOIC-8)



Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°



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