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FM25Q256I3

256M-BIT SERIAL FLASH MEMORY

Datasheet

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Trademarks

1. Description

The FM25Q256I3 is a 256M-bit (32,768K-byte) Serial Flash memory, operating in wide voltage range. The FM25Q256I3 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O as well as 2-clock instruction cycle Quad Peripheral Interface (QPI).

The FM25Q256I3 can be programmed 1 to 256 bytes at a time, using the Page Program instruction. It is designed to allow either single Sector/Block at a time or full chip erase operation. The FM25Q256I3 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

2. Features

- **256Mbit of Flash memory**
  - 8192 uniform sectors with 4K-byte each
  - 512 uniform blocks with 64K-byte each or
  - 1024 uniform blocks with 32K-byte each
  - 256 bytes per programmable page
- **Serial Interface**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ0, DQ1, WP#
  - Quad SPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - QPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - DTR (Double Transfer Rate) Read
  - Continuous READ mode support
  - Program / Erase Suspend and Resume support
  - Allow true XIP (execute in place) operation
- **High Performance**
  - Max FAST_READ clock frequency: 100MHz
  - Max DTR_FAST_READ clock frequency: 50MHz
  - Max READ clock frequency: 50MHz
  - Typical page program time: 0.7ms
  - Typical sector erase time: 45ms
  - Typical block erase time: 200/250ms
  - Typical chip erase time: 90s
- **Supply Voltage: 2.7V to 3.6V**
- **Industrial Temperature Rage**
- **Flexible Architecture with 4KB Sectors**
  - Uniform Sector Erase(4K-bytes)
  - Uniform Block Erase(32K and 64K-bytes)
  - Program 1 to 256 bytes per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and hardware write protection
  - Top/Bottom, 64KB complement array protection
  - Power Supply Lock-Down and OTP protection
  - Individual Block/Sector array protection
  - Lockable 4X256-Byte OTP Security Register
  - Discoverable Parameters (SFDP) Register
  - 64-Bit Unique ID for each device
  - Volatile & Non-volatile Status Register Bits
- **Green Package**
  - 8-pin SOP 208-mil
  - 16-pin SOP 300-mil
  - 8-pad TDFN 6x5-mm
  - 8-pad TDFN 8x6-mm
  - 24-ball TFBGA 8x6-mm
  - All Packages are RoHS Compliant and Halogen-free

3. Packaging Type And Pin Configurations

FM25Q256I3 is offered in an 8-pin SOP8 208-mil，a 16-pin SOP16 300-mil，an 8-pad TDFN 6x5-mm，an 8-pad TDFN 8x6-mm and a 24-ball TFBGA 8x6-mm packages as shown in Figure 1-4 respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1. Pin Configuration SOP16 300-mil

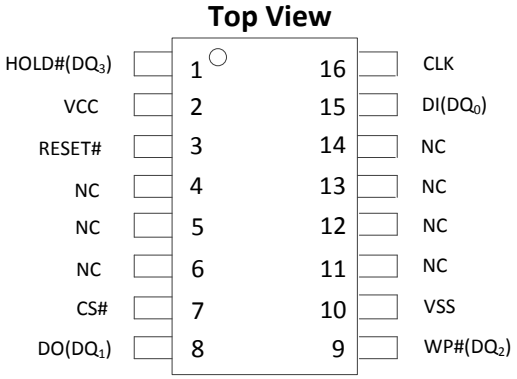


Figure 1 16-pin SOP(300mil)

3.2. Pin Description SOP16 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	HOLD#/RESET# (DQ3)	I/O	Hold Input (Data Input Output 3)(2)
2	VCC		Power Supply
3	RESET#	I	Reset Input
4	NC		No Connect
5	NC		No Connect
6	NC		No Connect
7	CS#	I	Chip Select Input
8	DO (DQ1)	I/O	Data Output (Data Input Output 1)(1)
9	WP# (DQ2)	I/O	Write Protect Input (Data Input Output 2)(2)
10	VSS		Ground
11	NC		No Connect
12	NC		No Connect
13	NC		No Connect
14	NC		No Connect
15	DI (DQ0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Note:

1 DQ0 and DQ1 are used for Dual SPI instructions.

2 DQ0 – DQ3 are used for Quad SPI and QPI instructions

3 WP#(DQ2), HOLD# (DQ3) will remain internal pull up function while this pin is not physically connected in system confguration. However, the internal pull up function will be disabled if the system has physical connection to WP#(DQ2) or HOLD#(DQ3).

3.3. Pin Configuration TDFN 6x5-mm and TDFN 8x6-mm

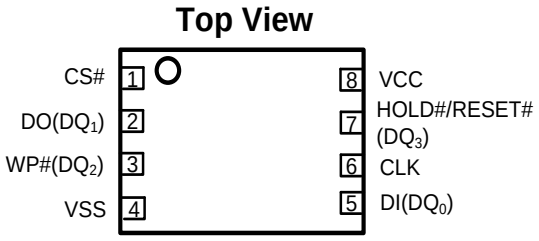


Figure 2 TDFN 6x5-mm

3.4. Pin Description TDFN 6x5-mm and TDFN 8x6-mm

PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO (DQ1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS		Ground
5	DI (DQ0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD#/RESET# (DQ3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Note:

1 DQ0 and DQ1 are used for Dual SPI instructions.

2 DQ0 – DQ3 are used for Quad SPI and QPI instructions

3 WP#(DQ2), HOLD#/RESET#(DQ3) will remain internal pull up function while this pin is not physically connected in system confguration. However, the internal pull up function will be disabled if the system has physical connection to WP#(DQ2) or HOLD#/RESET#(DQ3).

3.5. Ball Configuration TFBGA 8x6-mm (6x4 Ball Array)

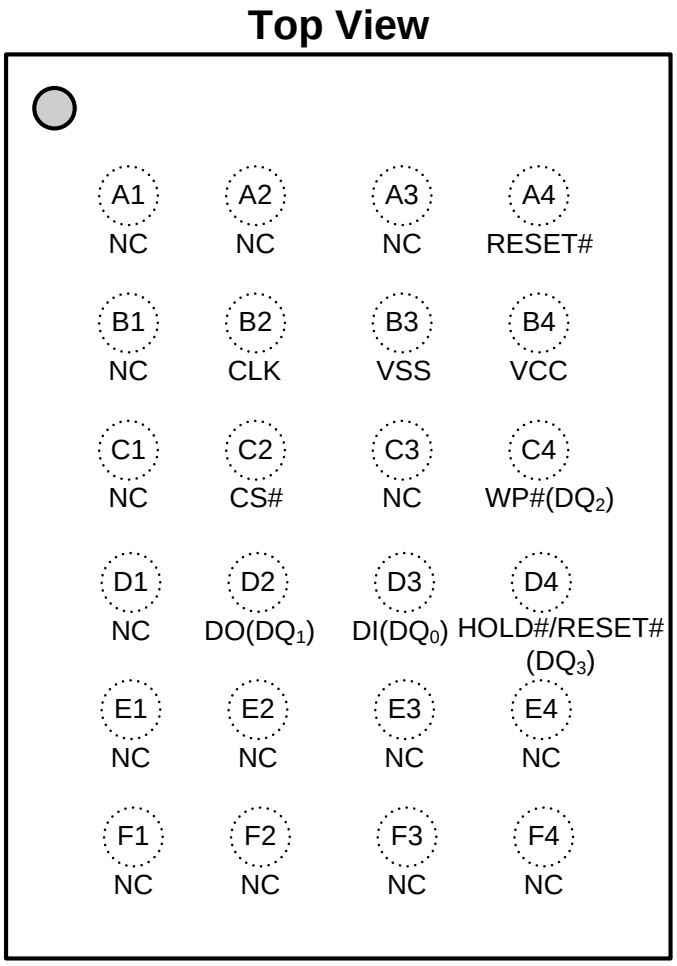


Figure 3 24-ball TFBGA 8x6-mm

3.6. Ball Configuration TFBGA 8x6-mm (6x4 Ball Array)

BALL NO.	PIN NAME	I/O	FUNCTION
A4	RESET#	I	Reset Input
B2	CLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
C2	CS#	I	Chip Select Input
C4	WP# (DQ2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (DQ1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (DQ0)	I/O	Data Input (Data Input Output 0)(1)
D4	HOLD# (DQ3)	I/O	Hold Input (Data Input Output 3)(2)

Note:

1 DQ0 and DQ1 are used for Dual SPI instructions.

2 DQ0 – DQ3 are used for Quad SPI and QPI instructions

3 WP#(DQ2), HOLD# (DQ3) will remain internal pull up function while this pin is not physically connected in system confguration. However, the internal pull up function will be disabled if the system has physical connection to WP#(DQ2) or HOLD#(DQ3).

3.7. Pin Configuration SOP8 208-mil

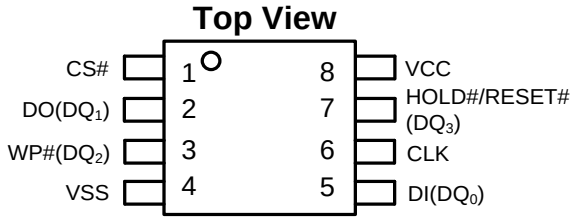


Figure 4 SOP8 208-mil

3.8. Pin Description SOP8 208-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO (DQ1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS		Ground
5	DI (DQ0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD#/RESET# (DQ3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Note:

1 DQ0 and DQ1 are used for Dual SPI instructions.

2 DQ0 – DQ3 are used for Quad SPI and QPI instructions

3 WP#(DQ2), HOLD#/RESET#(DQ3) will remain internal pull up function while this pin is not physically connected in system confguration. However, the internal pull up function will be disabled if the system has physical connection to WP#(DQ2) or HOLD#/RESET#(DQ3).

4. PIN DESCRIPTIONS

4.1. Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up (see "8 Write Protection" and Figure 122). If needed a pull-up resister on CS# can be used to accomplish this.

4.2. Serial Data Input, Output and I/Os (DI, DO and DQ0, DQ1, DQ2, DQ3)

The FM25Q256I3 supports standard SPI, Dual SPI, Quad SPI and QPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual/Quad SPI and QPI instructions use the bidirectional DQ pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the WP# pin becomes DQ_2 and HOLD# pin becomes DQ_3.

4.3. Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Registers from being written. The WP# pin is active low. However, when the QE bit of Status Register-2 is set for Quad I/O, the WP# pin function is not available since this pin is used for DQ2.

4.4. HOLD (HOLD#)

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the HOLD# pin function is not available since this pin is used for DQ_3.

4.5. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

4.6. Hardware Reset (RESET#)

The /RESET pin allows the device to be reset by the controller.

5. Block Diagram

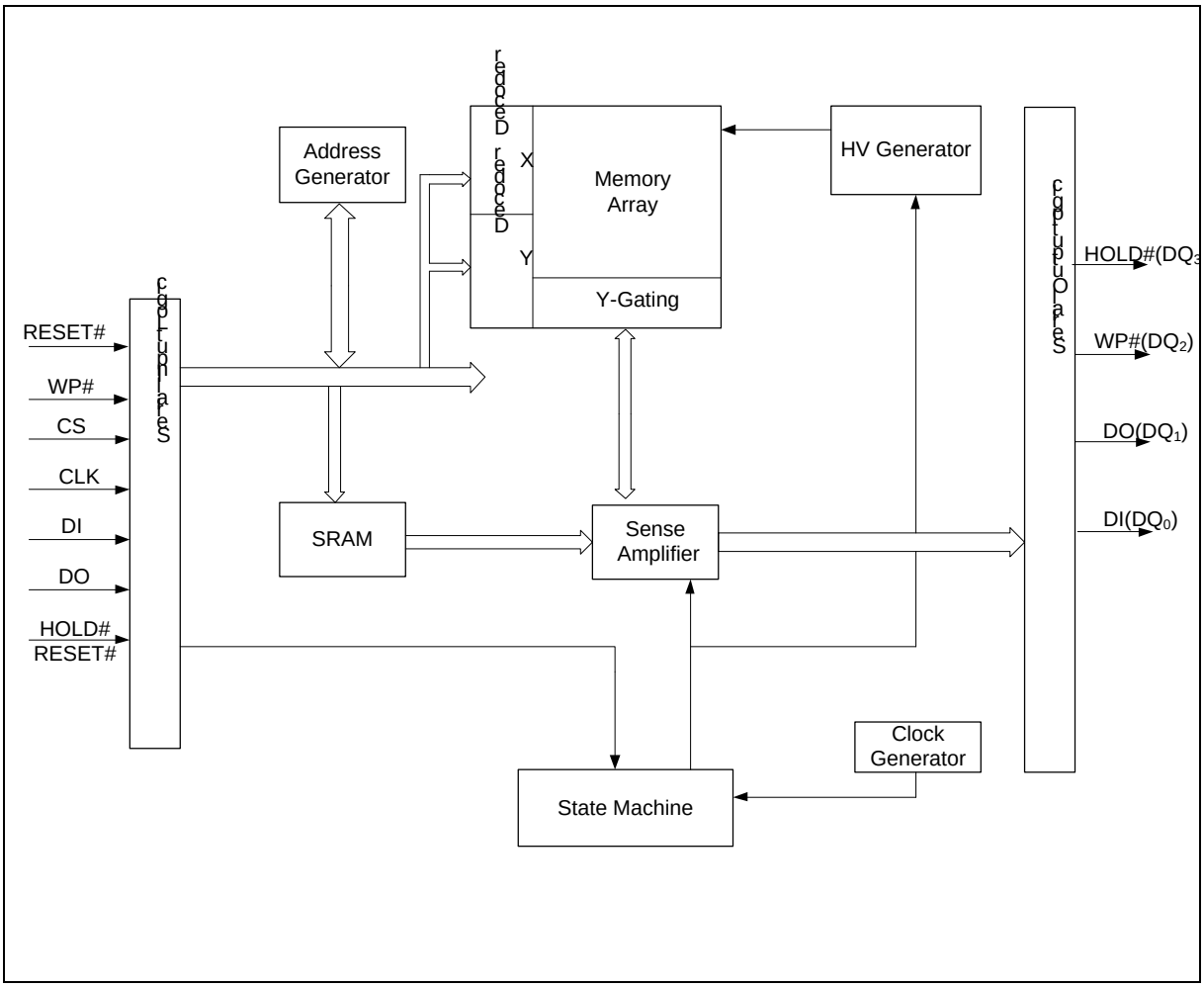


Figure 5 FM25Q256I3 Serial Flash Memory Block Diagram

6. Memory Organization

The FM25Q256I3 array is organized into 131,072 programmable pages of 256-bytes each. Up to 256 bytes can be programmed (bits are programmed from 1 to 0) at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The FM25Q256I3 has 8,192 erasable sectors, 1,024 erasable 32-k byte blocks and 512 erasable 64-k byte blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

Table 1 Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
511	1023 | 1022	8191	01FFF000h	01FFFFFFh
		…	…	…
		8176	01FF0000h	01FF0FFFh
.....	.....	.....	.....	.....
		.....	.....	.....
		.....	.....	.....
2	5 | 4	47	0002F000h	0002FFFFh
		…	…	…
		32	00020000h	00020FFFh
1	3 | 2	31	0001F000h	0001FFFFh
		…	…	…
		16	00010000h	00010FFFh
0	1 | 0	15	0000F000h	0000FFFFh
		…	…	…
		2	00002000h	00002FFFh
		1	00001000h	00001FFFh
		0	00000000h	00000FFFh

7. Device Operations

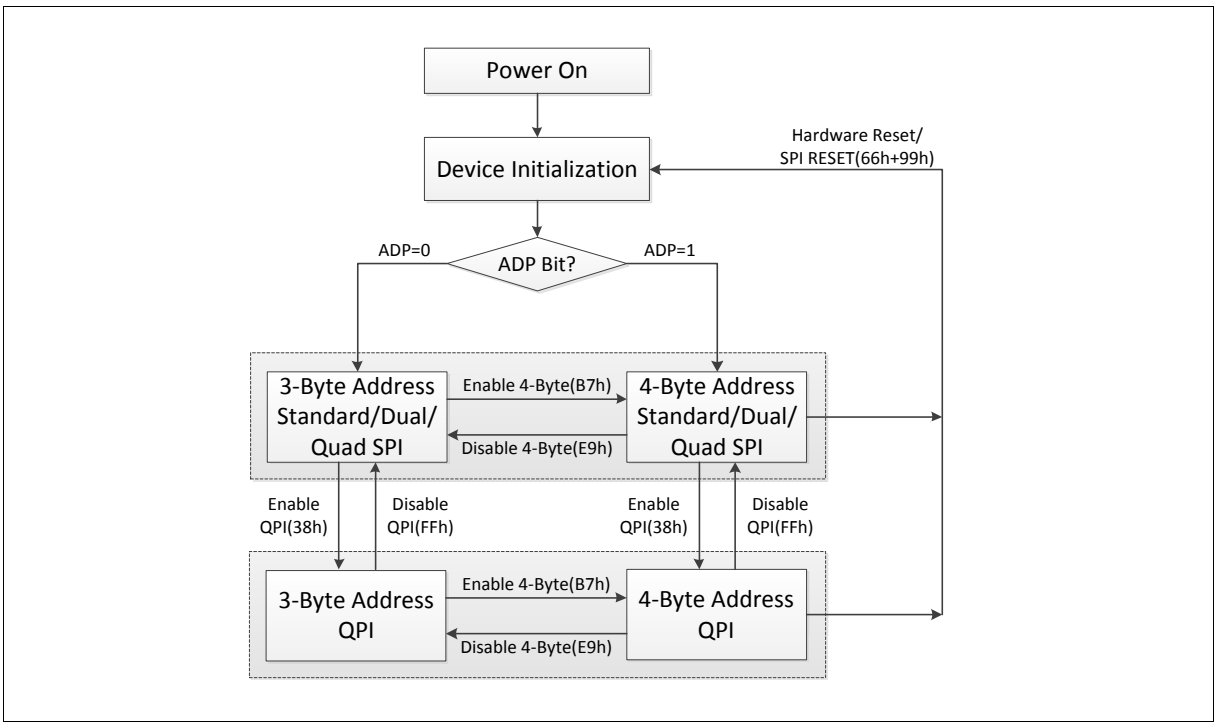


Figure 6 Operation Diagram

7.1. Standard SPI

The FM25Q256I3 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device. The DO output pin is used to read data or status from the device.

Commands, write instructions, addresses or data are latched on the rising edge of CLK, read data or status are available on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

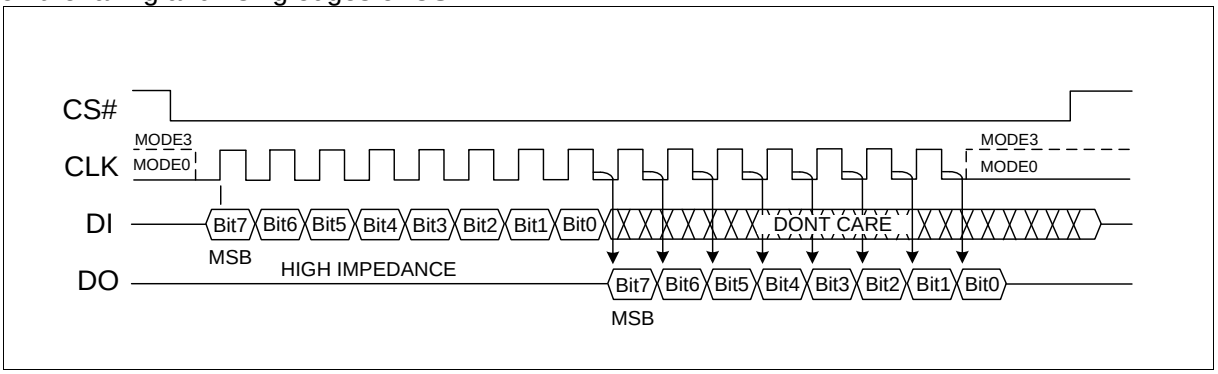


Figure 7 The difference between Mode 0 and Mode 3

7.2. Dual SPI

The FM25Q256I3 supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” , “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

7.3. Quad SPI

The FM25Q256I3 supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, “Word Read Quad I/O (E7h)”, “Octal Word Read Quad I/O (E3h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional DQ_0 and DQ_1 and the WP # and HOLD# pins become DQ_2 and DQ_3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

7.4. QPI

The FM25Q256I3 supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four DQ pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enable QPI (38h)” and “Disable QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction or hardware reset, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively. See Figure 6 for the device operation modes.

7.5. SPI/QPI DTR Read Instruction

The FM25Q256I3 supports multiple DTR (Double Transfer Rate) Read instructions that operate in Standard/Dual/Quad SPI and QPI modes to effectively improve the read operation throughput without increasing the serial clock frequency.. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

7.6. 3-Byte/4-Byte Address Modes

The FM25Q256I3 provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Modes is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256M-bit or more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the FM25Q256I3 can operate in either 3-Byte Address Mode or 4-Byte Address

Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; If ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0.

To switch between the 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

FM25Q256I3 also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless the device Address Mode setting. Please refer to Instruction Set Table for details.

7.7. Hold

For Standard SPI and Dual SPI operations, the HOLD# signal allows the FM25Q256I3 operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The HOLD# function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

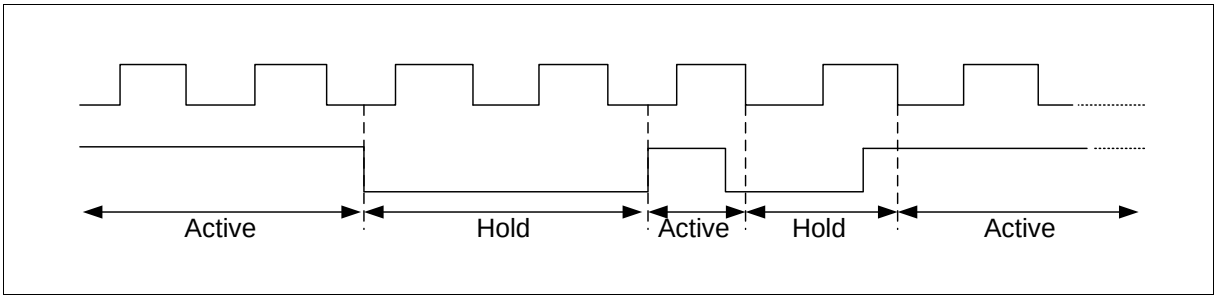


Figure 8 Hold Condition Waveform

7.8. Software Reset & Hardware Reset

The FM25Q256I3 can be reset to the initial power-on sate by a Software Reset sequence, either in SPI or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the commands sequence is successfully accepted, the device will take t_{RHSL} to reset. No command will be accepted during the reset period.

For the SOP8，TDFN-8 and TFBGA package types, FM25Q256I3 can also be configured to utilize a hardware RESET# pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for HOLD# pin function or RESET# pin function. When HOLD/RST=0 (factory default), the pin acts as a HOLD# pin as described above; when HOLD/RST=1, the pin acts as a RESET# pin. Drive the RESET# pin low for a minimum period of ~1us (t_{RLRH}) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While RESET# is low, the device will not accept any command input.

If QE bit is set to 1, the HOLD# or RESET# function will be disabled, the pin will become one of the four data I/O pins.

For 16-pin SOP & TFBGA package types, FM25Q256I3 provides a dedicated RESET# pin in addition to the HOLD# (DQ3) pin. Drive the RESET# pin low for a minimum period of ~1us (t_{RLRH}) will reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register will not affect the function of this dedicated RESET# pin.

Hardware RESET# pin has the highest priority among all the input signals. Drive RESET# low for a minimum period of ~1us (t_{RLRH}) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (CS#, CLK, DI, DO, WP# and/or HOLD#).

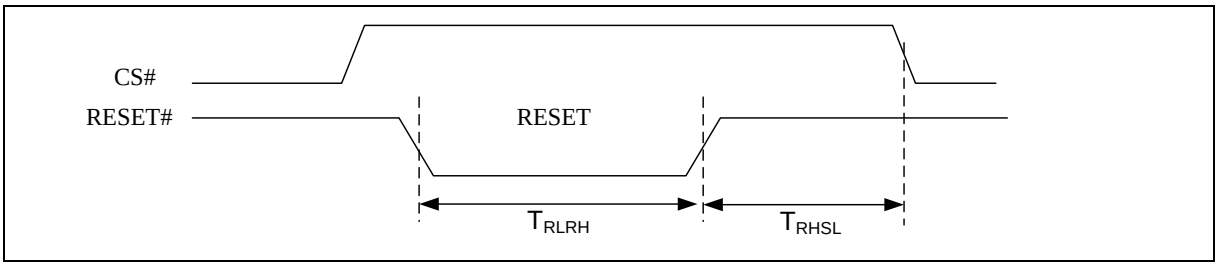


Figure 9 Hardware RESET Condition

Note:
1. While a faster RESET# pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum time is recommended to ensure reliable operation.
2. **Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when software/hardware reset is accepted by the device.** It is recommended to check the WIP bit and the SUS bit in Status Register before issuing the software reset command or hardware reset.

8. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the FM25Q256I3 provides several means to protect the data from inadvertent writes.

Write Protect Features

- Device resets when VCC is below threshold during WRITE operation
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Advanced Sector Protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write-protection for array and Security Sectors using Status Register.

At power-up and power-down, the device must not be selected; that is, CS# must follow the voltage applied on VCC until VCC reaches the correct values: V_{CC} (min) at power-up and Vss at power-down.

To avoid data corruption and inadvertent WRITE operations during power-up, a power-on reset circuit is included. The logic inside the device is held to RESET while VCC is less than the power-on reset threshold voltage of V_{CC} (low); all operations are disabled, and the device does not respond to any instruction. During a standard power-up phase, the device ignores all commands. After power-up, the device is in standby power mode.

In the event Power-on Reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RESET) will restart the POR process.

At power-down, when VCC drops from the operating voltage to below the threshold voltage V_{CC} (low), all operations are disabled and the device does not respond to any command.

Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, data corruption may result.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion as small as a 64KB block or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

The FM25Q256I3 also provides another Write Protect method using the individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 510 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock. When locked (DYB bit is 0 and PPB bit is 1), the corresponding sector or block can be erased or programmed; when unlocked (DYB bit is 1 or PPB bit is 0), Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all DYB bits will be 1, so the entire memory array is protected from Erase/Program. An “DYB Unlock (39h)” instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-2 is used to decide which Write Protect scheme should be used. When WPS=0(factory default), the device will only utilize CMP, TB, BP[3:0] to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks for write

protection, each protect scheme for the corresponding Block/Sector is available.

9. Register

Three Status Registers are provided for FM25Q256I3. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the Flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Sector lock status, Erase/Program Suspend status and output driver strength, power-up and current Address Mode.
The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Sector OTP lock, Hold/RESET functions, output driver strength and power-up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the WP# pin.

Factory default for all Status Register bits are 0.

9.1. Status Register-1(SR1)

Related Commands: Read Status Register (RDSR1 05h), Write Status Register (WRSR 01h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Enable for Volatile Status Register (50h).

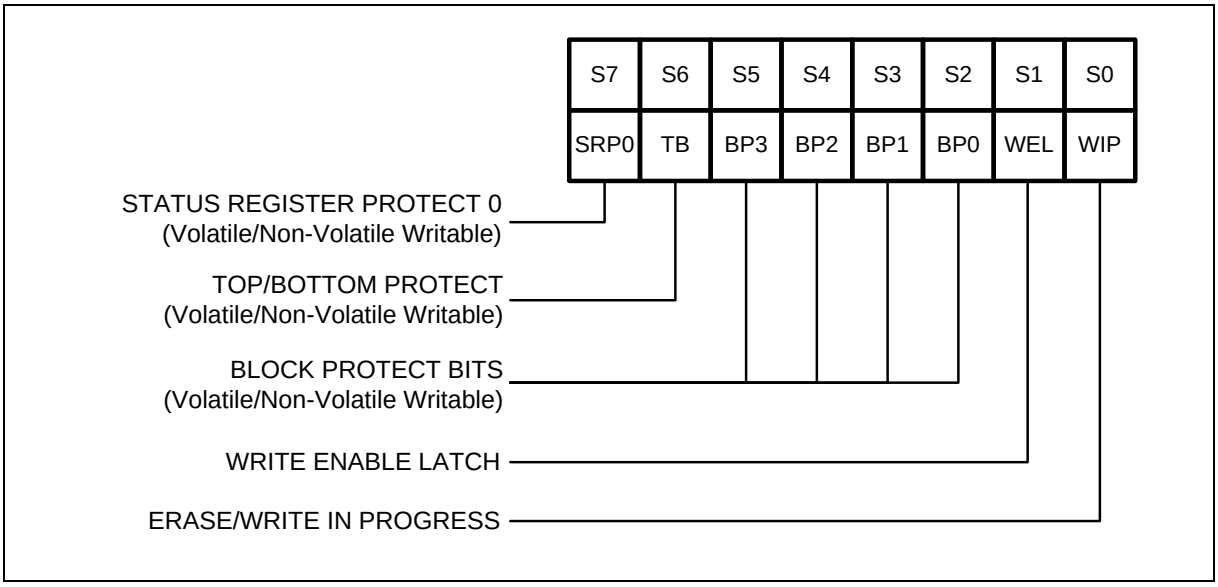


Figure 10 Status Register-1

9.1.1. Write In Progress (WIP)

WIP is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Sector instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in “11.6 AC Electrical Characteristics”). When the program, erase or write status register (or security sector) instruction has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

9.1.2. Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Sector and Program Security Sector.

9.1.3. Block Protect Bits (BP3, BP2, BP1, BP0)

The Block Protect Bits (BP3, BP2, BP1, BP0) are non-volatile read/write bits in the status register that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in "11.6 AC Electrical Characteristics"). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

9.1.4. Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP3, BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

9.2. Status Register-2 (SR2)

Related Commands: Read Status Register-2 (RDSR2 35h), Write Status Register-2 (WRSR2 31h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Enable for Volatile Status Register (50h).

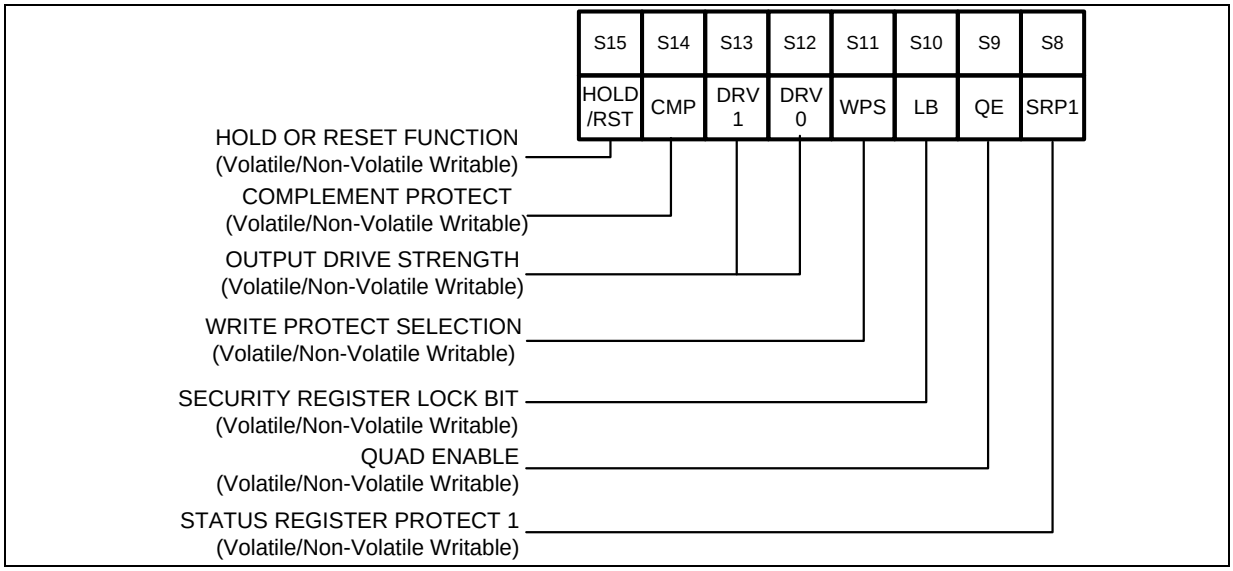


Figure 11 Status Register-2

9.2.1. Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 2 Status Register Protect bits

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protection	WP# pin has no control. The Status register can be written. (Factory Default)
0	1	0	Hardware Protected	When WP# pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When WP# pin is high the Status register is unlocked and can be written.
1	0	X	Power Supply Lock-Down	Status Register is protected and can not be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program	Status Register is permanently protected and can not be written to.

Note:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

9.2.2. HOLD# or RESET# pin function(HOLD/RST)

The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as HOLD#; when HOLD/RST=1, the pin acts as RESET#. However, HOLD# or RESET# functions are only available when QE=0. If QE is set to 1, the HOLD# and RESET# functions are disabled, the pin acts as a dedicated data I/O pin.

9.2.3. Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with TB, BP[3:0] bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by TB, BP3, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB sector can be protected while the rest of the array is not; when CMP=1, the top 64KB sector will become unprotected while the rest of the array become read-only. Please refer to Status Register Memory Protection table for details. The default setting is CMP=0.

9.2.4. Write Protect Selection (WPS)

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, TB, BP[3:0] to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

9.2.5. Output driver strength (DRV1, DRV0)

The DRV1 & DRV0 bits are used to determine the output driver strength.

Table 3 Driver strength configuration

DRV1, DRV0	Driver Strength
0,0	100%
0,1	75%
1,0	50%

1,1	25%

9.2.6. Security Sector Lock Bit (LB)

The Security Register Lock Bit (LB) is non-volatile One Time Program (OTP) bits in Status Register (S10) that provide the write protect control and status to the Security Registers. The default state of LB is 0, Security Registers are unlocked. LB can be set to 1 individually using the Write Status Register instruction. LB is One Time Programmable (OTP), once it's set to 1, the corresponding 1024-Byte Security Register will become read-only permanently.

9.2.7. Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# are enabled. When the QE bit is set to a 1, the Quad DQ2 and DQ3 pins are enabled, and WP# and HOLD# functions are disabled.

QE bit is required to be set to a 1 before issuing an "Enable QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI; otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A "Write Status Register" command in QPI mode cannot change QE bit from a 1 to a 0.

WARNING: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

9.3. Status Register-3 (SR3)

Related Commands: Read Status Register-3 (RDSR3 15h), Write Status Register-3 (WRSR3 11h), Enter 4-Byte Address Mode (B7h), Exit 4-Byte Address Mode (E9h), Write Enable (06h). Write Enable (06h) can be used to clear ERR bit of SR3 if ERR is set to 1 by the last operation.

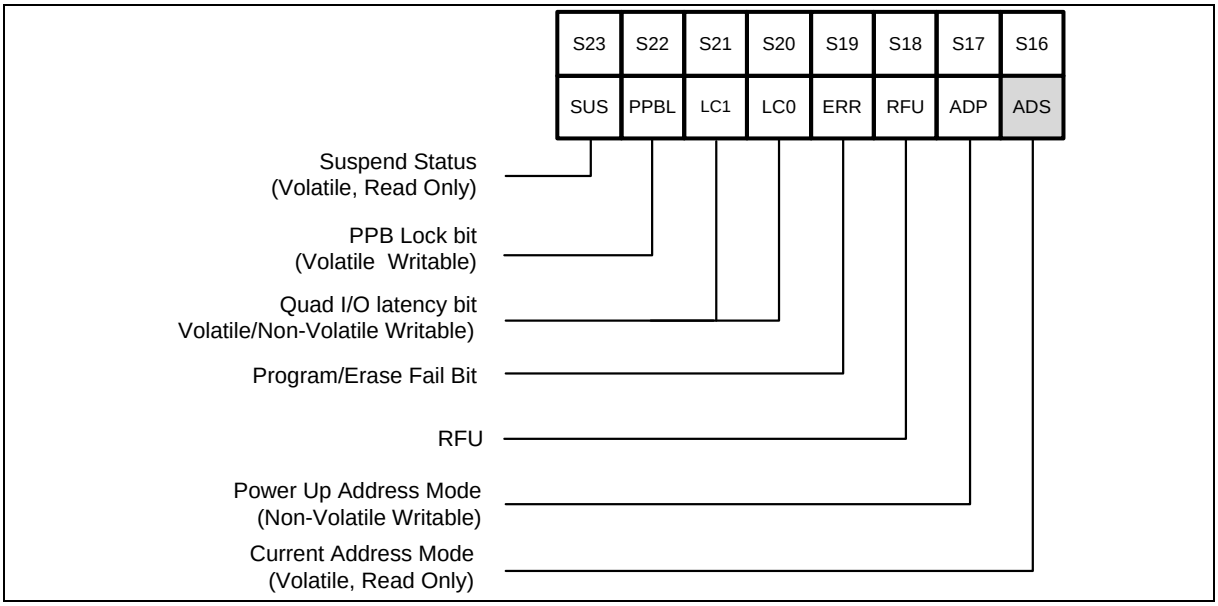


Figure 12 Status Register-3

9.3.1. Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S11) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

9.3.2. Write Fail Bit (ERR)

The Write Fail bit is a status flag, which shows the status of last write operation. It will be set to 1, if the program or erase or write status register operation fails. It is cleard to 0 by WREN (06h) or Reset operation.

if the block or sector to be programed or erased is protected, It also will be set to 1.

9.3.3. Power Up Address Mode (ADP)

The ADP bit is a non-volatile read/write bit in the status register (S17) that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0 (factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

9.3.4. Current Address Mode (ADS)

The Current Address Mode bit is a read only bit in the status register (S16) that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

9.3.5. Latency Code (LC1, LC0)

The Latency Code bits (LC1 and LC0) are non-volatile read/write bits in the status register(S20 and S21). The Latency Code selects the number of continuous mode and dummy cycles between the end of address and the start of read data output for all QIO read commands(EBH, ECH, EDH, EEH) in SPI and read commands in QPI.

Table 4 Latency Code bits for SPI mode

LC (Latency clock number)	DTR SIO/DIO 0Dh/0Eh/ BDh/BEh	DIO in SPI BBh	STR QIO in SPI EBh/ECh	DTR QIO in SPI EDh/EEh	STR in QPI 0Bh/0Ch/ EBh/ECh	DTR in QPI 0Dh/0Eh/ EDh/EEh
00	6	4	6	8	Set by C0h	8
01	8	8	8	8	8	8
10	10	10	10	10	10	10
11	12	12	12	12	12	12

9.3.6. PPB Lock Register–Volatile Writable Only (PPBL)

The PPB Lock Bit is a volatile bit for protecting all PPB bits. When cleared to 0, it locks all PPBs and when set to 1, it allows the PPBs to be changed.

The PPB Lock bit is set to 1 during POR, or Hardware Reset so that the PPB bits are unprotected by a device reset. The Write PPB Lock Bit command is used to clear the PPB Lock bit to 0 to protect the PPB. There is no command to set the PPB Lock bit to 1, therefore the PPB Lock bit will remain at 0 until the next power-off or hardware reset.

The PPB Lock Bit must be cleared to 0 only after all the PPBs are configured to the desired settings.

Related Commands: Read PPB Lock bit (RDSR3 15h), Write PPB Lock Register (WRPPBL A6h).

9.4. Status Register Memory Protection (WPS=0, CMP=0)

Table 5 Status Register Memory Protection (WPS=0, CMP=0)

STATUS REGISTER					FM25Q256I3 (256M-BIT) MEMORY PROTECTION			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h – 01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 thru 511	01FE0000h – 01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 thru 511	01FC0000h – 01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 thru 511	01F80000h – 01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 thru 511	01F00000h – 01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 thru 511	01E00000h – 01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 thru 511	01C00000h – 01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 thru 511	01800000h – 01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 thru 511	01000000h – 01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0 thru 3	00000000h – 0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 thru 7	00000000h – 0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 thru 15	00000000h – 0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 thru 31	00000000h – 0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 thru 63	00000000h – 000FFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 thru 127	00000000h – 001FFFFFh	2MB	Lower 1/16
1	0	1	1	1	0 thru 15	00000000h – 003FFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 thru 31	00000000h – 007FFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 thru 63	00000000h – 00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	0 thru 511	00000000h – 01FFFFFFh	32MB	ALL
X	1	X	1	X	0 thru 511	00000000h – 01FFFFFFh	32MB	ALL

9.5. Status Register Memory Protection (WPS=0, CMP=1)

Table 6 Status Register Memory Protection (WPS=0, CMP=1)

STATUS REGISTER					FM25Q256I3 (256M-BIT) MEMORY PROTECTION			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	ALL	00000000h – 01FFFFFFh	ALL	ALL
0	0	0	0	1	0 thru 510	00000000h – 01FEFFFFh	32,704KB	Lower 511/512
0	0	0	1	0	0 thru 509	00000000h – 01FDFFFFh	32,640KB	Lower 255/256
0	0	0	1	1	0 thru 507	00000000h – 01FBFFFFh	32,512KB	Lower 127/128
0	0	1	0	0	0 thru 503	00000000h – 01F7FFFFh	32,256KB	Lower 63/64
0	0	1	0	1	0 thru 495	00000000h – 01EFFFFFh	31MB	Lower 31/32
0	0	1	1	0	0 thru 479	00000000h – 01DFFFFFh	30MB	Lower 15/16
0	0	1	1	1	0 thru 447	00000000h – 01BFFFFFh	28MB	Lower 7/8
0	1	0	0	0	0 thru 383	00000000h – 017FFFFFh	24MB	Lower 3/4
0	1	0	0	1	0 thru 255	00000000h – 00FFFFFFh	16MB	Lower 1/2
1	0	0	0	1	1 thru 511	00010000h – 01FFFFFFh	•	Upper 511/512
1	0	0	1	0	2 thru 511	00020000h – 01FFFFFFh	32,640KB	Upper 255/256
1	0	0	1	1	4 thru 511	00040000h – 01FFFFFFh	32,512KB	Upper 127/128
1	0	1	0	0	8 thru 511	00080000h – 01FFFFFFh	32,256KB	Upper 63/64
1	0	1	0	1	16 thru 511	00100000h – 01FFFFFFh	31MB	Upper 31/32
1	0	1	1	0	32 thru 511	00200000h – 01FFFFFFh	30MB	Upper 15/16
1	0	1	1	1	64 thru 511	00400000h – 01FFFFFFh	28MB	Upper 7/8
1	1	0	0	0	128 thru 511	00800000h – 01FFFFFFh	24MB	Upper 3/4
1	1	0	0	1	256 thru 511	01000000h – 01FFFFFFh	16MB	Upper 1/2
X	1	1	0	X	NONE	NONE	NONE	NONE
X	1	X	1	X	NONE	NONE	NONE	NONE

9.6. Status Register Memory Protection (WPS=1)

Advanced Sector Protection (ASP) is the name used for a set of independent hardware and software methods used to disable or enable programming or erase operations, individually, in any or all sectors. An overview of these methods is shown in Figure 13.

Block Protection and ASP protection settings for each sector are logically OR'd to define the protection for each sector, i.e. if either mechanism is protecting a sector the sector cannot be programmed or erased.

Every main flash array sector has a non-volatile (PPB) and a volatile (DYB) protection bit associated with it. When PPB bit is 0 or DYB bit is 1, the sector is protected from program and erase operations.

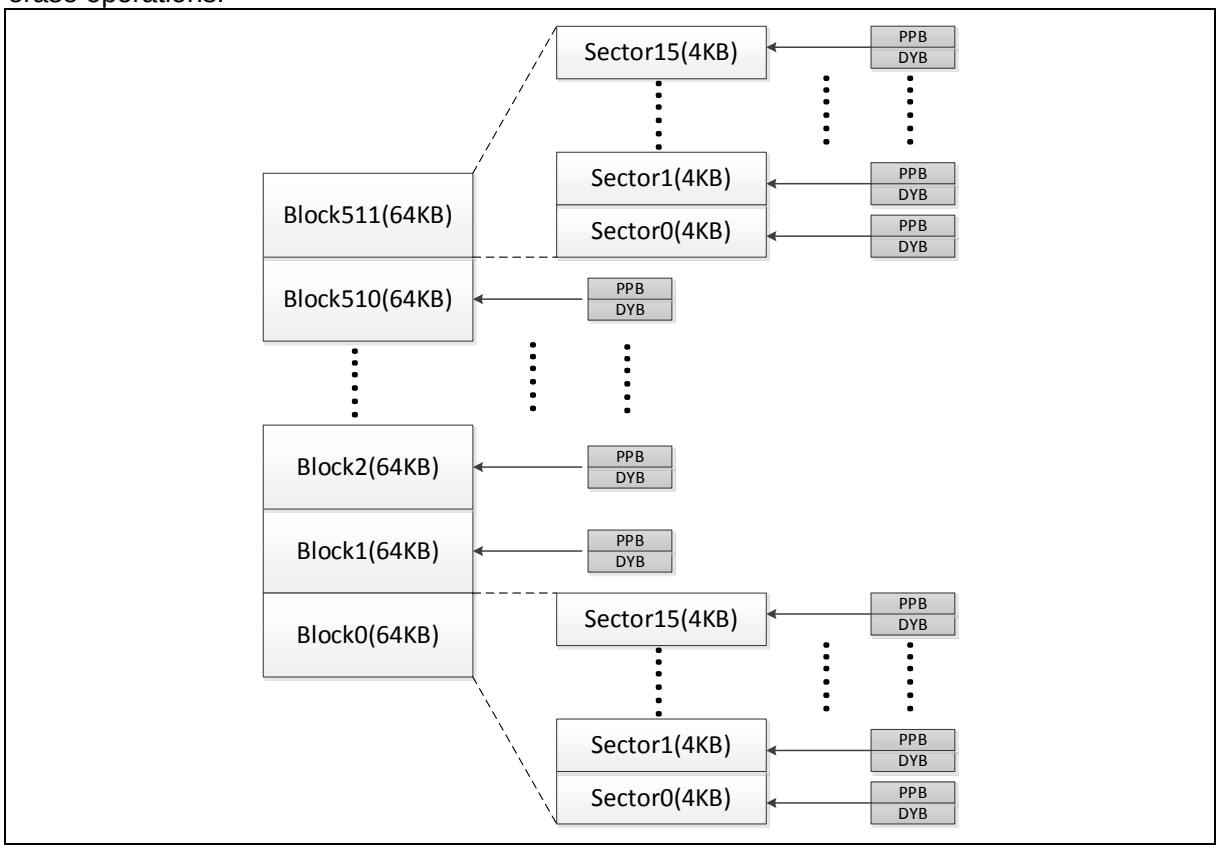


Figure 13 Individual Sector/Block Locks

The PPB bits are protected from program and erase when the PPB Lock bit is 0. PPB Lock bit is set to 1 during POR, or Hardware Reset so that the PPB bits are unprotected by a device reset. There is a command to clear the PPB Lock bit to 0 to protect the PPB. There is no command in the Persistent Protection method to set the PPB Lock bit to 1, therefore the PPB Lock bit will remain at 0 until the next power-off or hardware reset. This method allows boot code the option of changing sector protection by programming or erasing the PPB, then protecting the PPB from further change for the remainder of normal system operation by clearing the PPB Lock bit to 0. This is sometimes called Boot-code controlled sector protection.

9.6.1. Persistent Protection Bits

The Persistent Protection Bits (PPB) are located in a separate nonvolatile flash array. One of the PPB bits is related to each sector. When a PPB is 0, it's related sector is protected from program and erase operations. The PPB are programmed individually but must be erased as a group, similar to the way individual words may be programmed in the main array but an entire sector must be erased at the same time. The PPB have the same program and erase endurance as the

main flash memory array. Preprogramming and verification prior to erasure are handled by the device.

Programming a PPB bit requires the typical page programming time. Erasing all the PPBs requires typical sector erase time. During PPB bit programming and PPB bit erasing, status is available by reading the Status register. Reading of a PPB bit requires the initial access time of the device.

Notes:
1. Each PPB is individually programmed to 0 and all are erased to 1 in parallel.
2. If the PPB Lock bit is 0, the PPB Program or PPB Erase command does not execute and fails without programming or erasing the PPB.
3. The state of the PPB for a given sector can be verified by using the PPB Read command.

9.6.2. Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYB only control the protection for sectors that have their PPB set to 1. By issuing the DYB Write command, a DYB is cleared to 0 or set to 1, thus placing each sector in the unprotected or protected state respectively. This feature allows software to easily protect sectors against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed. The DYBs can be set or cleared as often as needed as they are volatile bits.

9.6.3. Sector Protection States Summary

Each sector can be in one of the following protection states:

■ Unlocked — The sector is unprotected and protection can be changed by a simple command. The protection state defaults to unprotected after a power cycle, software reset, or hardware reset.

■ Dynamically Locked — A sector is protected and protection can be changed by a simple command. The protection state is not saved across a power cycle or reset.

■ Persistently Locked — A sector is protected and protection can only be changed if the PPB Lock Bit is set to 1. The protection state is non-volatile and saved across a power cycle or reset. Changing the protection state requires programming and or erase of the PPB bits.

Protection Bit Values			Sector State
PPB Lock	PPB	DYB	
1	1	0	Unprotected - PPB and DYB are changeable
1	1	1	protected - PPB and DYB are changeable
1	0	0	protected - PPB and DYB are changeable
1	0	1	protected - PPB and DYB are changeable
0	1	0	Unprotected - PPB not changeable, DYB is changeable
0	1	1	protected - PPB not changeable, DYB is changeable
0	0	0	protected - PPB not changeable, DYB is changeable
0	0	1	protected - PPB not changeable, DYB is changeable

9.7. Extended Address Register

In addition to the Status Registers, FM25Q256I3 provides a volatile Extended Address Register which consists of the 4th byte of memory addresss. The Extended Address Register is used only when the device is operating in the 3-Byte Address Mode (ADS=0). The lower 128Mb memory array (00000000h – 00FFFFFFh) is selected when A24=0, all instructions with 3-Byte addresses will be excuted within that region. When A24=1, the upper 128Mb memory array (01000000h –

01FFFFFFh) will be selected.

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7h)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Register setting will be ignord. However, any command with 4-byte address input will replace the Extended Address Register Bites (A31 – A24) with new settings.

Upon power up or after the execution of a Software/Hardware Reset, the Extended Address Register values will be cleared to 0.

The READ operation begins reading in the selected 128Mb segment, but is not bound by it. In a continuous READ, when the last byte of the segment is read, the next byte output is the first byte of the other segment as the operation wraps to 0000000h; Therefore, a download of the whole array is possible with one READ operation. The value of the extended address register does not change when a READ operation crosses the selected 128Mb boundary.

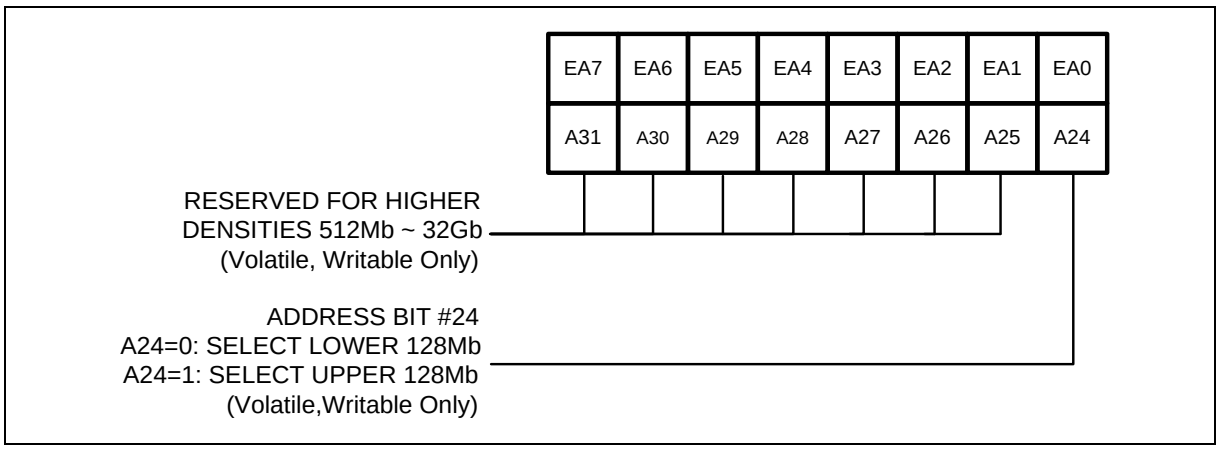


Figure 14 Extended Address Register

10. Instructions

The Standard/Dual/Quad SPI instruction set of the FM25Q256I3 consists of 58 basic instructions that are fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the FM25Q256I3 consists of 41 basic instructions that are fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked through DQ[3:0] pins provides the instruction code. Data on all four DQ pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four DQ pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of CS#. Clock relative timing diagrams for each instruction are included in Figure 15 through Figure 127. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

10.1. Device ID and Instruction Set Tables

10.1.1. Manufacture and Device Identification

Table 7 Manufacturer and Device Identification

OP Code	MF7-MF0	ID15-ID0	ID7-ID0
ABh			18h
90h, 92h, 94h	A1h		18h
9Fh	A1h	4019h	

10.1.2. Instructions Set Table 1 (Standard/Dual/Quad SPI, 3- & 4-Byte Address Mode) (1)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*	
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Read Status Register-1	**05h**	(S7-S0)(2)					
Write Status Register-1(3)	**01h**	(S7-S0)(3)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Write Status Register-2	**31h**	(S15-S8)					
Read Status Register-3	**15h**	(S23-S16)(2)					
Write Status Register-3	**11h**	(S23-S16)					
Read Extended Addr. Register	**C8h**	(EA7-EA0)(3)					
Write Extended Addr. Register	**C5h**	(EA7-EA0)					
Chip Erase	**C7h/60h**						
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Release Powerdown / ID(5)	**ABh**	dummy	dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID(5)(6)	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID(6)	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read SFDP Register	**5Ah**	00h	00h	A7-A0	dummy	(D7-D0)	
Enable QPI	**38h**						
Enter 4-Byte Address Mode	**B7h**						
Exit 4-Byte Address Mode	**E9h**						
Enable Reset	**66h**						
Reset	**99h**						
Global DYB Lock	**7Eh**						
Global DYB Unlock	**98h**						
Read Data with 4-byte Address	**13h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read with 4-Byte Address	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read Dual Output with 4-Byte Address	**3Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0, …)(9)
Fast Read Quad Output with 4-Byte Address	**6Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0, …)(11)
Fast Read Dual I/O with 4-Byte Address	**BCh**	A31-A16(8)	A15-A0(8)	M7-M0, (D7-D0)(8)	(D7-D0, …)(11)		
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A0(10)	M7-M0(10), Dmy3-0(10), (D7-	(D7-D0, …)(11)			

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
			D0) (11)				
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0		
Quad Page Program with 4-Byte Address	**34h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0, …(11)	
Sector Erase with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0		
PPB Read	**E2h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
PPB Program	**E3h**	A31-A24	A23-A16	A15-A8	A7-A0		
PPB Erase	**E4h**	A31-A24	A23-A16	A15-A8	A7-A0		
Write PPB Lock Register	**A6h**						

10.1.3. Instructions Set Table 2 (Standard/Dual/Quad SPI, 3-Byte Address Mode) (1)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(4)
Quad Page Program	**32h**	A23-A16	A15-A8	A7-A0	D7-D0, …(11)	D7-D0, …(11)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Read Unique ID(6)	**4Bh**	dummy	dummy	dummy	dummy	(UID63-UID0)
Erase Security Sectors(7)	**44h**	A23-A16	A15-A8	A7-A0		
Program Security Sectors(7)	**42h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0
Read Security Sectors(7)	**48h**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Individual DYB Lock	**36h**	A23-A16	A15-A8	A7-A0		
Individual DYB Unlock	**39h**	A23-A16	A15-A8	A7-A0		
Read DYB	**3Dh**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0, …)(9)
Fast Read Dual I/O	**BBh**	A23-A8(8)	A7-A0, M7-M0 (8)	(D7-D0, …)(9)		
Manufacturer/Device ID by Dual I/O(5)(6)	**92h**	A23-A8(8)	A7-A0, M7-M0(8)	(MF7-MF0, ID7-ID0)		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy(18)	(D7-D0, …)(11)
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0(10)	Dummy(15)	(D7-D0, …)(11)		
Word Read Quad I/O(12)	**E7h**	A23-A0, M7-M0(10)	Dummy(15)	(D7-D0, …)(11)		
Octal Word Read Quad I/O(13)	**E3h**	A23-A0, M7-M0(10)	Dummy(15)	(D7-D0, …)(11)		

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Manufacture/Device ID by Quad I/O(5)(6)	**94h**	A23-A0, M7-M0(10)	xxxx, (MF7-MF0, ID7-ID0)	(MF7-MF0, ID7-ID0, …)		
Set Burst with Wrap	**77h**	xxxxxxh, W8-W0(10)				

10.1.4. Instructions Set Table 3 (Standard/Dual/Quad SPI, 4-Byte Address Mode) (1)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*	*(48-55)*
Page Program	**02h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(4)
Quad Page Program	**32h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0, …(11)	D7-D0, …(11)
Sector Erase (4KB)	**20h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A31-A24	A23-A16	A15-A8	A7-A0		
Read Data	**03h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Read Unique ID(6)	**4Bh**	dummy	dummy	dummy	dummy	dummy	(UID63-UID0)
Erase Security Sectors(7)	**44h**	A31-A24	A23-A16	A15-A8	A7-A0		
Program Security Sectors(7)	**42h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0
Read Security Sectors(7)	**48h**	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Individual DYB Lock	**36h**	A31-A24	A23-A16	A15-A8	A7-A0		
Individual DYB Unlock	**39h**	A31-A24	A23-A16	A15-A8	A7-A0		
Read DYB	**3Dh**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read Dual Output	**3Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0, …)(9)
Fast Read Dual I/O	**BBh**	A31-A16(8)	A15-A0(8)	M7-M0 (8)	(D7-D0, …)(9)		
Manufacturer/Device ID by Dual I/O(5)(6)	**92h**	A31-A16(8)	A15-A0(8)	Dummy(15), (MF7-MF0) (9)	(ID7-ID0,MF7-MF0) (9)		
Fast Read Quad Output	**6Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(18)	(D7-D0, …)(11)
Fast Read Quad I/O	**EBh**	A31-A0	M7-M0(10) Dummy(15)	(D7-D0, …)(11)			
Word Read Quad I/O(12)	**E7h**	A31-A0	M7-M0(10), Dummy(15), (D7-D0)(11)	(D7-D0, …)(11)			
Octal Word Read Quad I/O(13)	**E3h**	A31-A0	M7-M0(10), Dummy(15), (D7-D0, …)(11)	(D7-D0, …)(11)			
Manufacture/Device ID by Quad I/O(5)(6)	**94h**	A31-A0	M7-M0(10) xxxxxxh	(MF7-MF0, ID7-ID0, …)			
Set Burst with Wrap	**77h**	xxxxxxxxh	W8-W0(10)				

10.1.5. Instructions Set Table 7 (DTR SPI, 3-Byte Address Mode)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8
CLOCK NUMBER$_{(1-1-1)}$	*8*	*4*	*4*	*4*	*(n)* (16)	*4*	*4*	*4*
DTR Fast Read	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…	
CLOCK NUMBER$_{(1-1-2)}$	*8*	*4*	*4*	*4*	*2*	*(n-2)* (16)	*2*	*2*
DTR Fast Read Dual I/O	**BDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0	…
CLOCK NUMBER$_{(1-1-4)}$	*8*	*4*	*4*	*4*	*1*	*(n-1)* (16)	*2*	*2*
DTR Fast Read Quad I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0	…
CLOCK NUMBER$_{(1-1-1)}$	*8*	*4*	*4*	*4*	*4*	*(n)* (16)	*4*	*4*
DTR Fast Read With 4Byte Address	**0Eh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…
CLOCK NUMBER$_{(1-2-2)}$	*8*	*2*	*2*	*2*	*2*	*2*	*(n-2)* (16)	*2*
DTR Fast Read Dual I/O With 4Byte Address	**BEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0
CLOCK NUMBER$_{(1-4-4)}$	*8*	*1*	*1*	*1*	*1*	*1*	*(n-1)* (16)	*1*
DTR Fast Read Quad I/O With 4Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0

10.1.6. Instructions Set Table 8 (DTR SPI, 4-Byte Address Mode)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8
CLOCK NUMBER$_{(1-1-1)}$	*8*	*4*	*4*	*4*	*4*	*(n)* (16)	*4*	*4*
DTR Fast Read	**0Dh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…
DTR Fast Read With 4Byte Address	**0Eh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…
CLOCK NUMBER$_{(1-2-2)}$	*8*	*2*	*2*	*2*	*2*	*2*	*(n-2)* (16)	*2*
DTR Fast Read Dual I/O	**BDh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0
DTR Fast Read Dual I/O With 4Byte Address	**BEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0
CLOCK NUMBER$_{(1-4-4)}$	*8*	*1*	*1*	*1*	*1*	*1*	*(n-1)* (16)	*1*
DTR Fast Read Quad I/O	**EDh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0
DTR Fast Read Quad I/O With 4Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0

10.1.7. Instructions Set Table 4 (QPI, 3- & 4-Byte Address Mode) (14)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
CLOCK NUMBER	*(0,1)*	*(2,3)*	*(4,5)*	*(6,7)*	*(8,9)*	*(10,11)*	
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Read Status Register-1	**05h**	(S7-S0)(2)					
Write Status Register-1(3)	**01h**	(S7-S0) (3)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Write Status Register-2	**31h**	(S15-S8)					
Read Status Register-3	**15h**	(S23-					

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
		S16)[2]					
Write Status Register-3	**11h**	(S23-S16)					
Read Status Register-4	**45h**	(S31-S24)[2]					
Write Status Register-4	**41h**	(S31-S24)					
Read Status Register-5	**55h**	(S39-S32)[2]					
Write Status Register-5	**51h**	(S39-S32)					
Read Extended Addr. Register	**C8h**	(EA7-EA0)[3]					
Write Extended Addr. Register	**C5h**	(EA7-EA0)					
Set Read Parameters	**C0h**	P7-P0					
Chip Erase	**C7h/60h**						
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Release Powerdown / ID[5]	**ABh**	dummy	dummy	Dummy	(ID7-ID0)[2]		
Manufacturer/Device ID[5][6]	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID[6]	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Exit QPI Mode	**FFh**						
Enter 4-Byte Address Mode	**B7h**						
Exit 4-Byte Address Mode	**E9h**						
Enable Reset	**66h**						
Reset	**99h**						
Global DYB Lock	**7Eh**						
Global DYB Unlock	**98h**						
Fast Read with 4-Byte Address	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A0[10]	M7-M0[10], Dmy3-0[10], (D7-D0) [11]	(D7-D0, …)[11]			
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0, …[11]	
Sector Erase with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0		
PPB Read	**E2h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
PPB Program	**E3h**	A31-A24	A23-A16	A15-A8	A7-A0		
PPB Erase	**E4h**	A31-A24	A23-A16	A15-A8	A7-A0		
Write PPB Lock Register	**A6h**						

10.1.8. Instructions Set Table 5 (QPI, 3-Byte Address Mode) (14)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0,1)*	*(2,3)*	*(4,5)*	*(6,7)*	*(8,9)*	*(10,11)*
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0(11)	D7-D0(4)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy(15)	(D7-D0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0(15)	(D7-D0)
Individual DYB Lock	**36h**	A23-A16	A15-A8	A7-A0		
Individual DYB Unlock	**39h**	A23-A16	A15-A8	A7-A0		
Read DYB	**3Dh**	A23-A16	A15-A8	A7-A0	(D7-D0) (2)	

10.1.9. Instructions Set Table 6 (QPI, 4-Byte Address Mode) (14)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
CLOCK NUMBER	*(0,1)*	*(2,3)*	*(4,5)*	*(6,7)*	*(8,9)*	*(10,11)*	*(11,12)*
Page Program	**02h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0(11)	D7-D0(4)
Sector Erase (4KB)	**20h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A31-A24	A23-A16	A15-A8	A7-A0		
Fast Read	**0Bh**	A31-A24	A23-A16	A15-A8	A7-A0	dummy(15)	(D7-D0)
Fast Read Quad I/O	**EBh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(15)	(D7-D0)
Individual DYB Lock	**36h**	A31-A24	A23-A16	A15-A8	A7-A0		
Individual DYB Unlock	**39h**	A31-A24	A23-A16	A15-A8	A7-A0		
Read DYB	**3Dh**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0) (2)	

10.1.10. Instructions Set Table 9 (DTR QPI, 3-Byte Address Mode)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8
CLOCK NUMBER(4-4-4)	*2*	*1*	*1*	*1*	*(n)* (16)	*1*	*1*	*1*
DTR Fast Read with Wrap	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…	
CLOCK NUMBER(4-4-4)	*2*	*1*	*1*	*1*	*1*	*(n-1)* (16)	*1*	*1*
DTR Fast Read Quad I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0	…
CLOCK NUMBER(4-4-4)	*2*	*1*	*1*	*1*	*1*	*(n)* (16)	*1*	*1*
DTR Fast Read With 4Byte Address with Wrap	**0Eh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…
CLOCK NUMBER(4-4-4)	*2*	*1*	*1*	*1*	*1*	*1*	*(n-1)* (16)	*1*
DTR Fast Read Quad I/O With 4Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0

10.1.11. Instructions Set Table 10 (DTR QPI, 4-Byte Address Mode)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8
CLOCK NUMBER(4-4-4)	*2*	*1*	*1*	*1*	*(n)* (16)	*1*	*1*	*1*
DTR Fast Read with Wrap	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…	
DTR Fast Read With 4Byte Address with Wrap	**0Eh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	…
CLOCK NUMBER(4-4-4)	*2*	*1*	*1*	*1*	*1*	*(n-1)* (16)	*1*	*1*
DTR Fast Read Quad I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0	…
DTR Fast Read Quad I/O With 4Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	D7-D0

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The Status Register contents/Device ID/ASP contnets will repeat continuously until CS# terminates the instruction.
3. Write Status Register-1(01h) can also be used to program Status Register-1&2, see secion 10.2.4.
4. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Sectors, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
5. See Table 7 for device ID information.
6. This feature is available upon special order. Please contact Shanghai Fudan Microelectronics Group Co., Ltd for details.
7. Security Sector Address:
   Security Sector 0: A23-A16 = 00h; A15-A8 = 00h; A7-A0 = byte address
   Security Sector 1: A23-A16 = 00h; A15-A8 = 01h; A7-A0 = byte address
   Security Sector 2: A23-A16 = 00h; A15-A8 = 10h; A7-A0 = byte address
   Security Sector 3: A23-A16 = 00h; A15-A8 = 11h; A7-A0 = byte address
8. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
9. Dual SPI data output format:
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)
10. Quad SPI address input format:
    DQ_0 = A20, A16, A12, A8, A4, A0, M4, M0
    DQ_1 = A21, A17, A13, A9, A5, A1, M5, M1
    DQ_2 = A22, A18, A14, A10, A6, A2, M6, M2
    DQ_3 = A23, A19, A15, A11, A7, A3, M7, M3
    Set Burst with Wrap input format:
    DQ_0 = x, x, x, x, x, x, W4, x
    DQ_1 = x, x, x, x, x, x, W5, x
    DQ_2 = x, x, x, x, x, x, W6, x
    DQ_3 = x, x, x, x, x, x, x, x
11. Quad SPI data input/output format:
    DQ_0 = (D4, D0, …)
    DQ_1 = (D5, D1, …..)
    DQ_2 = (D6, D2, …..)
    DQ_3 = (D7, D3, …..)
12. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)
13. For Octal Word Read Quad I/O, the lowest four address bits must be 0. (A3, A2, A1, A0 = 0)
14. QPI Command Address, Data input/output format:

CLK#	0	1	2	3	4	5	6	7	8	9	10	11
DQ_0	C4	C0	A20	A16	A12	A8	A4	A0	D4	D0	D4	D0
DQ_1	C5	C1	A21	A17	A13	A9	A5	A1	D5	D1	D5	D1
DQ_2	C6	C2	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2

DQ_3	C7	C3	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3

15. The number of dummy clocks is controlled by Set Read Parameters Command or LC bits in SR3.
16. The number of dummy clocks is controlled by LC bits in SR3..

10.2. Instruction Description

10.2.1. Write Enable (WREN) (06h)

The Write Enable (WREN) instruction sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Sectors instruction. The Write Enable **(**WREN**)** instruction is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

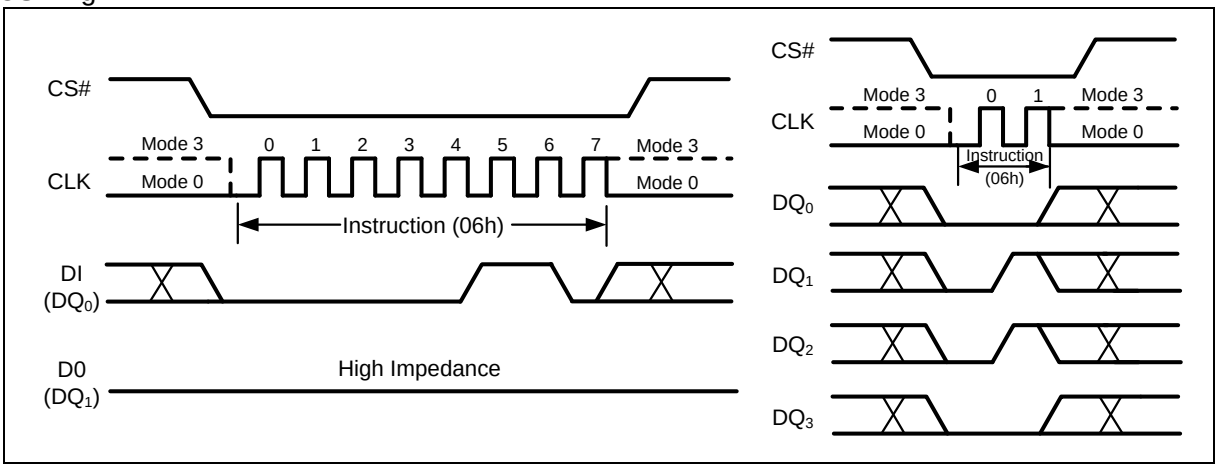


Figure 15 Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

10.2.2. Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 9.1, 9.2, 9.3 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

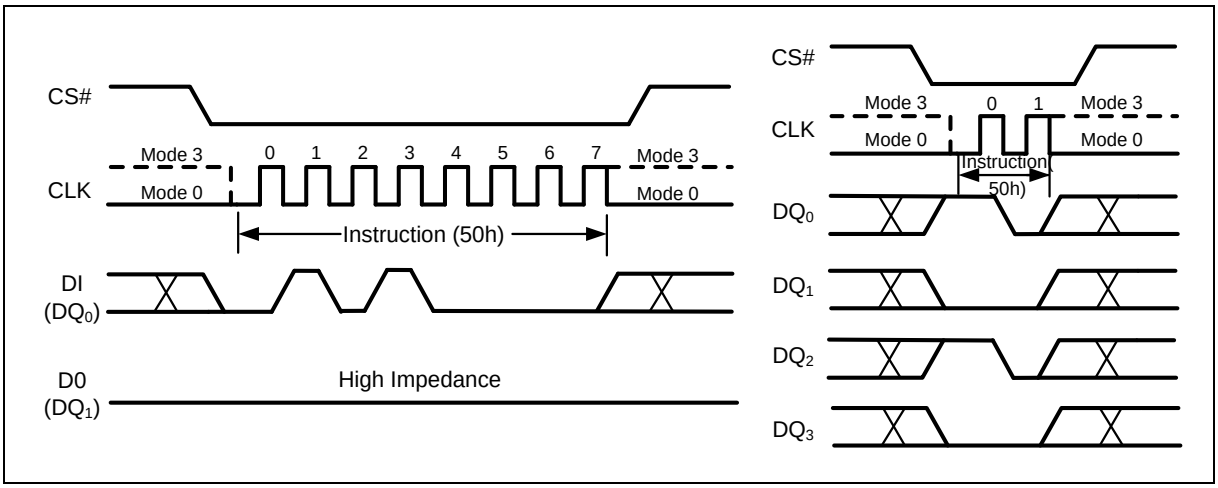


Figure 16 Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

10.2.3. Write Disable (WRDI) (04h)

The Write Disable (WRDI) instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable (WRDI) instruction is entered by driving CS# low, shifting the instruction code "04h" into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Sectors, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

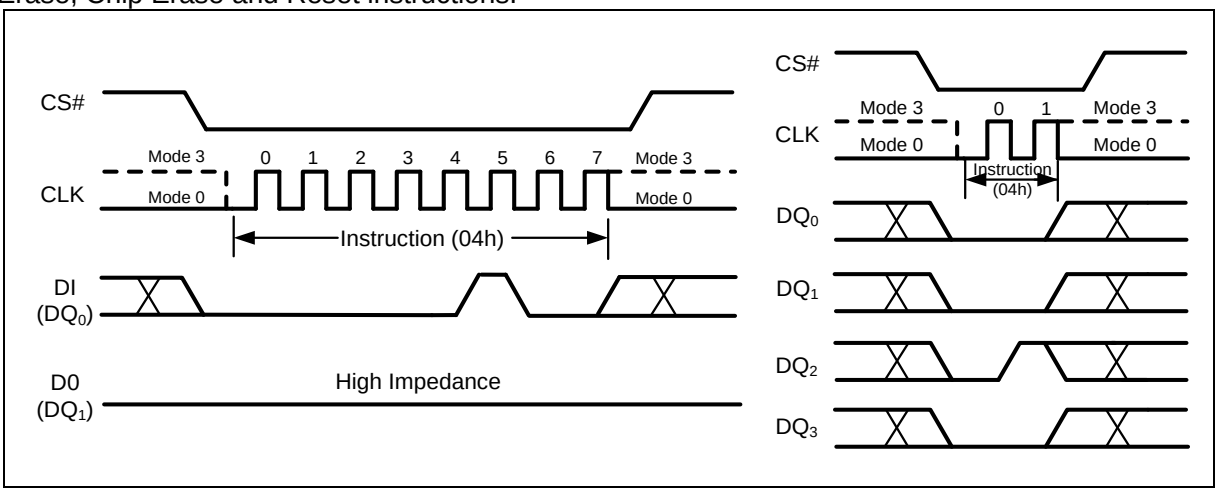


Figure 17 Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

10.2.4. Read Status Register-1 (RDSR1) (05h), Status Register-2 (RDSR2) (35h) & Status Register-3 (RDSR3) (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code "05h" for Status Register-1, "35h" for Status Register-2 or "15h" for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 18. Refer to section 9.1, 9.2 and 9.3 for Status Register description.

The Read Status Register instruction may be used at any time, even while a Program, Erase or

Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 19. The instruction is completed by driving CS# high.

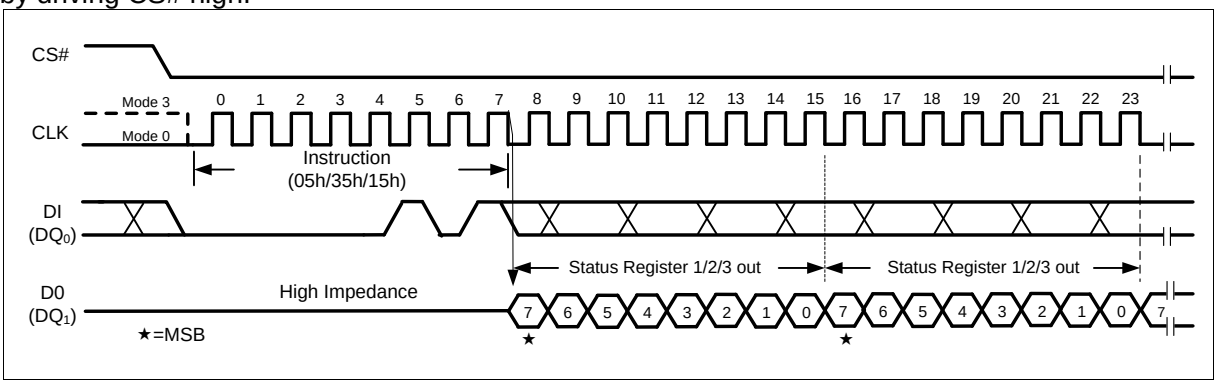


Figure 18 Read Status Register Instruction (SPI Mode)

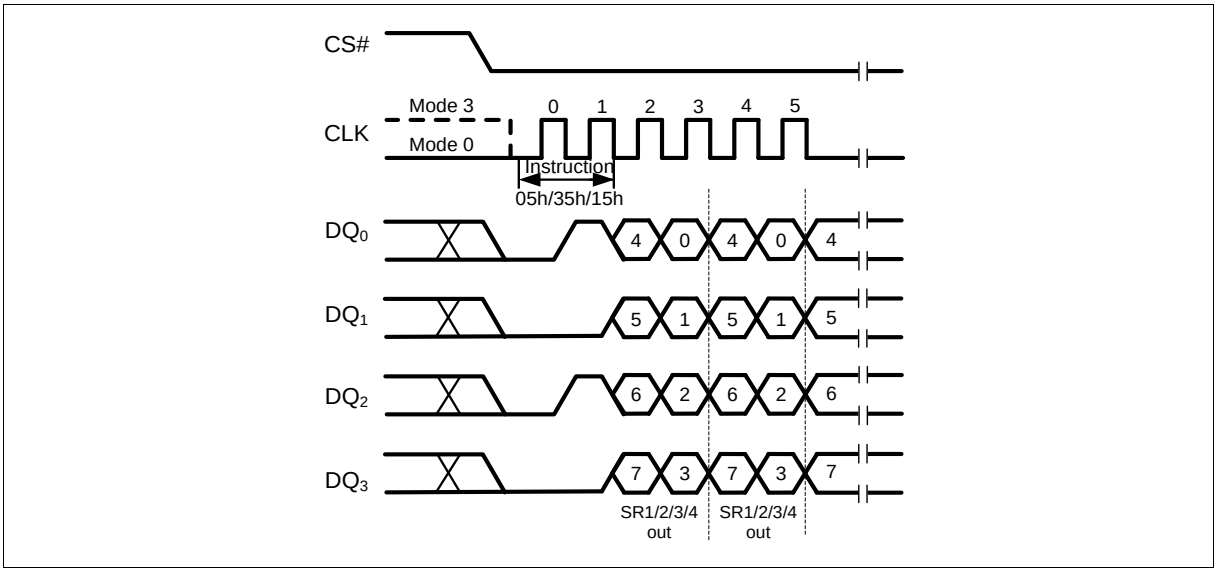


Figure 19 Read Status Register Instruction (QPI Mode)

10.2.5. Write Status Register-1 (WRSR1) (01h), Status Register-2 (WRSR2) (31h) & Status Register-3 (WRSR3) (11h)

The Write Status Register instruction allows the Status Register to be written. The writable Status Register bits include: SRP0, TB, BP3, BP2, BP1 and BP0 in Status Register-1; HOLD/RST, CMP, LB, QE, SRP1, DRV1, DRV0 and WPS in Status Register-2; LC1-0,,ADP in Status Register-3. All other Status Register bit locations are read-only and will not be affected by Write Status Register instruction. LB is a non-volatile OTP bit, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 20 and Figure 21.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL

remains 0). However, SRP1 and LB cannot be changed from 1 to 0 because of the OTP protection for these bits. Upon power off or the execution of Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See "11.6 AC Electrical Characteristics"). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after CS# is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See "11.6 AC Electrical Characteristics"). WIP bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to 0 when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Refer to section 9.1, 9.2, 9.3 for Status Register description. Factory default for all status Register bits are 0.

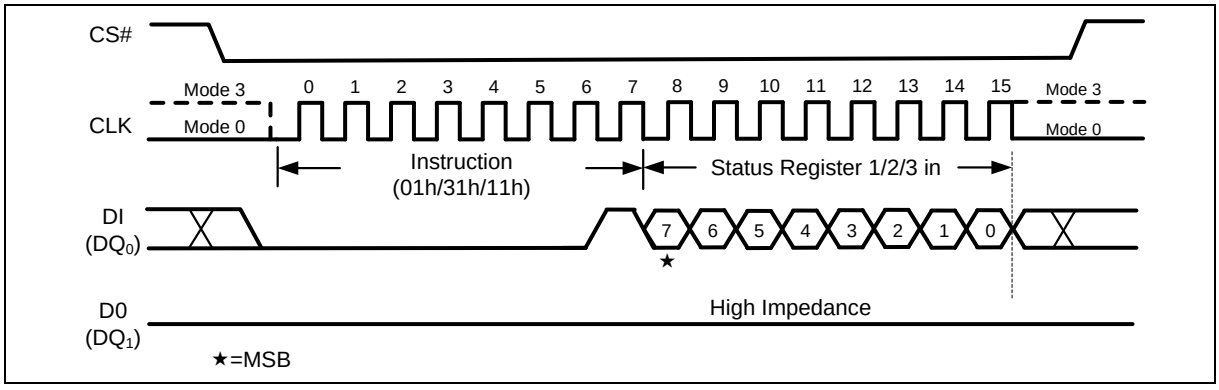


Figure 20 Write Status Register-1/2/3 Instruction (SPI Mode)

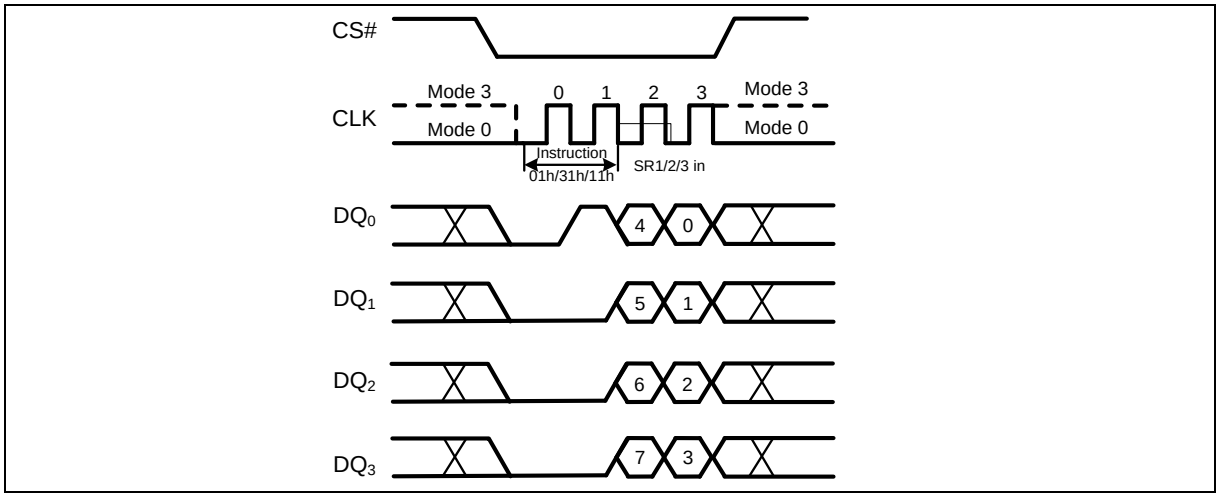


Figure 21 Write Status Register-1/2/3 Instruction (QPI Mode)

The FM25Q256I3 is also backward compatible to FMSH's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Register-1(01h)" command. To complete the Write Status Register1&2, the CS# pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 22. If CS# is driven high after the eighth clock, the Write Status Register (WRSR) instruction will only program the Status Register-1 and the Status Register-2 will not be affected.

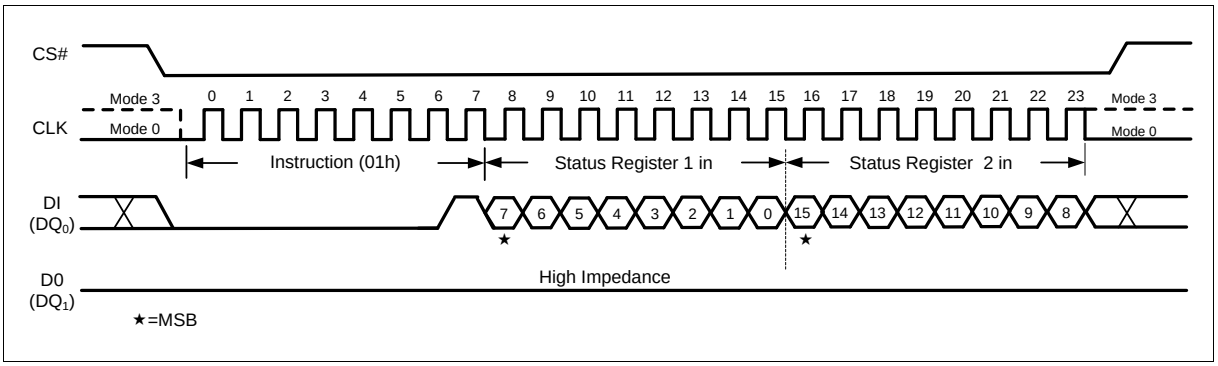


Figure 22 Write Status Register-1/2 Instruction (backward compatible,SPI Mode)

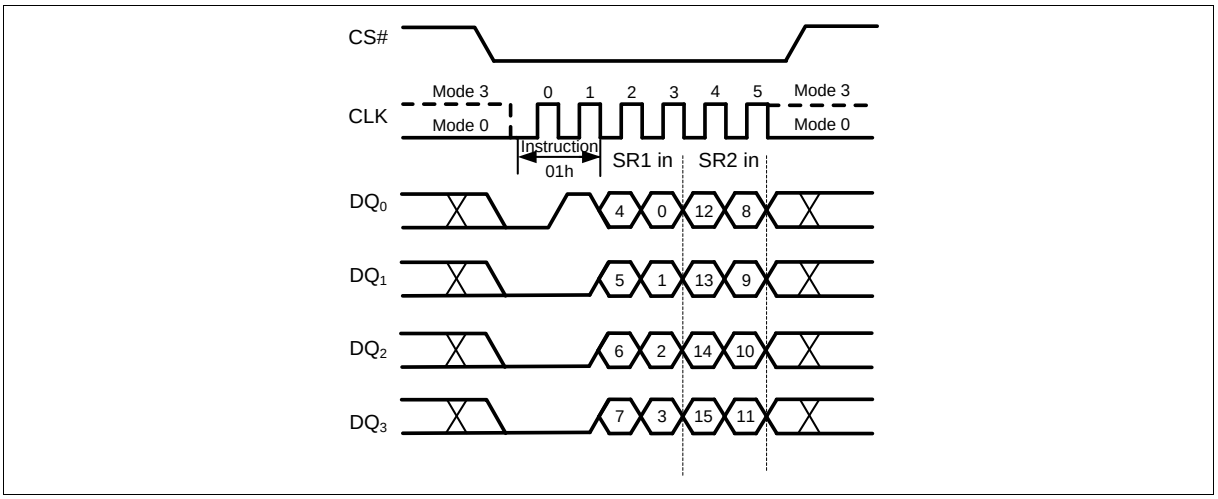


Figure 23 Write Status Register-1/2 Instruction (backward compatible,QPI Mode)

10.2.6. Read Extended Address Register(C8h)

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving CS# low and shifting the instruction code "C8h" into the DI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 24.

When the device is in the 4-Byte Address Mode, the Extended Address Register is not used.

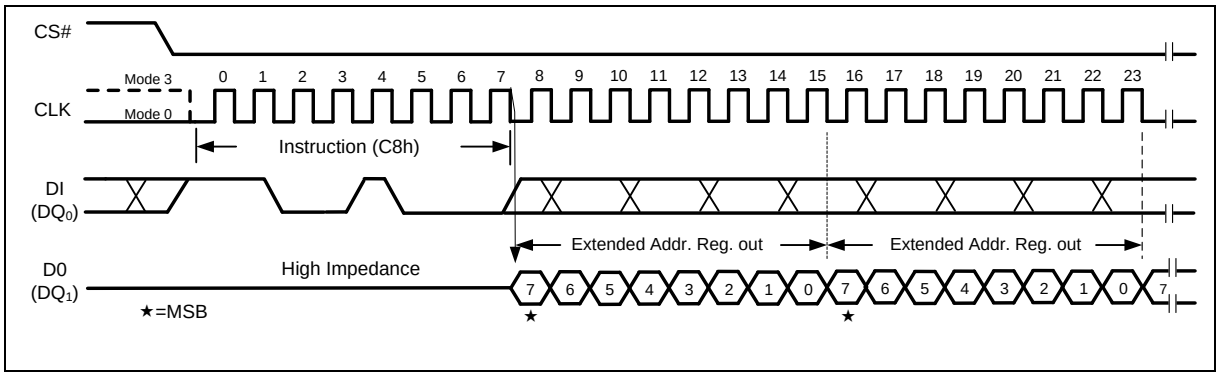


Figure 24 Read Extend Address Register Instruction (SPI Mode)

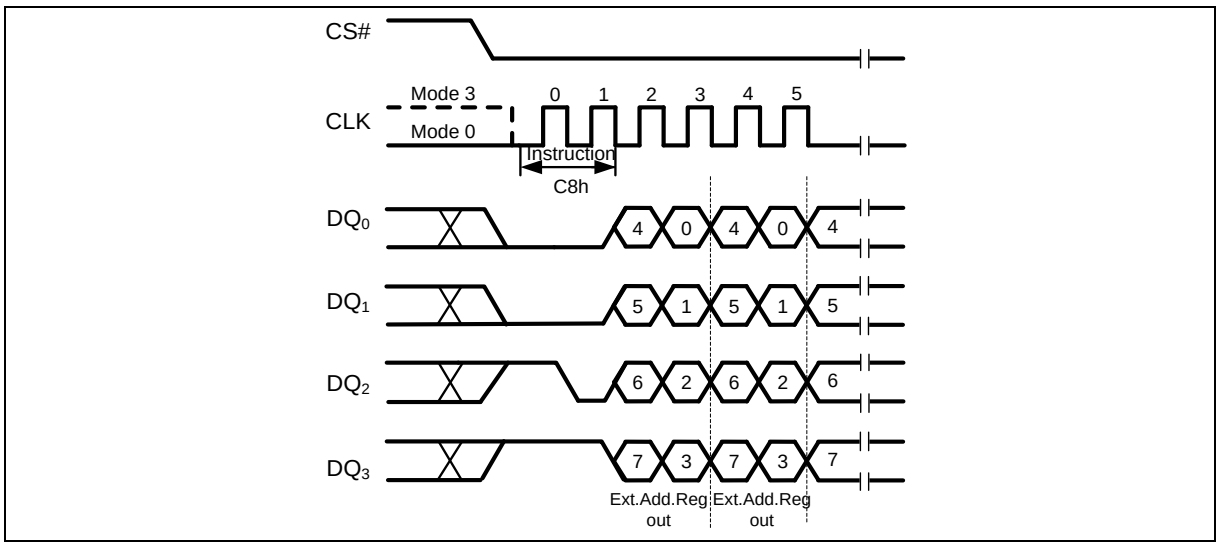


Figure 25 Read Extend Address Register Instruction (QPI Mode)

10.2.7. Write Extended Address Register(C5h)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, send the instruction code “C5h”, and then writing the Extended Address Register data byte as illustrated in.Figure 26

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

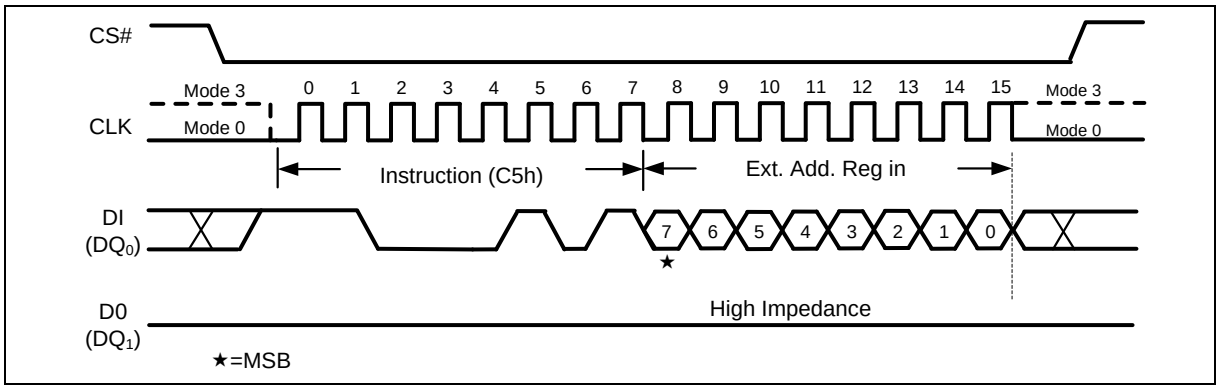


Figure 26 Write Extend Address Register Instruction (SPI Mode)

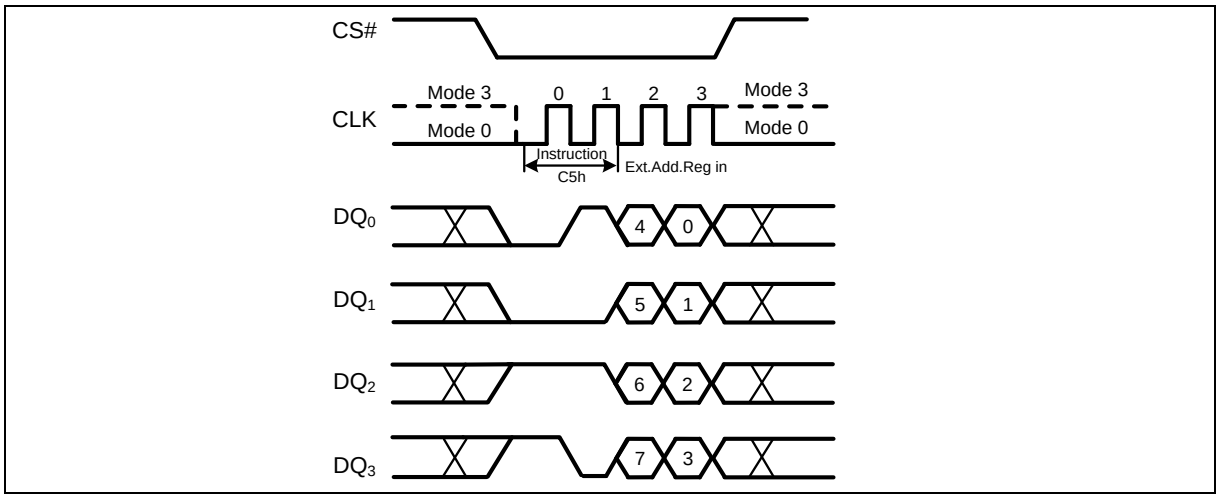


Figure 27 Write Extend Address Register Instruction (QPI Mode)

10.2.8. Enter 4-Byte Address Mode(B7h)

The Enter 4-Byte Address Mode instruction will allow 32-bit address (A31-A0) to be used to access the memory array beyong 128Mb. The Enter 4-Byte Address Mode instruction is entered by driving CS# low, shifting the instruction code “B7h” into the DI pin and then driving CS# high.

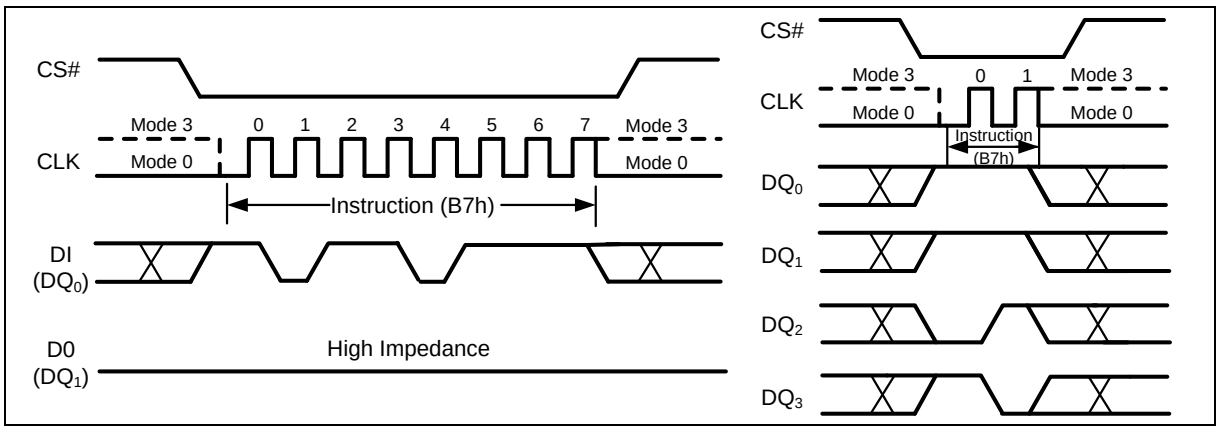


Figure 28 Enter 4-Byte Address Mode Instruction for SPI Mode (left) or QPI Mode (right)

10.2.9. Exit 4-Byte Address Mode(E9h)

In order to be backward compatible, the Exit 4-Byte Address Mode instruction will only allow 24-bit address (A23-A0) to be used to access the memory array up to 128Mb. The Extended Address Register must be used to access the memory array beyong 128Mb. The Exit 4-Byte Address Mode instruction is entered by driving CS# low, shifting the instruction code “E9h” into the DI pin and then driving CS# high.

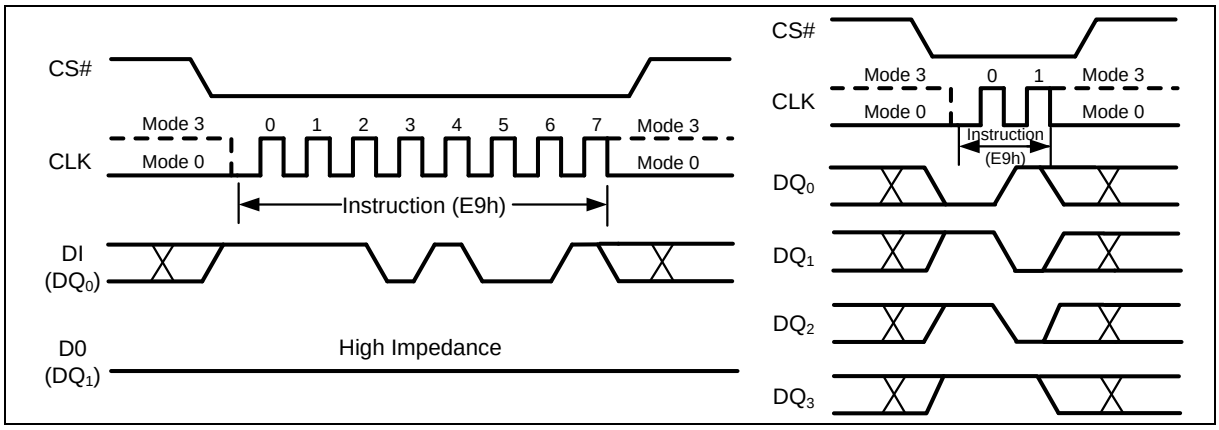


Figure 29 Exit 4-Byte Address Mode Instruction for SPI Mode (left) or QPI Mode (right)

10.2.10. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 32/24-bit address A31/A23-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in Figure 30. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP =1) the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see “11.6 AC Electrical Characteristics”).

The Read Data (03h) instruction is only supported in Standard SPI mode.

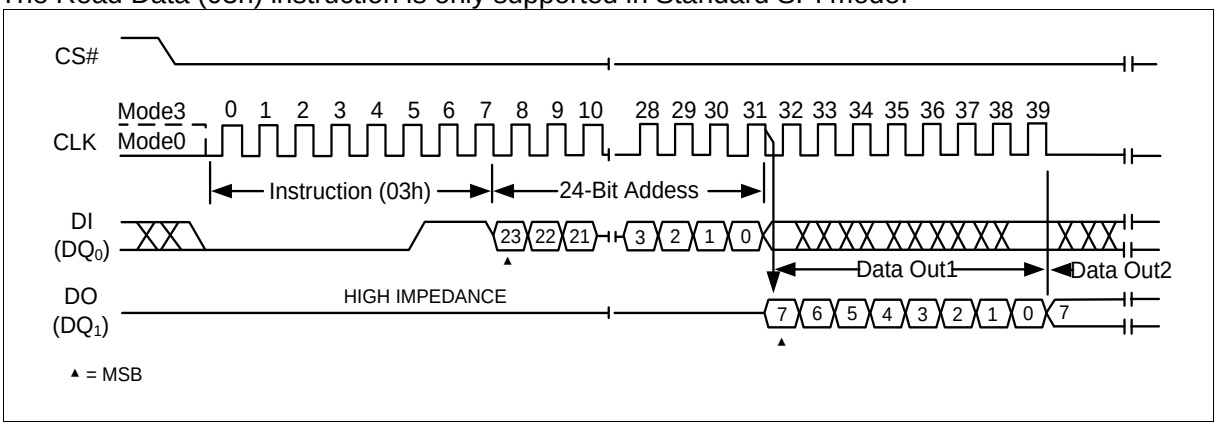


Figure 30 Read Data Instruction (SPI Mode only)

10.2.11. Read Data with 4-Byte Address(13h)

The Read Data with 4-Byte Address instruction is similar to the Read Data (03h) instruction. Instead of 24-bit address, 32-bit address is needed following the instruction code 13h. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always requir 32-bit address to access the entire 256Mb memory.

The Read Data with 4-Byte Address instruction sequence is shown in Figure 31. If this instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects in the current cycle. The Read Data with 4-Byte Address instruction allows clock rates from D.C. to a maximum of f_R (see "11.6 AC Electrical Characteristics").

The Read Data with 4-Byte Address (13h) instruction is only supported in Standard SPI mode.

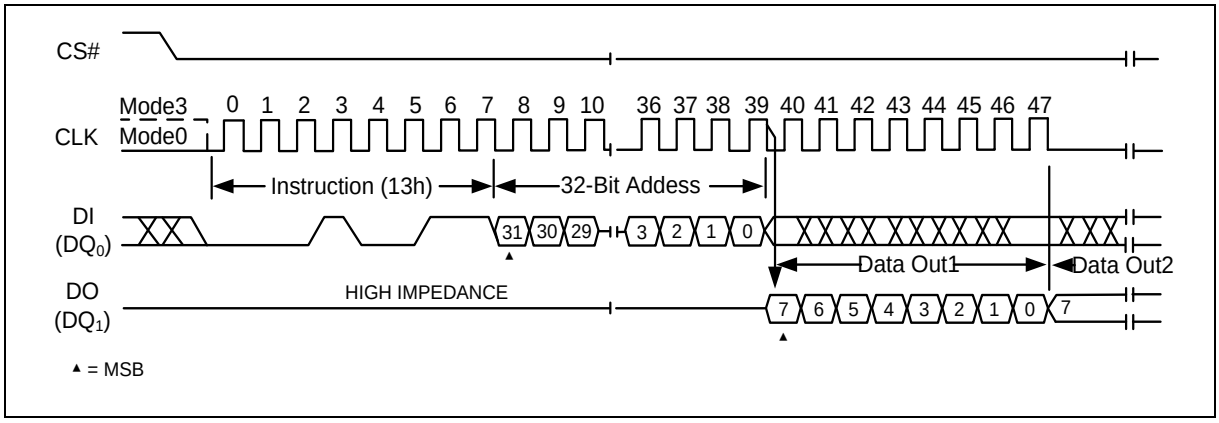


Figure 31 Read Data with 4-Byte Address Instruction (SPI Mode only)

10.2.12. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see "11.6 AC Electrical Characteristics"). This is accomplished by adding eight "dummy" clocks after the 32/24-bit address as shown in Figure 32. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a "don't care".

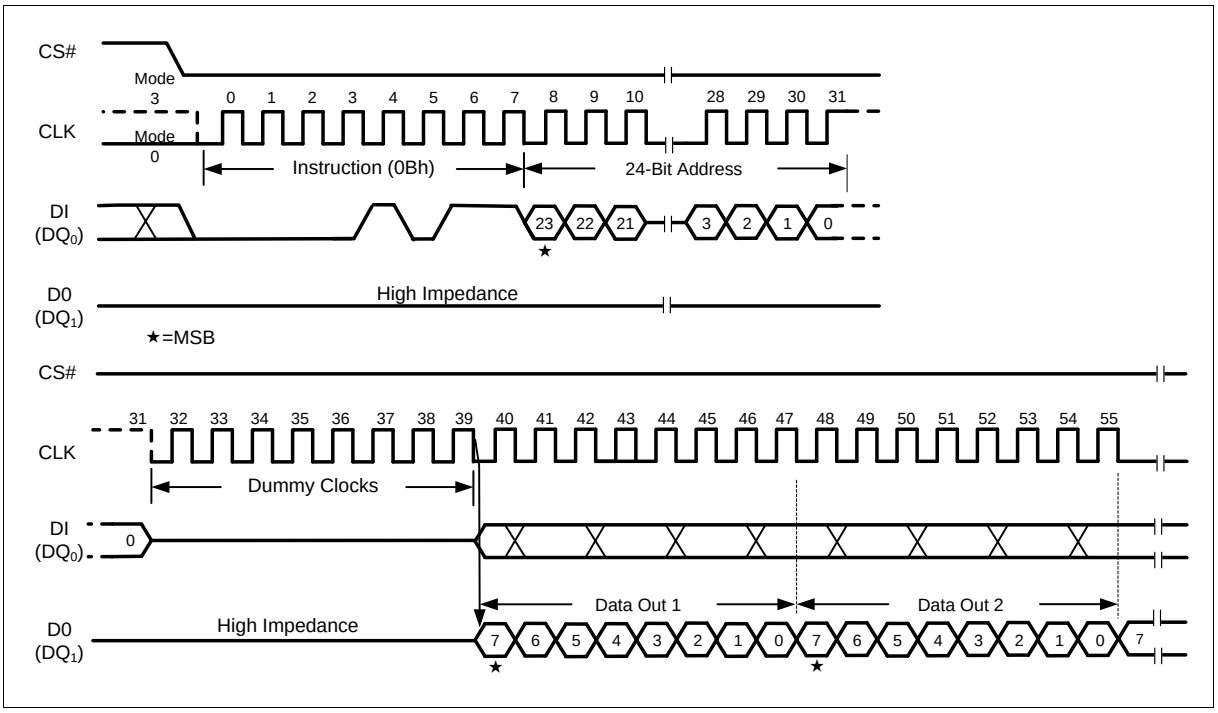


Figure 32 Fast Read Instruction (SPI Mode)

Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting and LC bits in SR3, the number of dummy clocks can be configured as either 2, 4, 6, 8, 10 or 12.

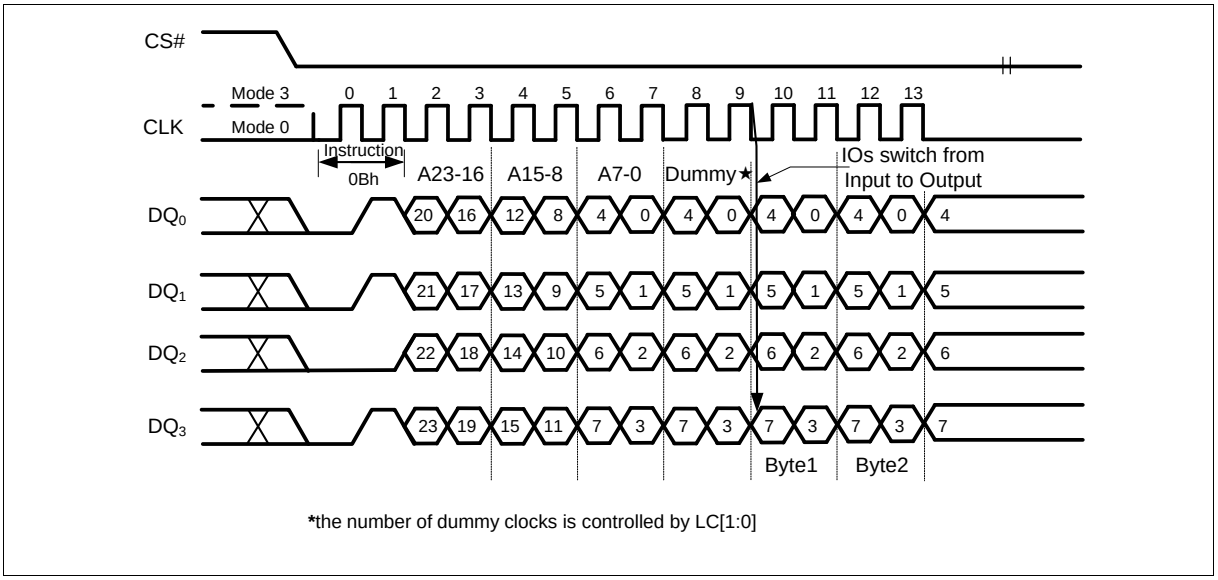


Figure 33 Fast Read Instruction (QPI Mode)

10.2.13. Fast Read with 4-Byte Address (0Ch)

The Fast Read with 4-Byte Address instruction is similar to the Fast Read instruction except that it require 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode. The Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

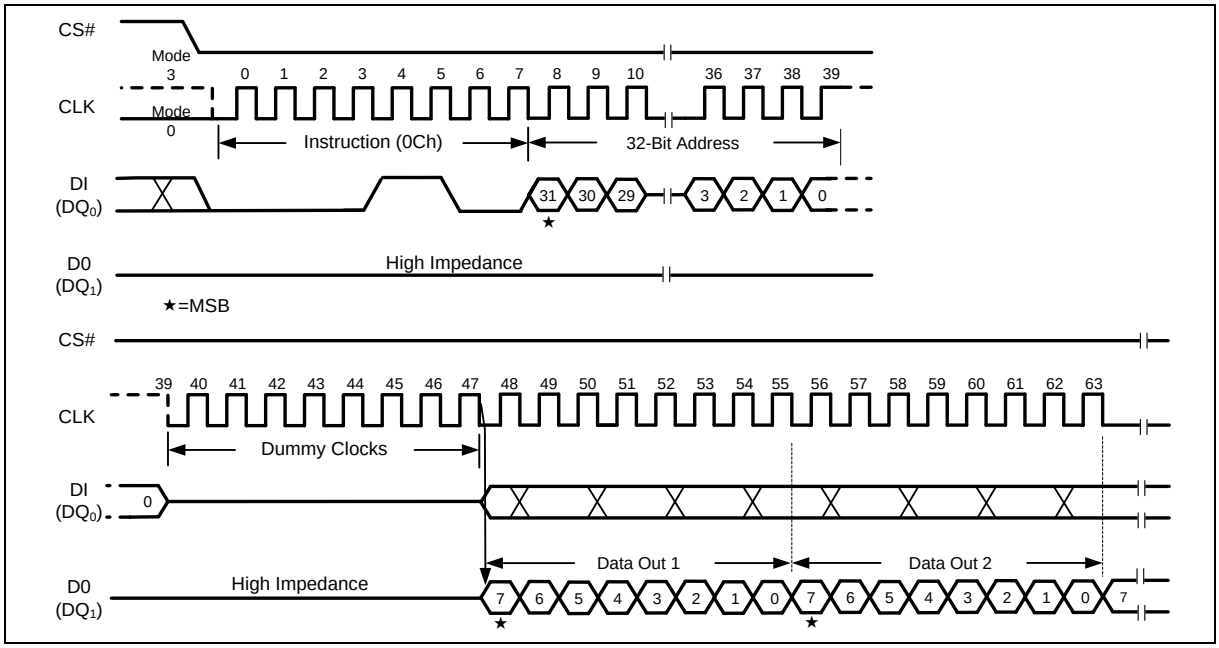


Figure 34 Fast Read Data with 4-Byte Address Instruction (SPI Mode)

Fast Read (0Ch) with 4-Byte Address in QPI Mode

The Fast Read with 4-Byte Address instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting and LC bits in SR3, the number of dummy clocks can be configured as either 2, 4, 6, 8, 10 or 12.

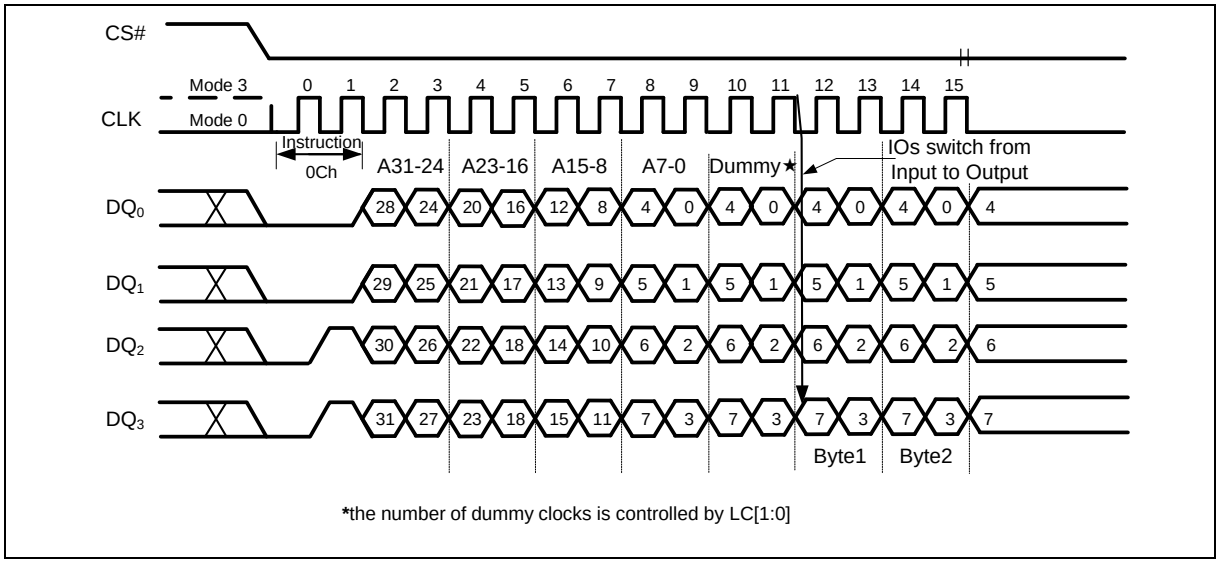


Figure 35 Fast Read Data with 4-Byte Address Instruction (QPI Mode)

10.2.14. DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24/32-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding 6/8/10/12 dummy clocks set by LC bits in SR3 after the 24/32-bit address. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

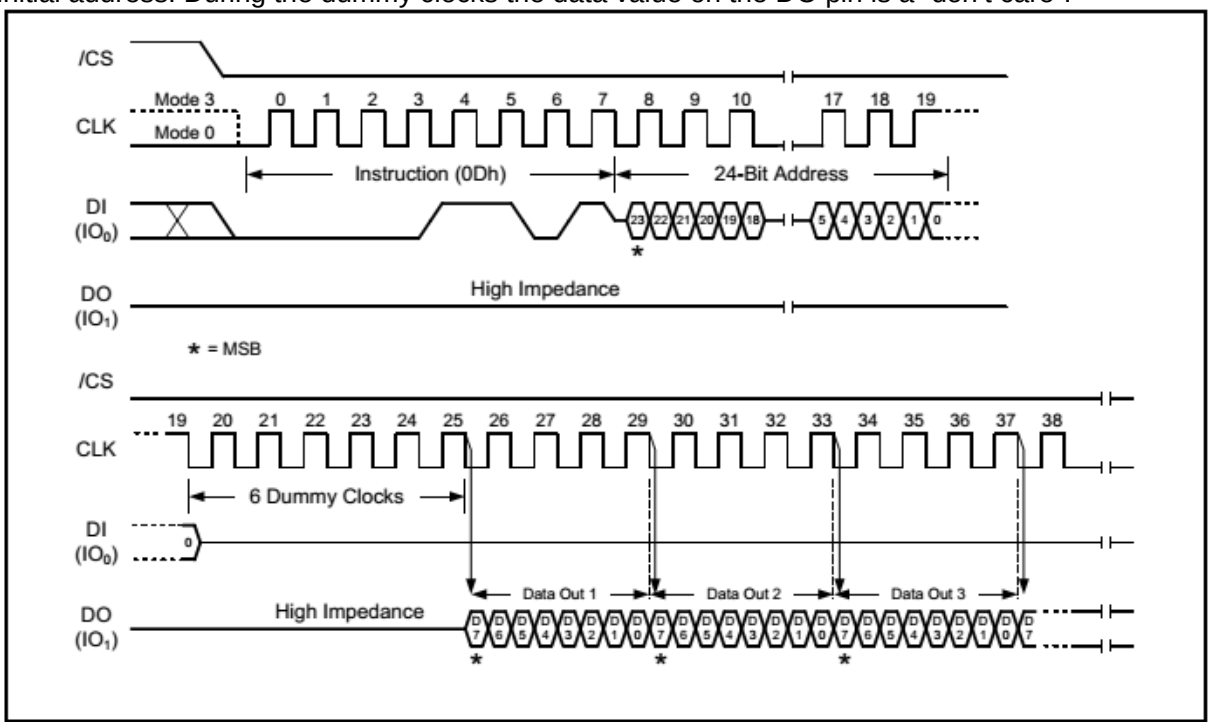


Figure 36 DTR Fast Read Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

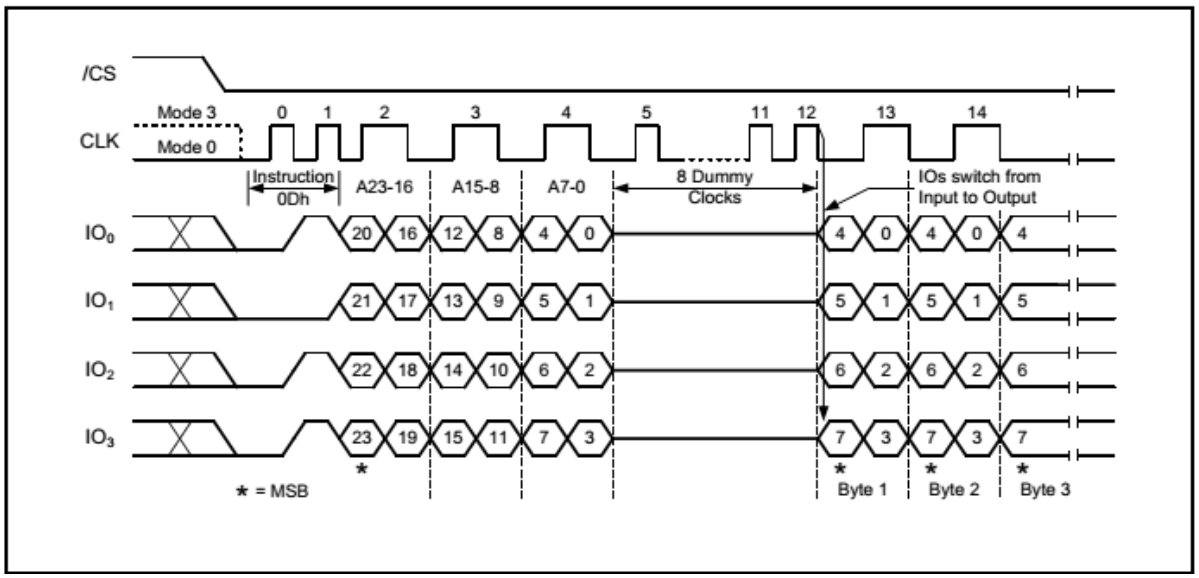


Figure 37 DTR Fast Read Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

10.2.15. DTR Fast Read with 4-Byte Address (0Eh)

The DTR Fast Read with 4-Byte Address instruction is similar to the Fast Read with 4-Byte Address instruction except that the 32-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding 6/8/10/12 dummy clocks set by LC bits in SR3 after the 32-bit address. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a "don't care".

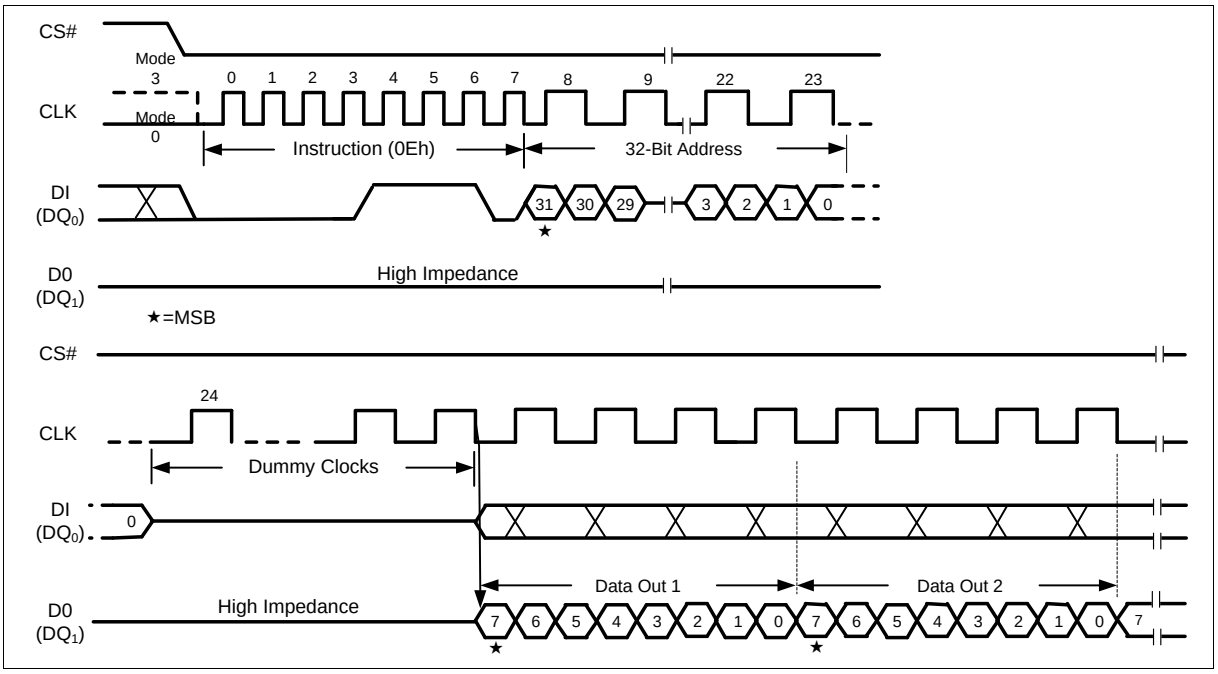


Figure 38 DTR Fast Read with 4-Byte Address Instruction (SPI Mode)

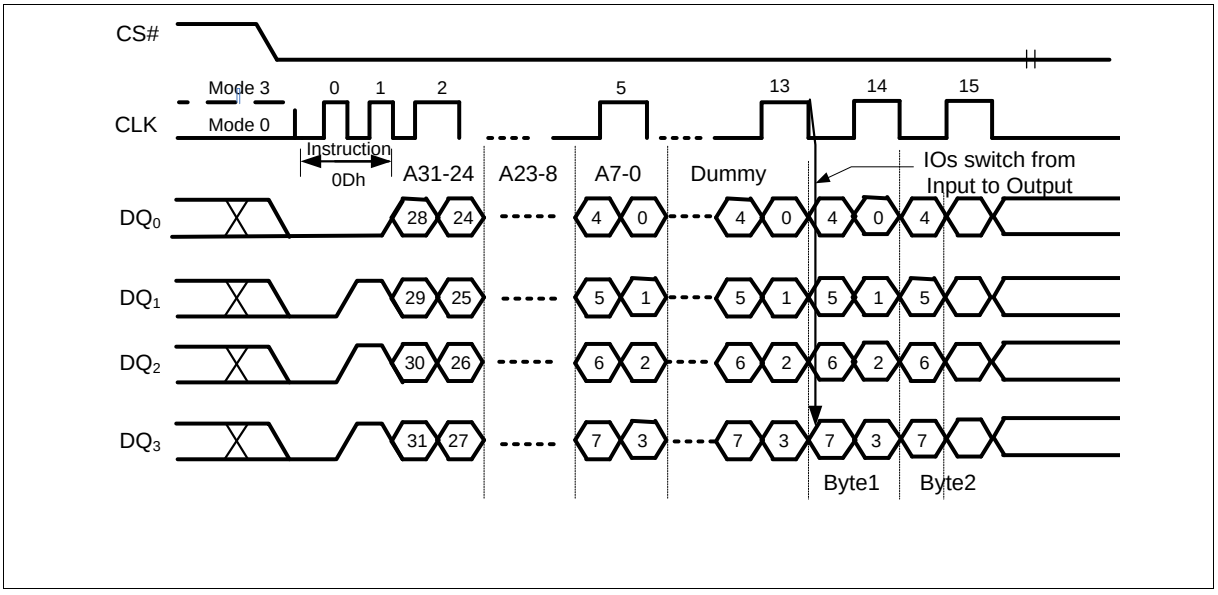


Figure 39 DTR Fast Read with 4-Byte Address Instruction (QPI Mode)

10.2.16. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; DQ_0 and DQ_1. This allows data to be transferred from the FM25Q256I3 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see "11.6 AC Electrical Characteristics"). For Fast Read Dual Output instruction, there are eight dummy cycles required after the 32/24-bit address is shifted into DI before data begins shifting out of DQ_0 and DQ_1. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.

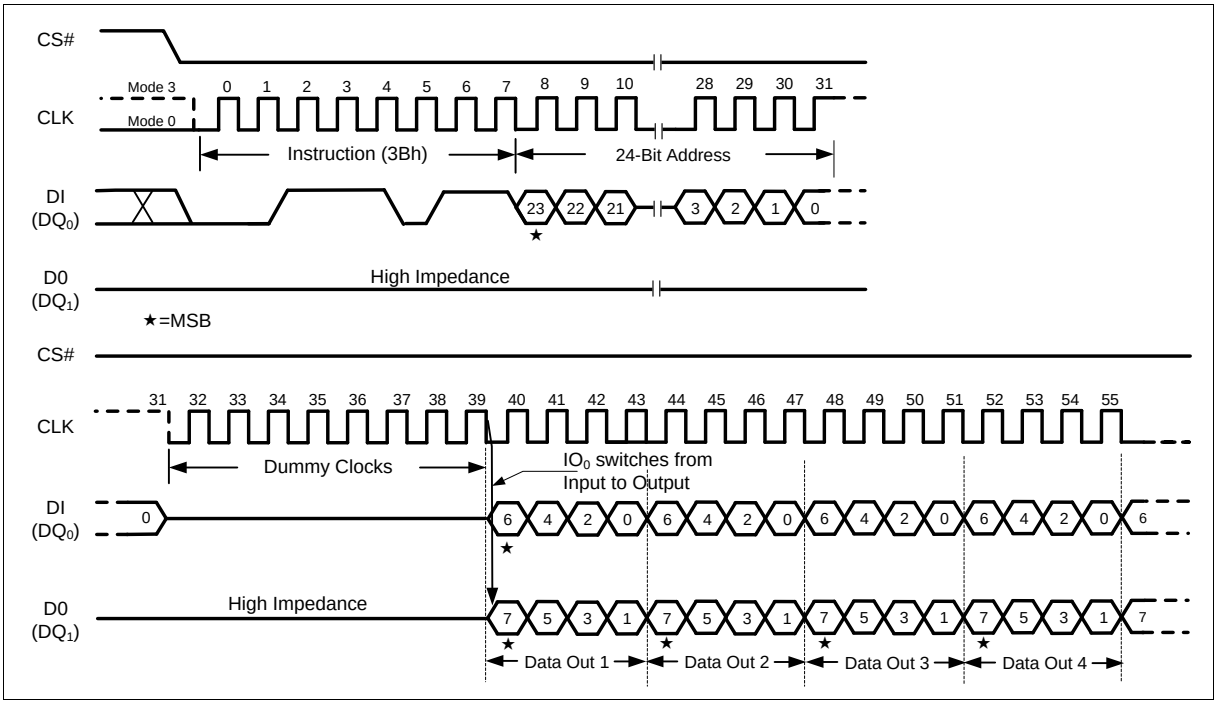


Figure 40 Fast Read Dual Output Instruction (SPI Mode only)

10.2.17. Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output with 4-Byte Address instruction is similar to the Fast Read Dual Output instruction except that if requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the Fast Read Dual output with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read Dual Output with 4-Byte Address (3Ch) instruction is only supported in Standard SPI mode.

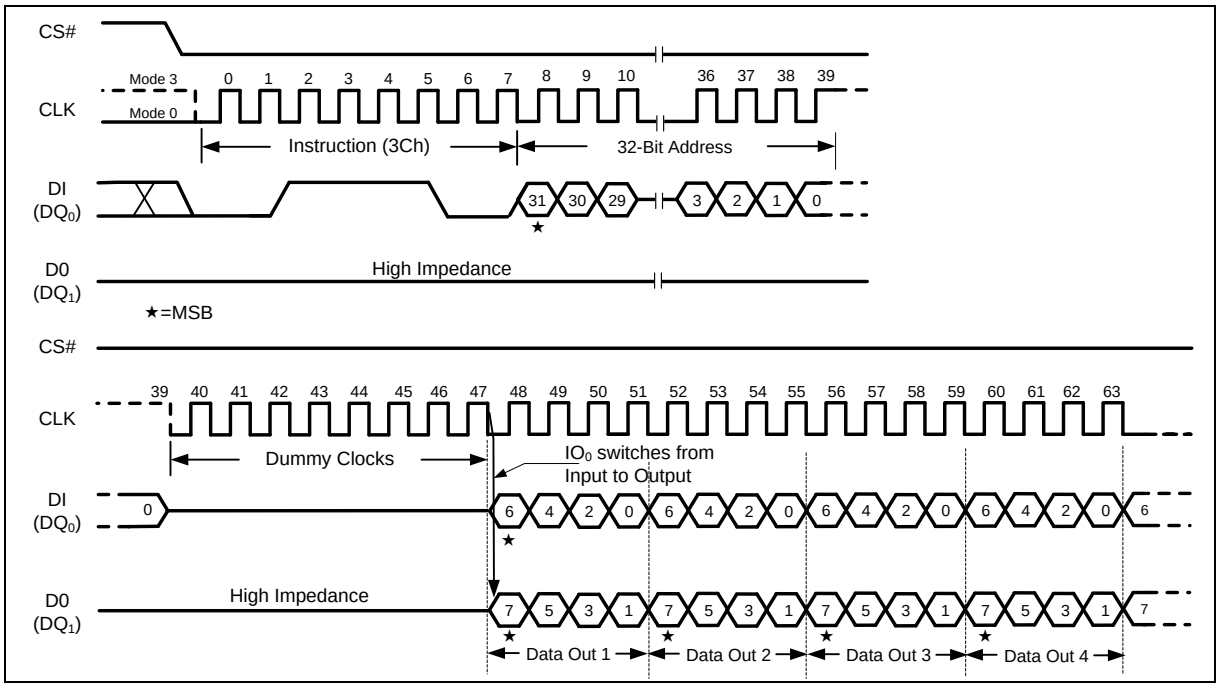


Figure 41 Fast Read Dual Output with 4-Byte Address Instruction (SPI Mode only)

10.2.18. Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, DQ_0, DQ_1, DQ_2, and DQ_3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Instruction (Status Register bit QE must equal 1). The Fast Read Quad Output Instruction allows data to be transferred from the FM25Q256I3 at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see "11.6 AC Electrical Characteristics"). For Fast Read Quad Output instruction, there are eight dummy cycles required after the 32/24-bit address is shifted into DI before data begins shifting out of DQ_0, DQ_1, DQ_2 and DQ_3. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

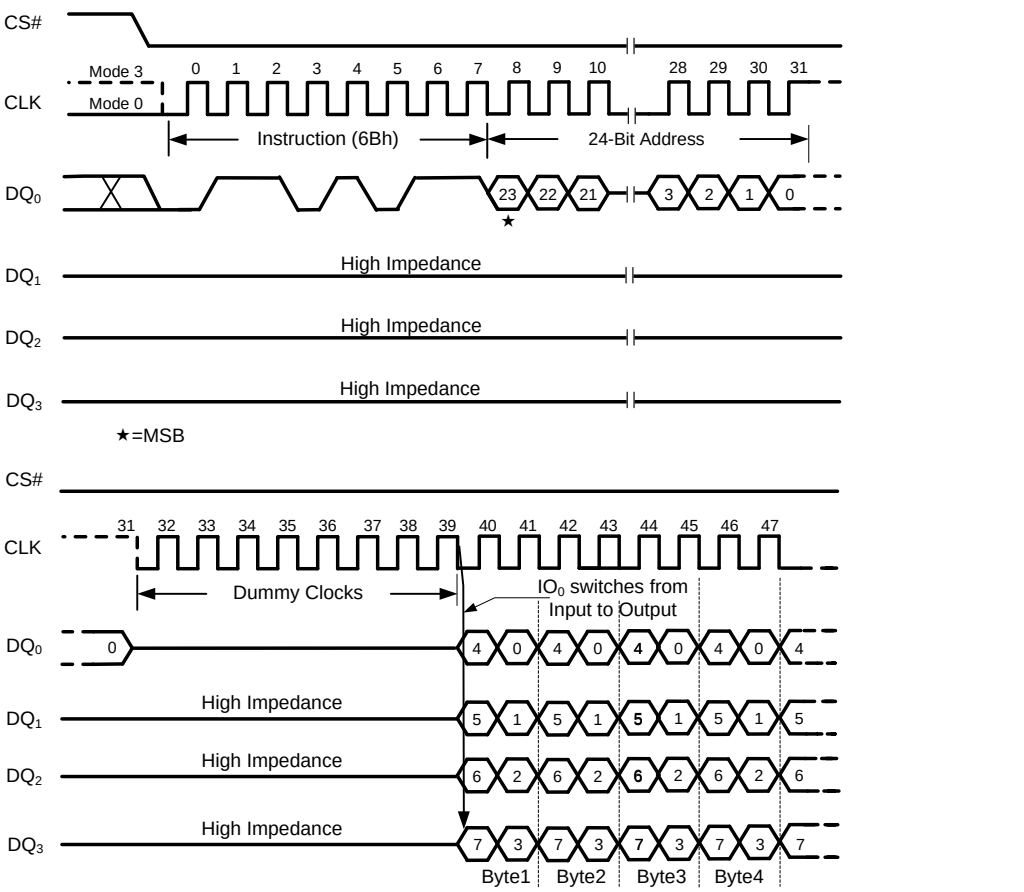


Figure 42 Fast Read Quad Output Instruction (SPI Mode only)

10.2.19. Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output with 4-Byte Address instruction is similar to the Fast Read Quad Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the Fast Read Quad Output with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read Quad Output with 4-Byte Address (6Ch) instruction is only supported in Standard SPI mode.

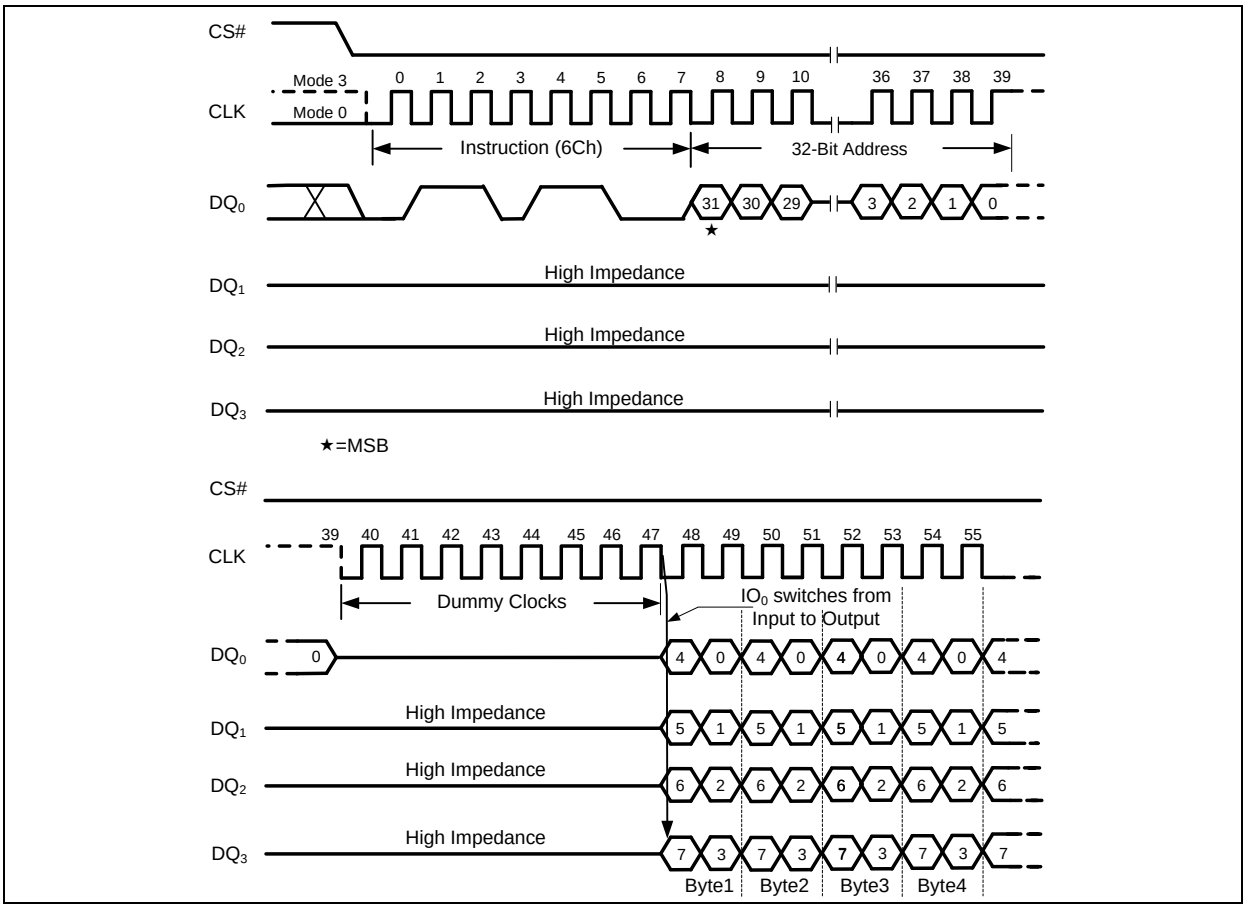


Figure 43 Fast Read Quad Output with 4-Byte Address Instruction (SPI Mode only)

10.2.20. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two I/O pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits A31/A23-A0 two bits per clock. Two continuous mode bit clocks are required in SPI mode prior to the data output, and dummy clock number can be set by LC bits in SR3. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A31/A23-A0, as shown in Figure 44. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 45. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

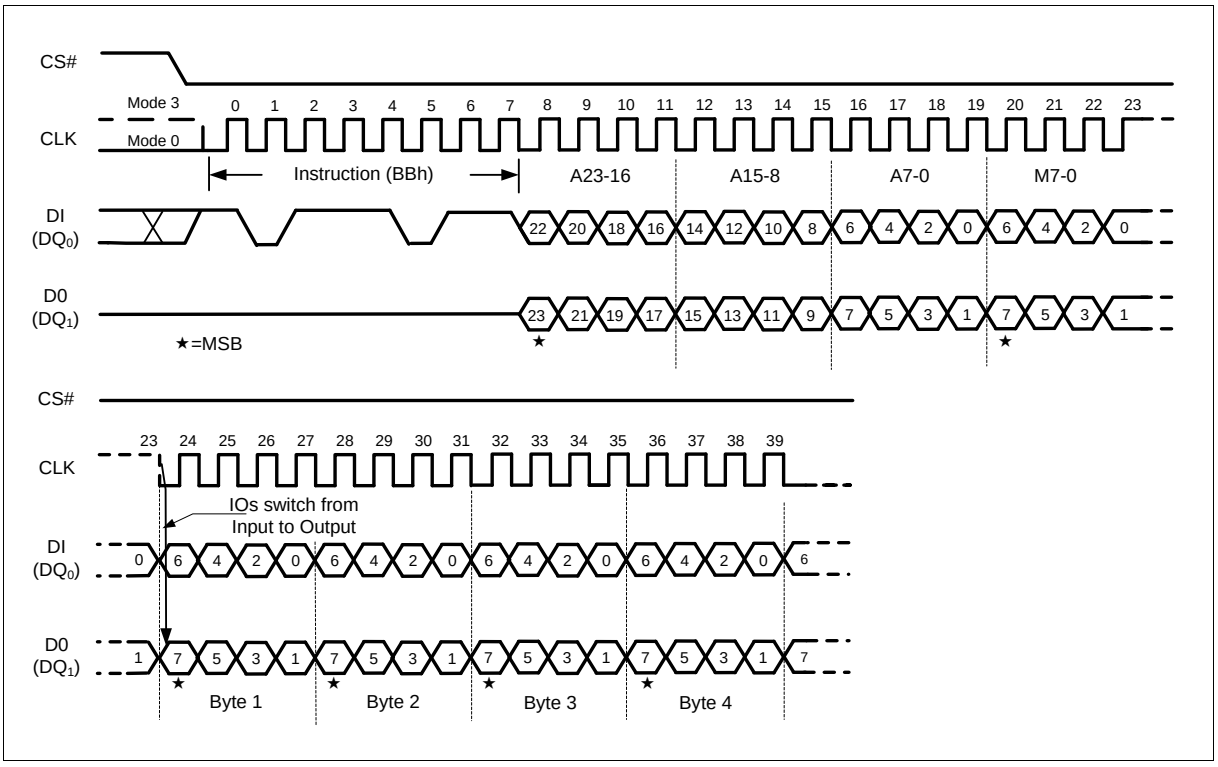


Figure 44 Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

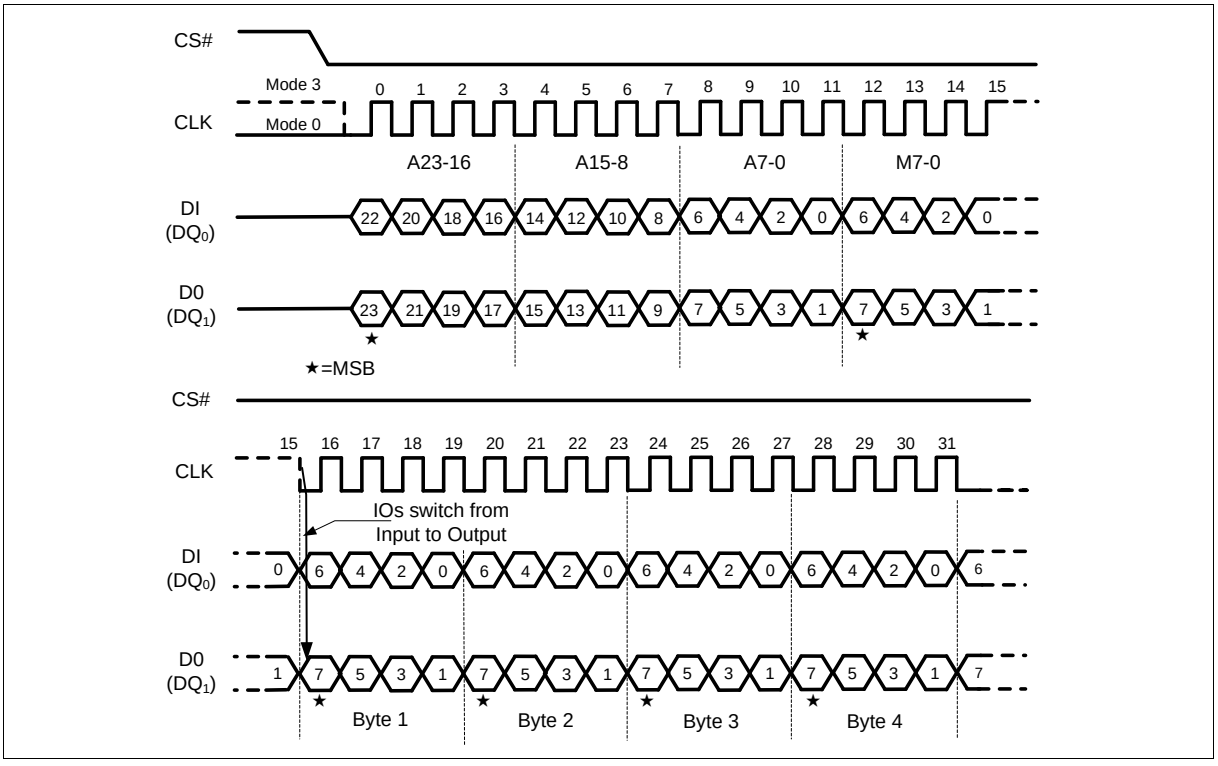


Figure 45 Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

10.2.21. Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O with 4-Byte Address instruction is similar to the Fast Read Dual I/O instruction except that it requires 32-bit address instead of 24-bit address. Two continuous mode bit clocks are required in SPI mode prior to the data output, and dummy clock number can be set by LC bits in SR3. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the Fast Read Dual I/O with 4-Byte Address instruction will always require 32-bit access the entire 256Mb memory.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O with 4-Byte Address instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A31-A0, as shown in Figure 46. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O with 4-Byte Address instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O with 4-Byte Address instruction (after CS# is raised and then lowered) does not require the BCh instruction code, as shown in Figure 47. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

The Fast Read Dual I/O with 4-Byte Address (BCh) instruction is only supported in Standard SPI mode.

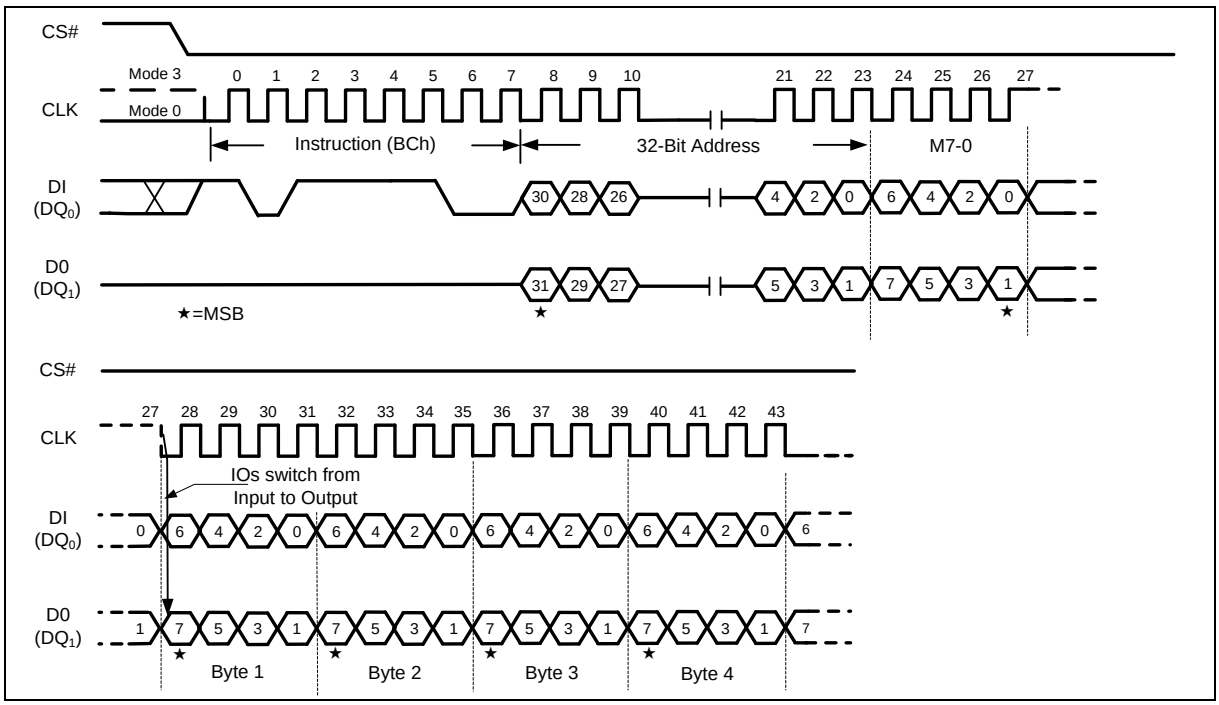


Figure 46 Fast Read Dual I/O with 4-Byte Address Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

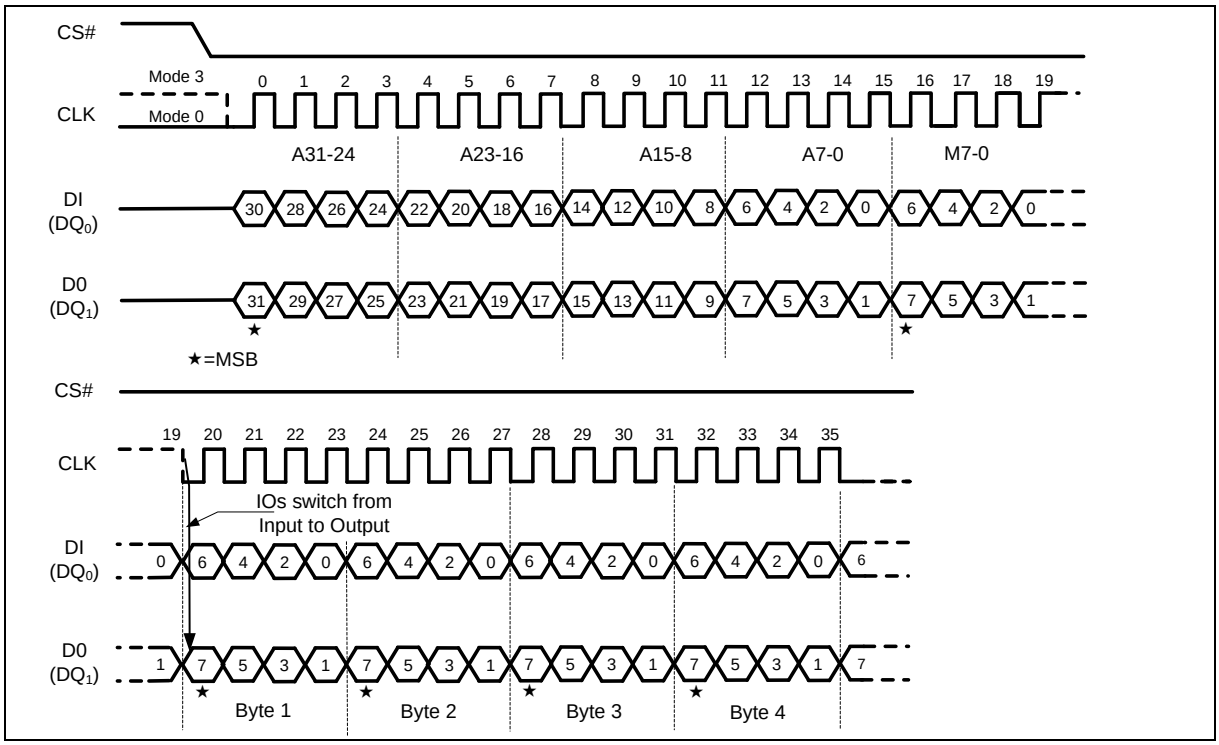


Figure 47 Fast Read Dual I/O with 4-Byte Address Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

10.2.22. DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (BBh) instruction except that the 24/32-bit address input and the data output require DTR (Double Transfer Rate) operation. The 6/8/10/12 dummy clocks set by LC bits in SR3 after the 24/32-bit address are required. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with "Continuous Read Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A31/A23-A0, as shown in Figure 48.The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 49. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

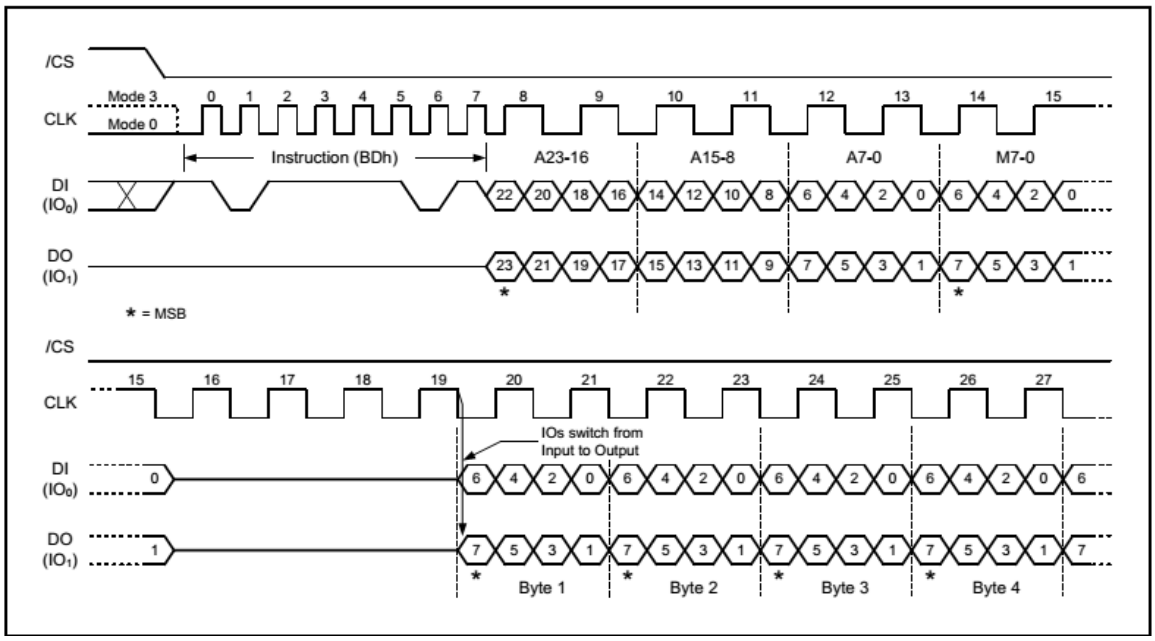


Figure 48 DTR Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

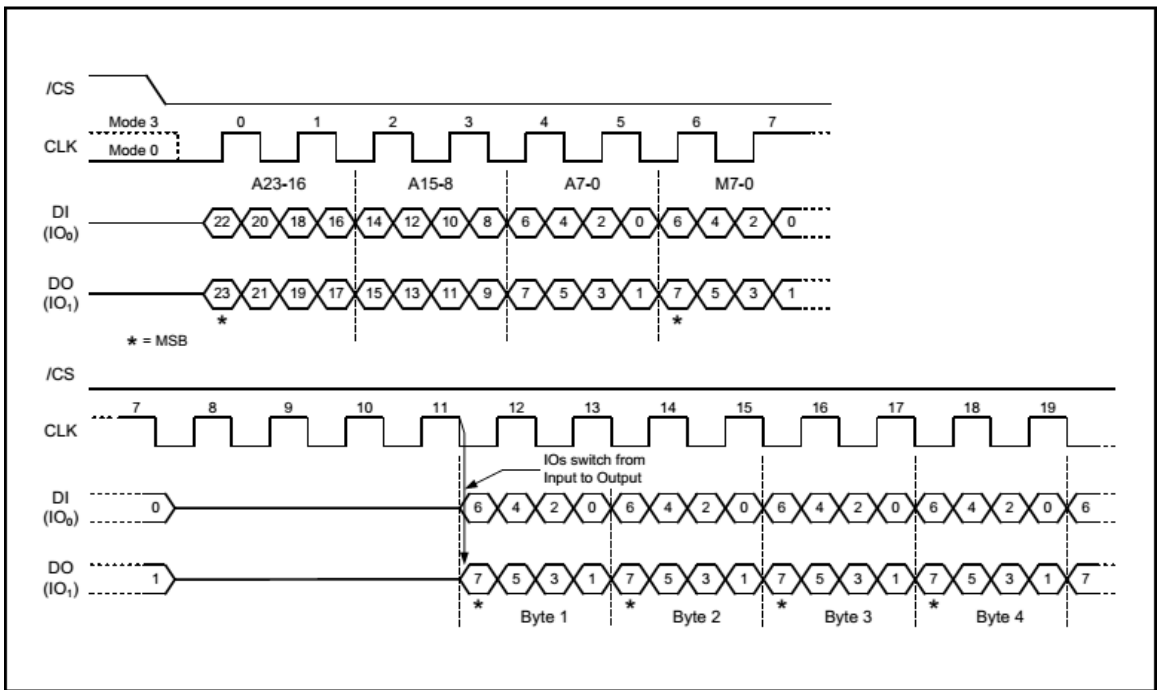


Figure 49 DTR Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

10.2.23. DTR Fast Read Dual I/O with 4-Byte Address (BEh)

The DTR Fast Read Dual I/O with 4-Byte Address (BEh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (BBh) instruction except that the 24/32-bit address input and the data output require DTR (Double Transfer Rate) operation. The 6/8/10/12 dummy clocks set by LC bits in SR3 after the 32-bit

address are required. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

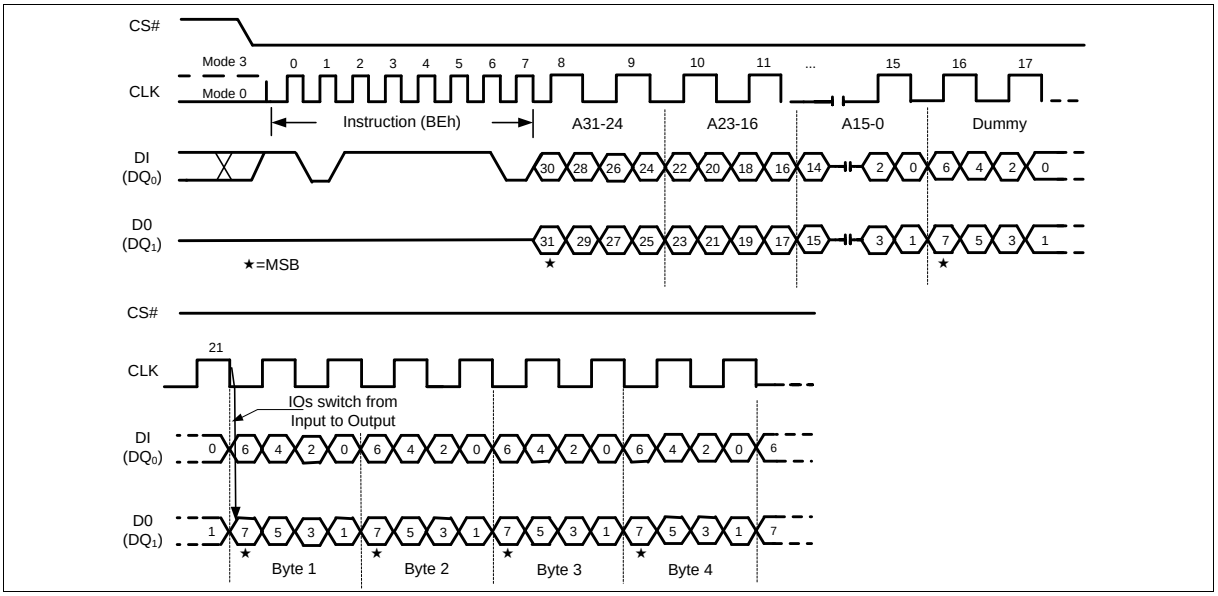


Figure 50 DTR Fast Read Dual I/O with 4-Byte Address Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

10.2.24. Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins DQ_0, DQ_1, DQ_2 and DQ_3. Two continuous mode bit clocks and minimum four Dummy clocks are required in SPI mode prior to the data output, dummy clock number can be set by LC bits in SR3. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A31/A23-A0, as shown in Figure 51. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the EBh instruction code, as shown in Figure 52. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

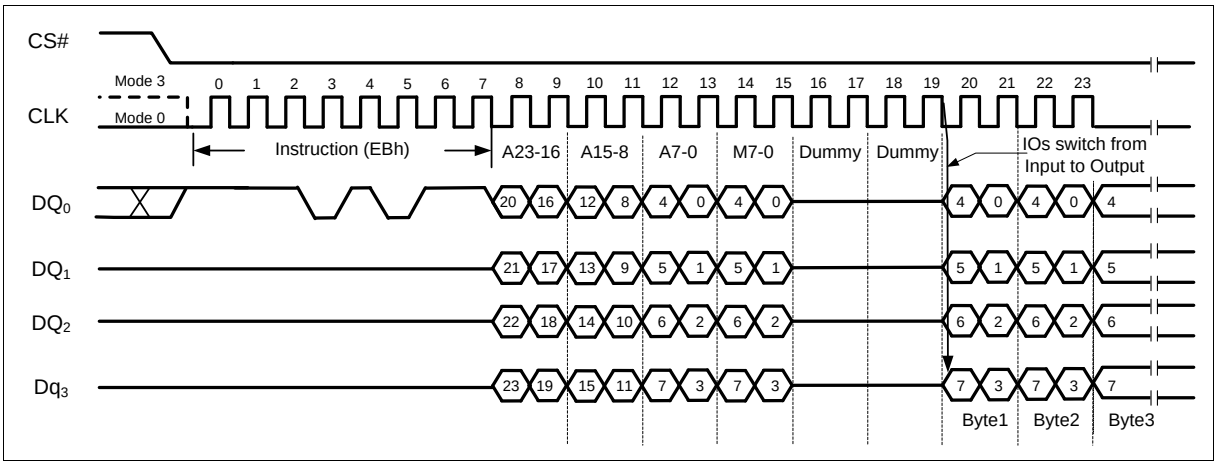


Figure 51 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

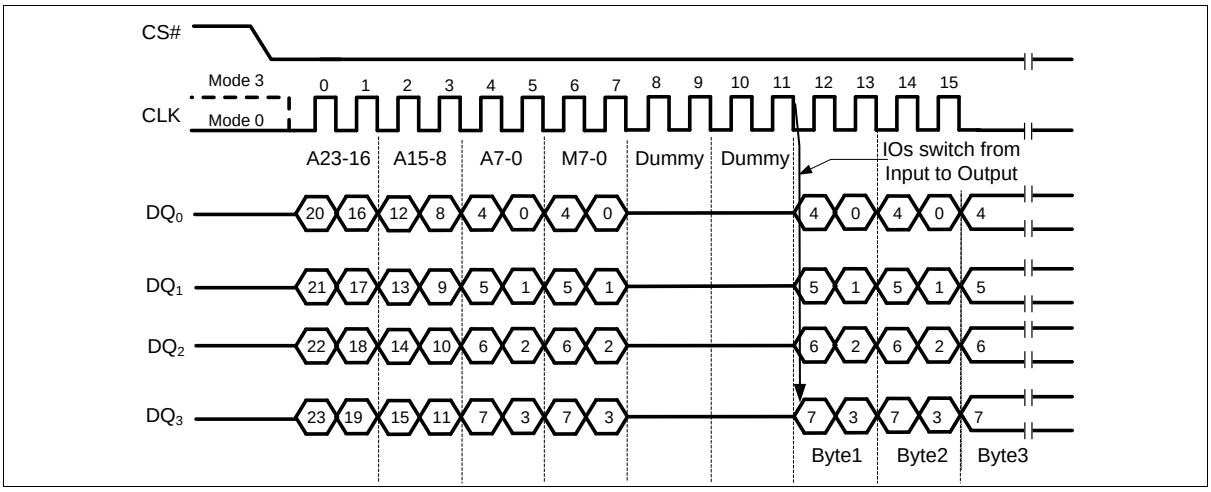


Figure 52 Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "Set Burst with Wrap (77h)" for detail descriptions.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 53. Depending on the Read Parameter Bits P[5:4] setting and LC bits in SR3, the number of dummy clocks can be configured as either 2, 4, 6, 8, 10 or 12.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages for details.

"Wrap Around" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages for details.

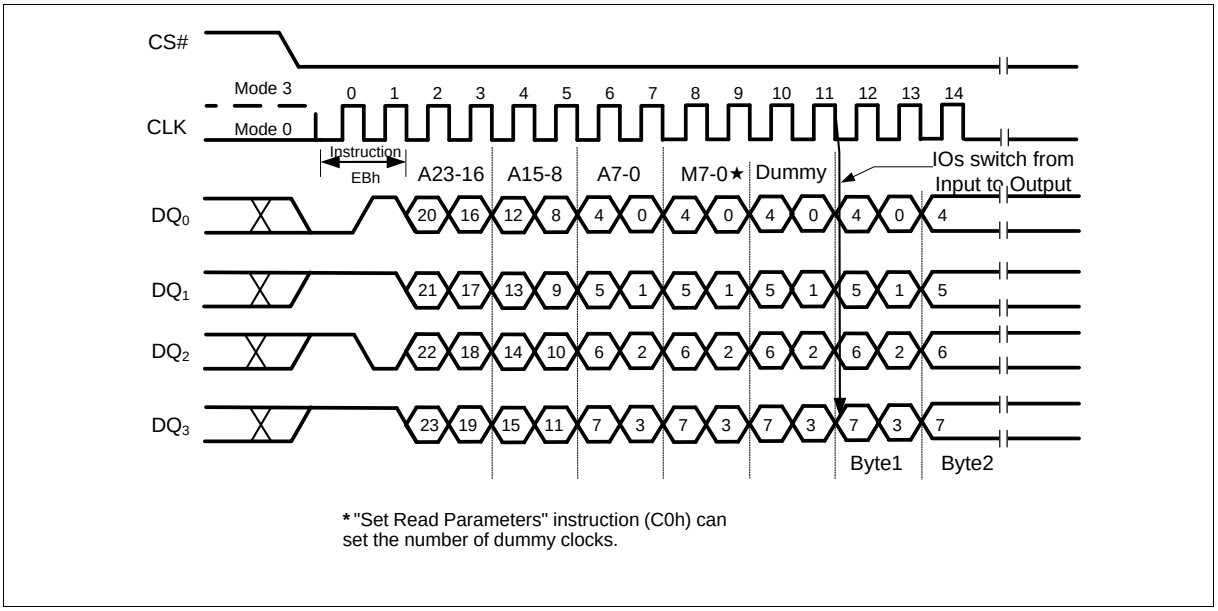


Figure 53 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, QPI Mode)

10.2.25. Fast Read Quad I/O with 4-Byte Address (ECh)

The Fast Read Quad I/O with 4-Byte Address instruction is similar to the Fast Read Quad I/O instruction except that it requires 32-bit address instead of 24-bit address. Two continuous mode bit clocks and minimum four Dummy clocks are required in SPI mode prior to the data output, dummy clock number can be set by LC bits in SR3. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O with 4-Byte Address instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A31-A0, as shown in Figure 54. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the ECh instruction code, as shown in Figure 55. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

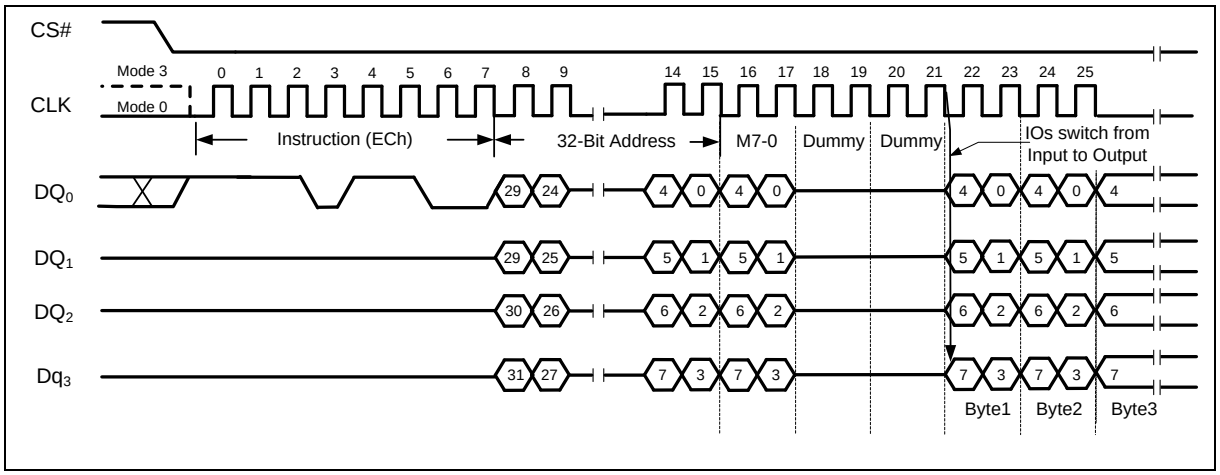


Figure 54 Fast Read Quad I/O with 4-Byte Address Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

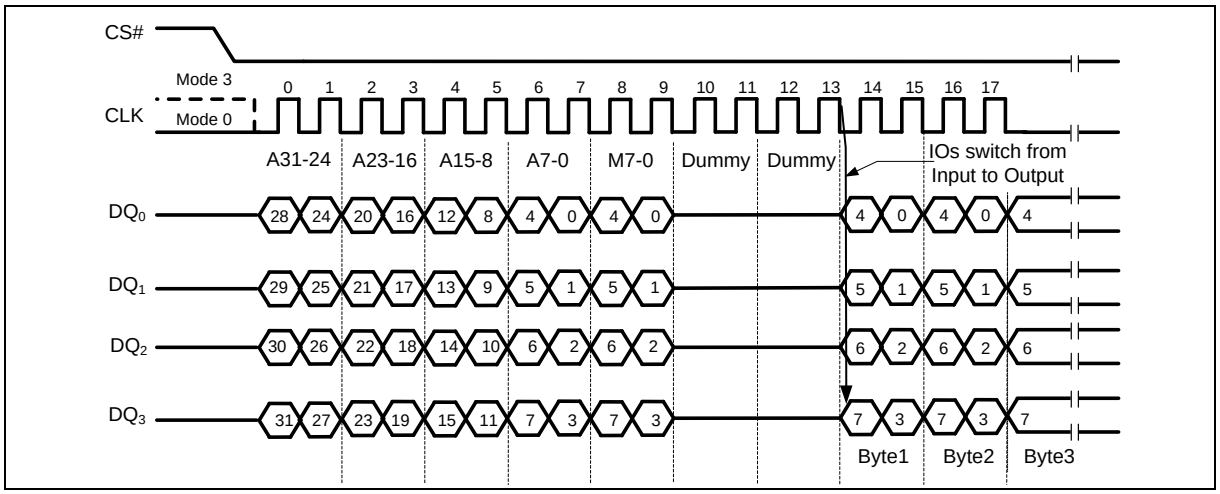


Figure 55 Fast Read Quad I/O with 4-Byte Address Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with 4-Byte Address with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O with 4-Byte Address instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to ECh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following ECh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "Set Burst with Wrap (77h)" for detail descriptions.

Fast Read Quad I/O with 4-Byte Address (ECh) in QPI Mode

The Fast Read Quad I/O with 4-Byte Address instruction is also supported in QPI mode, When QPI mode is enabled, Depending on the Read Parameter Bits P[5:4] setting and LC bits in SR3, the number of dummy clocks can be configured as either 2, 4, 6, 8, 10 or 12.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O with 4-Byte Address instruction. Please refer to the description on previous pages for details.

"Wrap Around" feature is also available in QPI mode for Fast Read Quad I/O with 4-Byte Address instruction. Please refer to the description on previous pages for details.

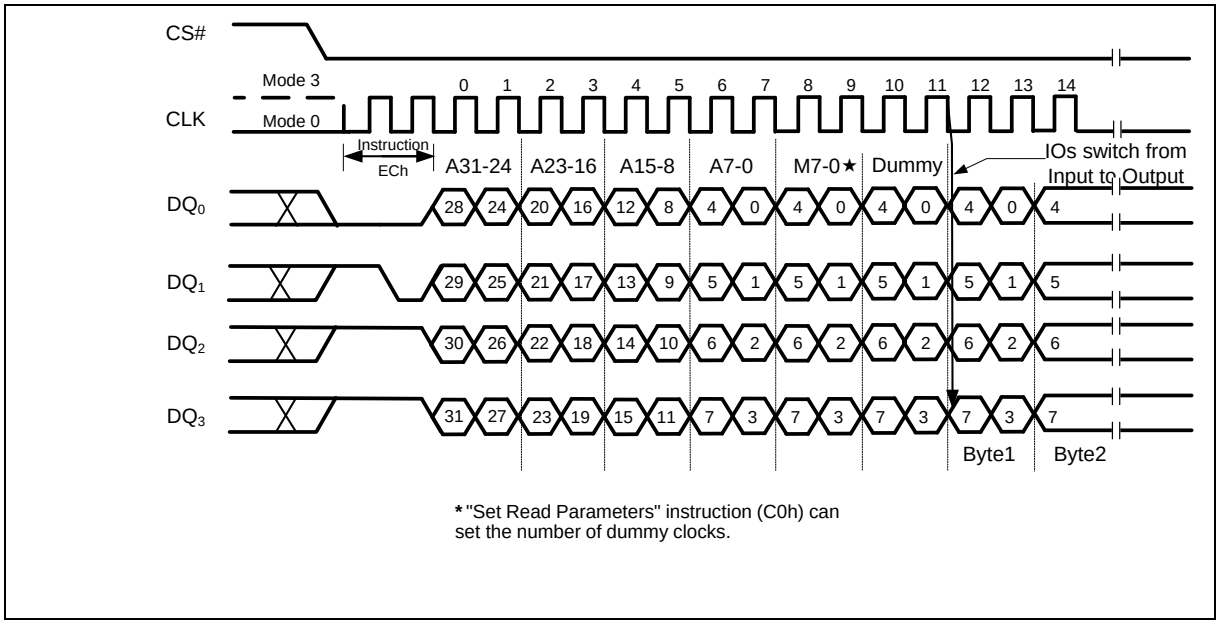


Figure 56 Fast Read Quad I/O with 4-Byte Address Instruction (Initial instruction or previous M5-4≠10, QPI Mode)

10.2.26. DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the 24/32-bit address input and the data output require DTR (Double Transfer Rate) operation. The one continuous mode bit clock and minimum 7 Dummy clocks are required in SPI mode prior to the data output, dummy clock number can be set by LC bits in SR3. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

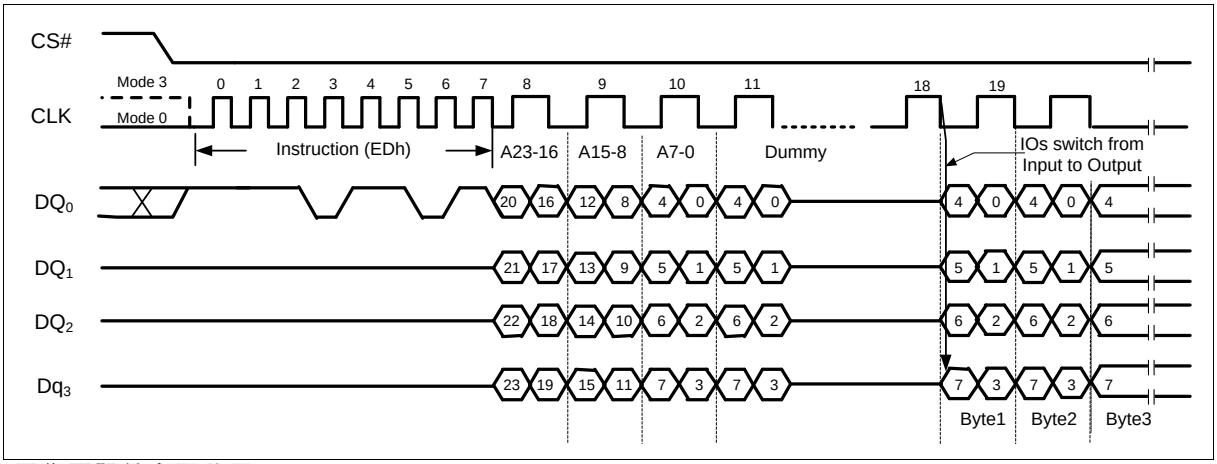


Figure 57 DTR Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

10.2.27. DTR Fast Read Quad I/O with 4-Byte Address (EEh)

The DTR Fast Read Quad I/O with 4-Byte Address (EEh) instruction is similar to the Fast Read Quad I/O (ECh) instruction except that the 24/32-bit address input and the data output require DTR (Double Transfer Rate) operation. The one continuous mode bit clock and minimum 7 Dummy clocks are required in SPI mode prior to the data output, dummy clock number can be set by LC bits in SR3. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

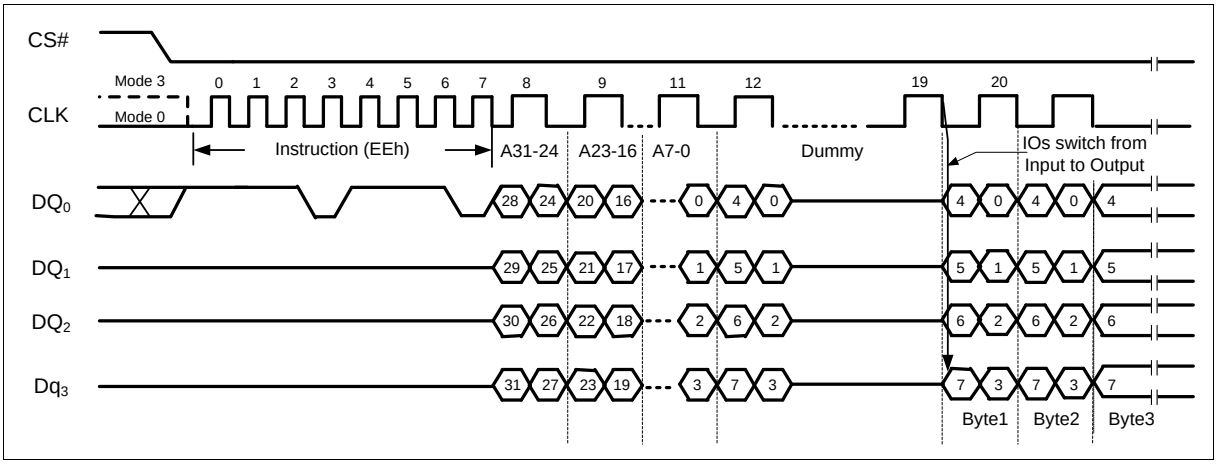


Figure 58 DTR Fast Read Quad I/O with 4-Byte Address Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

10.2.28. Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lowest Address bit (A0) must equal 0, two continuous mode bit clocks and two Dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

Word Read Quad I/O with "Continuous Read Mode"

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A31/A23-A0, as shown in Figure 59. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the E7h instruction code, as shown in Figure 60. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0

for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

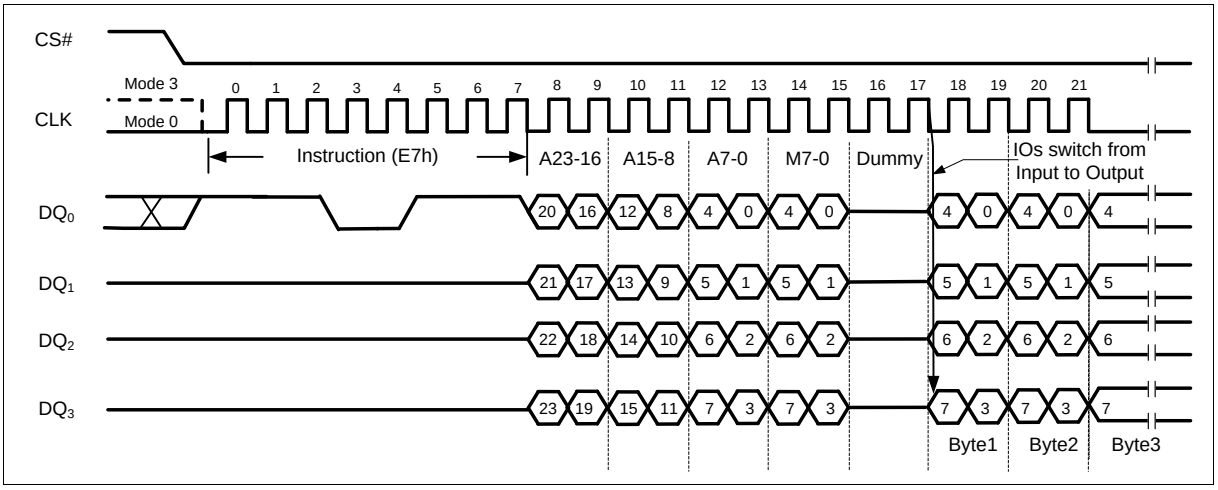


Figure 59 Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

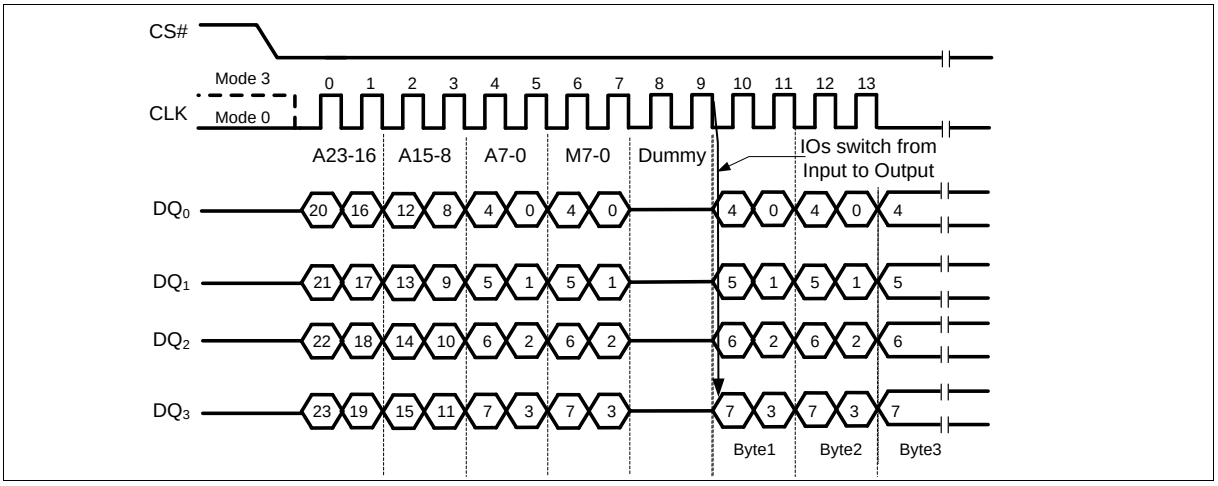


Figure 60 Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "Set Burst with Wrap (77h)" for detail descriptions.

10.2.29. Octal Word Read Quad I/O (E3h)(WEL=0)

The Octal Word Read Quad I/O (E3h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lower four Address bits (A0, A1, A2, A3) must equal 0. As a result, only continuous mode bit clocks are required without any dummy clock, which further reduces the instruction overhead allowing even faster random access for code execution (XIP). The Quad Enable bit (QE) of Status Register-2 must be set to enable the Octal Word Read Quad I/O Instruction.

Octal Word Read Quad I/O with "Continuous Read Mode"

The Octal Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits M7-M0 after the input Address bits A31/A23-A0, as shown in Figure 61. The upper nibble of the (M7-4) controls the length of the next Octal Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the E3h instruction code, as shown in Figure 62. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

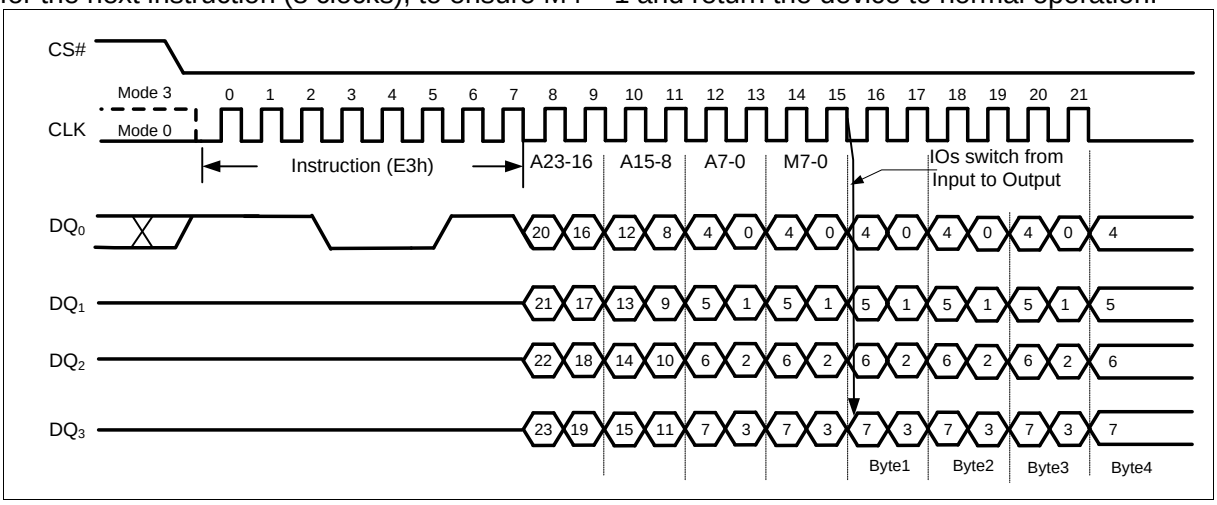


Figure 61 Octal Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

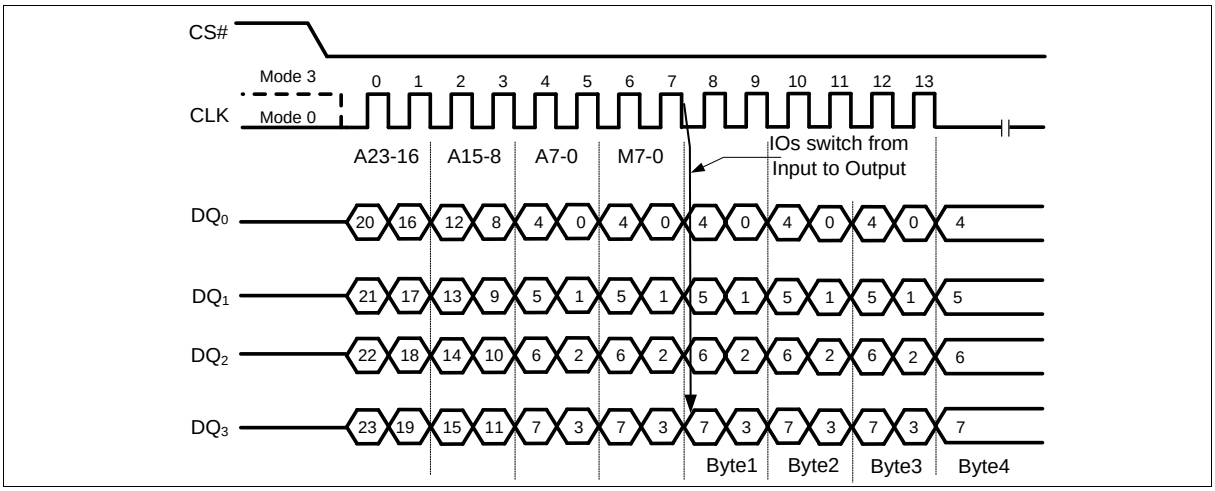


Figure 62 Octal Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

10.2.30. Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) instruction is used in conjunction with "Fast Read Quad I/O" and "Word Read Quad I/O" instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the CS# pin low and then shifting the instruction code "77h" followed by 24/32 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in Figure 63. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "Fast Read Quad I/O" and "Word Read Quad I/O" instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction to reset W4 = 1 prior to any normal Read instructions since FM25Q256I3 does not have a hardware Reset Pin.

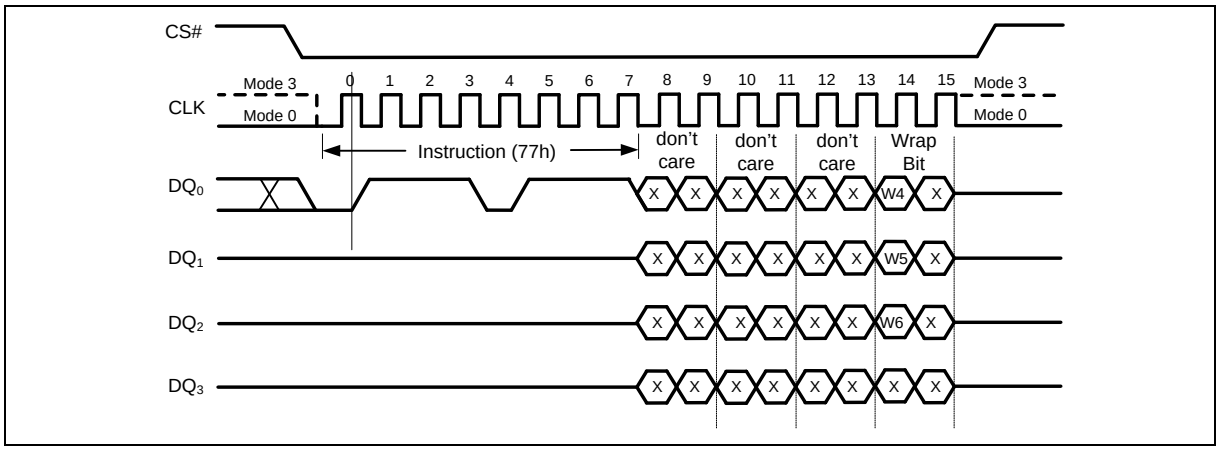


Figure 63 Set Burst with Wrap Instruction for SPI Mode

32-Bit dummy bits are required when the device is operating in 4-Byte Address Mode

10.2.31. Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "02h" followed by a 32/24-bit address A31/A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 64 and Figure 65.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of t_{PP} (See "11.6 AC Electrical Characteristics"). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.

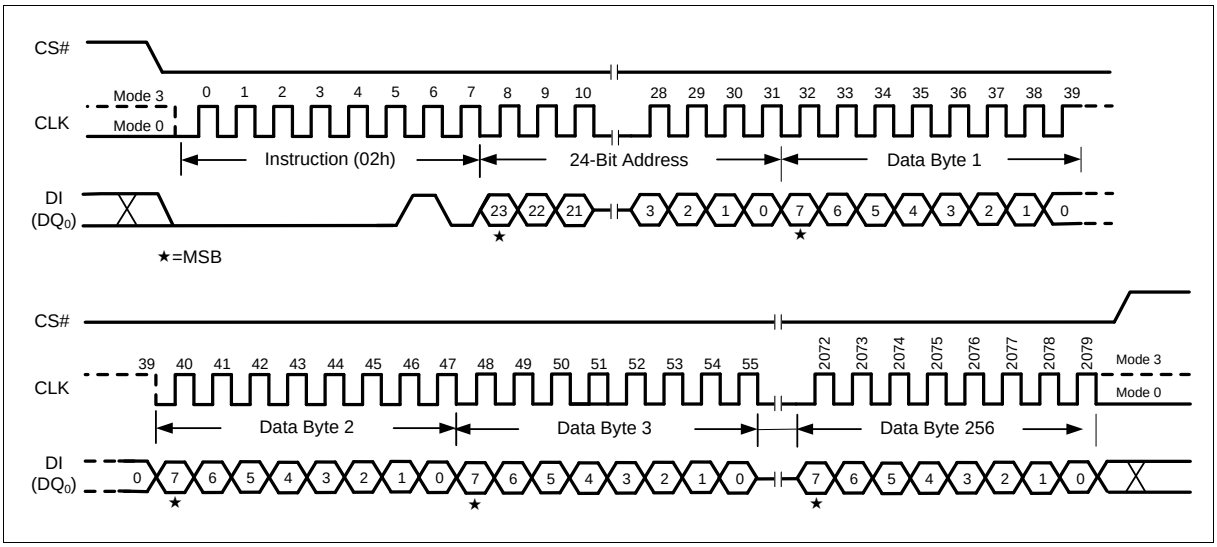


Figure 64 Page Program Instruction (SPI Mode)

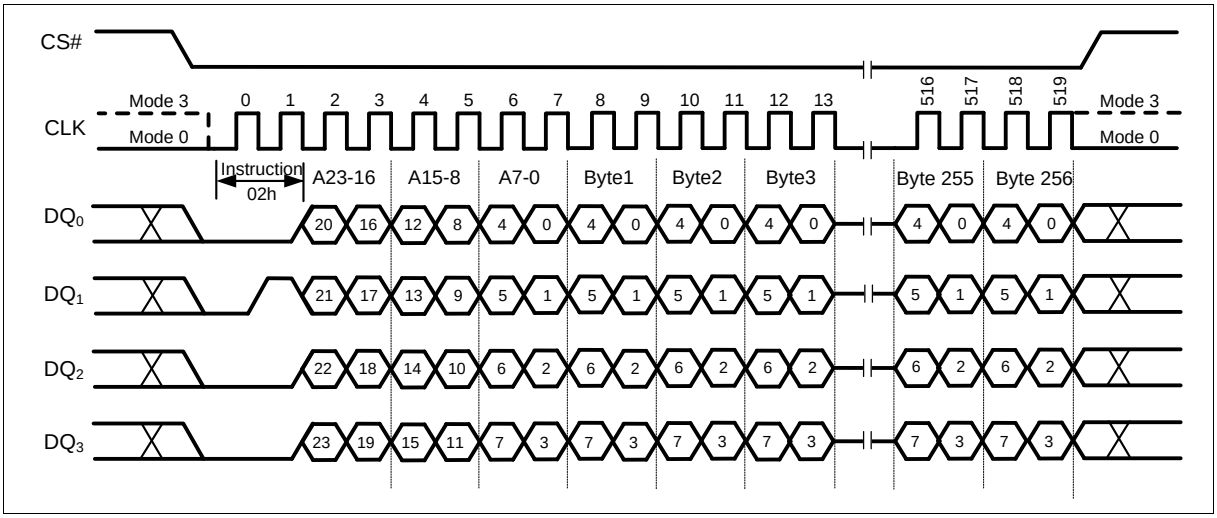


Figure 65 Page Program Instruction (QPI Mode)

10.2.32. Page Program with 4-Byte Address (12h)

The Page Program with 4-Byte Address instruction is similar to the Page Program instruction except that it require 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the Page Program with 4-Byte Address instruction will always require 32 bit address to access the entire 256Mb memory.

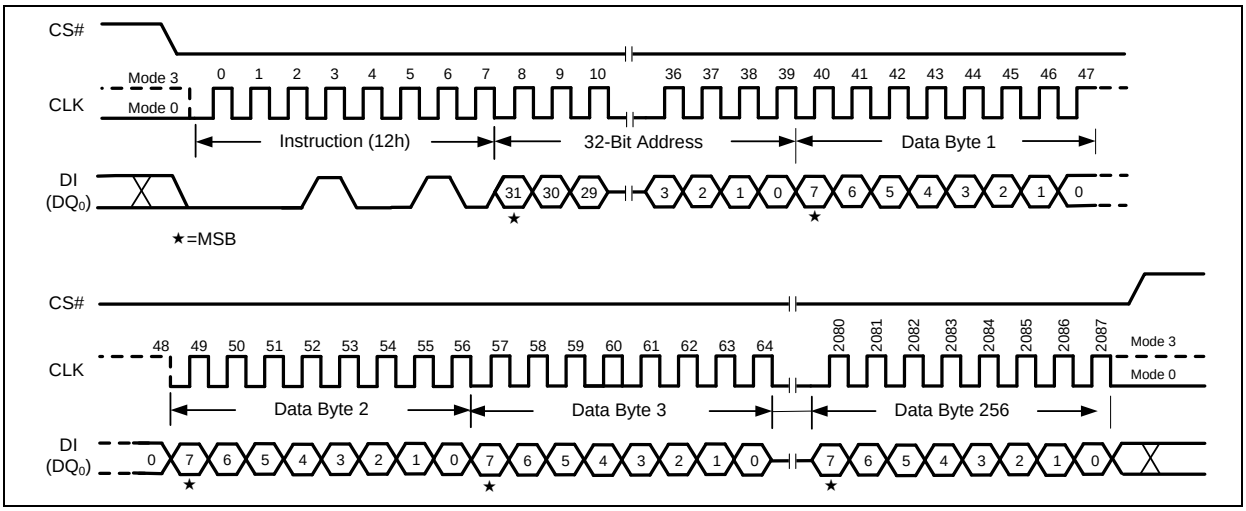


Figure 66 Page Program with 4-Byte Address Instruction (SPI Mode)

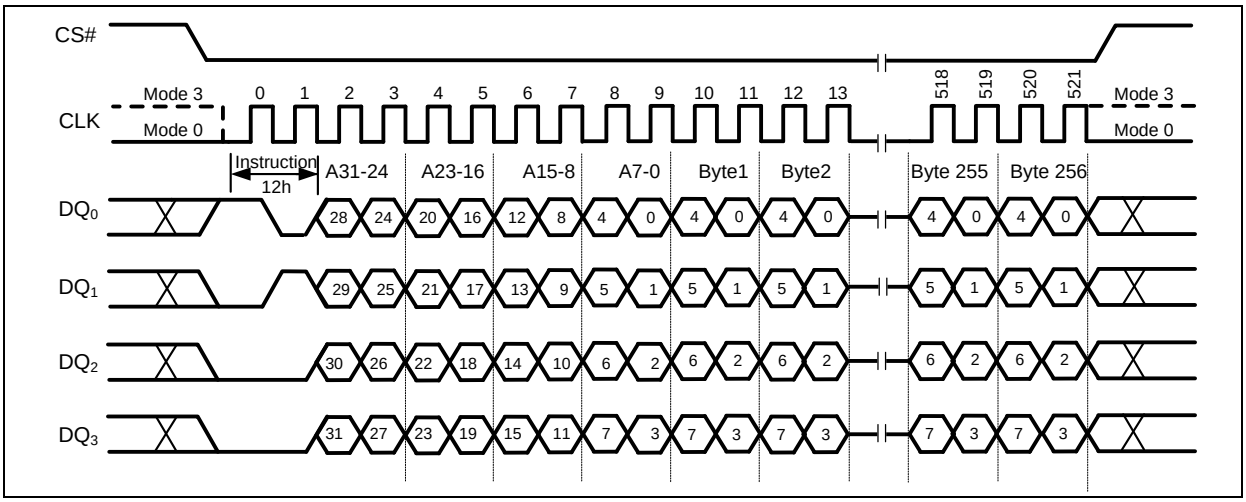


Figure 67 Page Program with 4-Byte Address Instruction (QPI Mode)

10.2.33. Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ_0, DQ_1, DQ_2, and DQ_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “32h” followed by a 32/24-bit address A31/A23-A0 and at least one data byte, into the DQ pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 68.

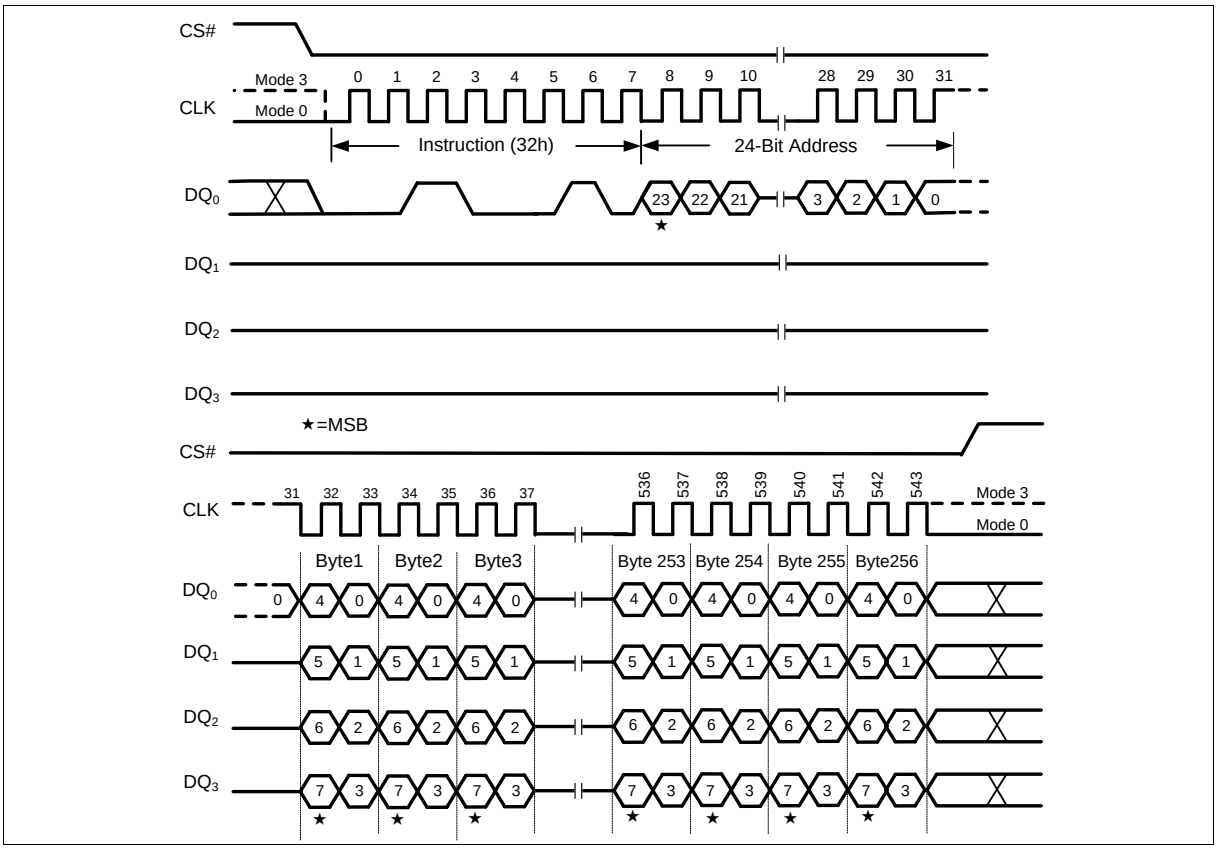


Figure 68 Quad Input Page Program Instruction (SPI Mode only)

10.2.34. Quad Input Page Program with 4-Byte Address (34h)

The Quad Input Page Program with 4-Byte Address instruction is similar to the Quad Input Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the Quad Input Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

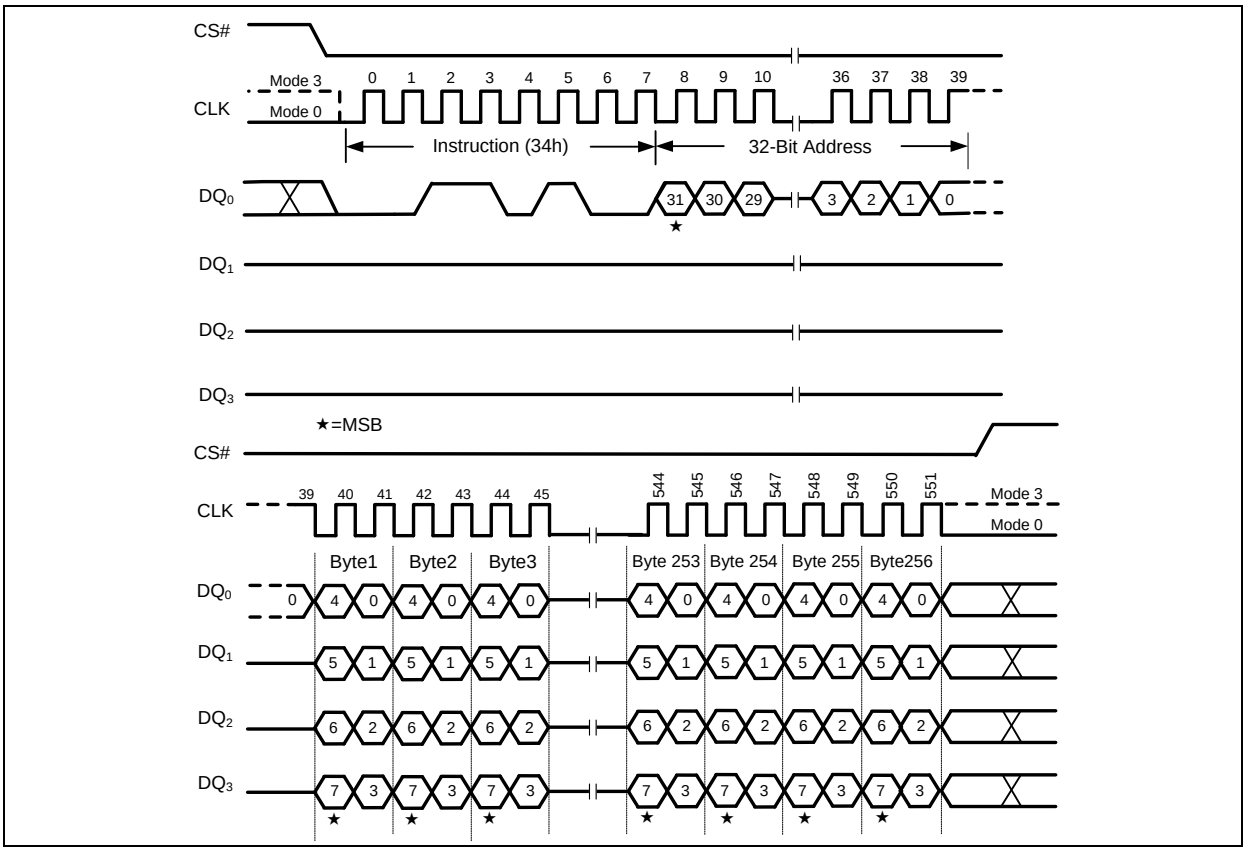


Figure 69 Quad Input Page Program with 4-Byte Address Instruction (SPI Mode only)

10.2.35. Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 32/24-bit sector address A31/A23-A0. The Sector Erase instruction sequence is shown in Figure 70 & Figure 71.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See “11.6 AC Electrical Characteristics”). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks (see Table 5 Status Register Memory Protection table).

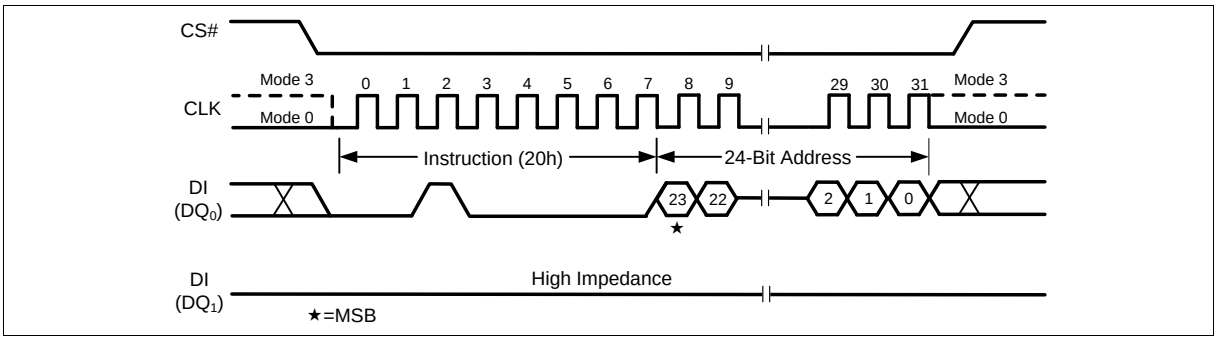


Figure 70 Sector Erase Instruction (SPI Mode)

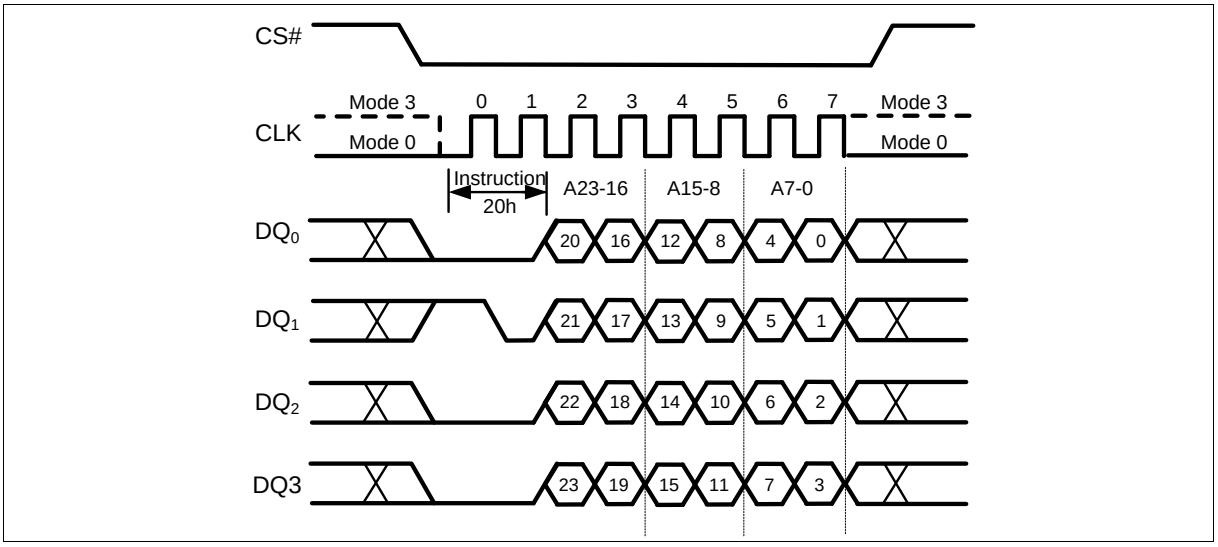


Figure 71 Sector Erase Instruction (QPI Mode)

10.2.36. Sector Erase with 4-Byte Address (21h)

The Sector Erase with 4-Byte Address instruction is similar to the Sector Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the Sector Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

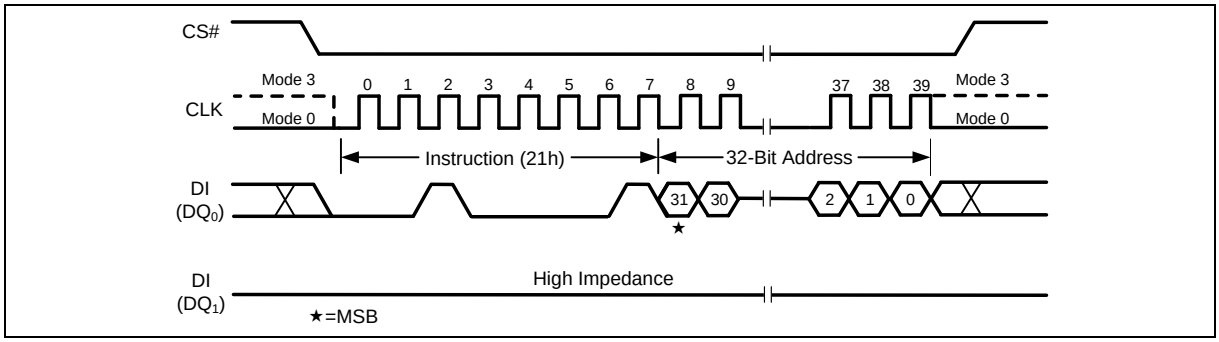


Figure 72 Sector Erase with 4-Byte Address Instruction (SPI Mode)

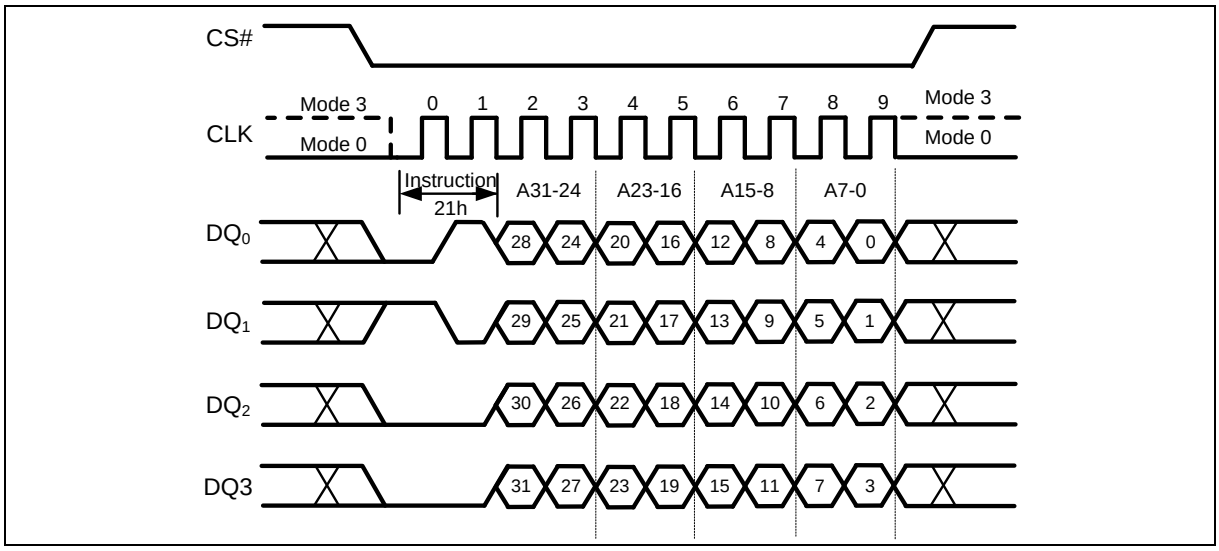


Figure 73 Sector Erase with 4-Byte Address Instruction (QPI Mode)

10.2.37. 32KB Block Erase (BE32) (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "52h" followed a 32/24-bit block address A31/A23-A0. The Block Erase instruction sequence is shown in Figure 74 & Figure 75.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See "11.6 AC Electrical Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.

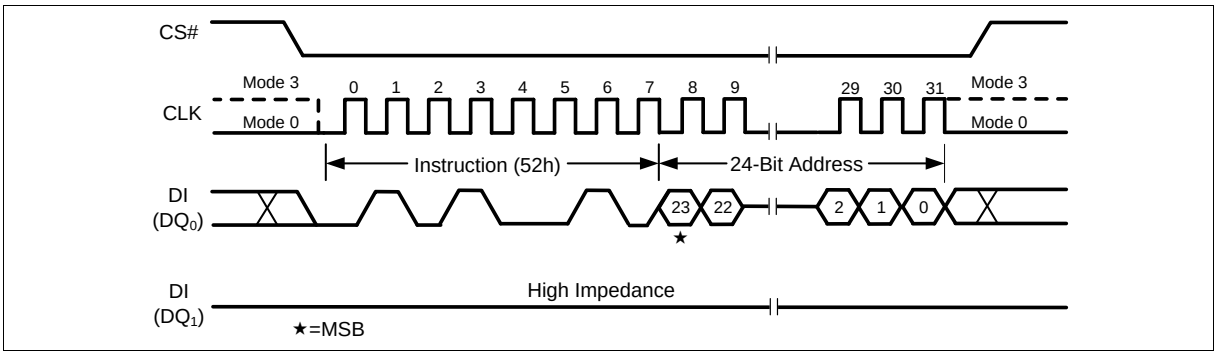


Figure 74 32KB Block Erase Instruction (SPI Mode)

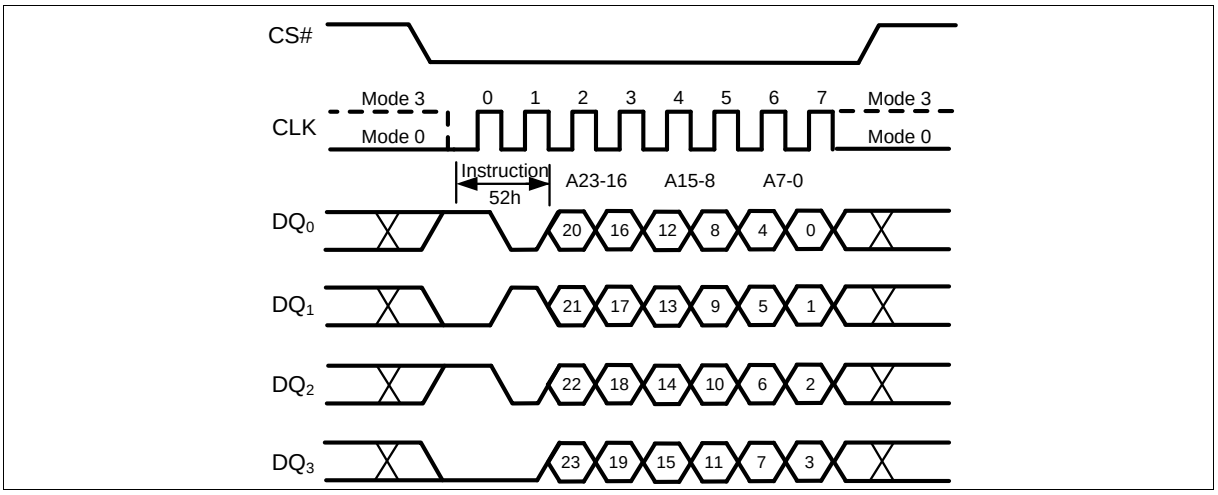


Figure 75 32KB Block Erase Instruction (QPI Mode)

10.2.38. 32KB Block Erase with 4-Byte Address (BE32) (5Ch)

The 32KB Block Erase with 4-Byte Address instruction is similar to the 32KB Block Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the 32KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

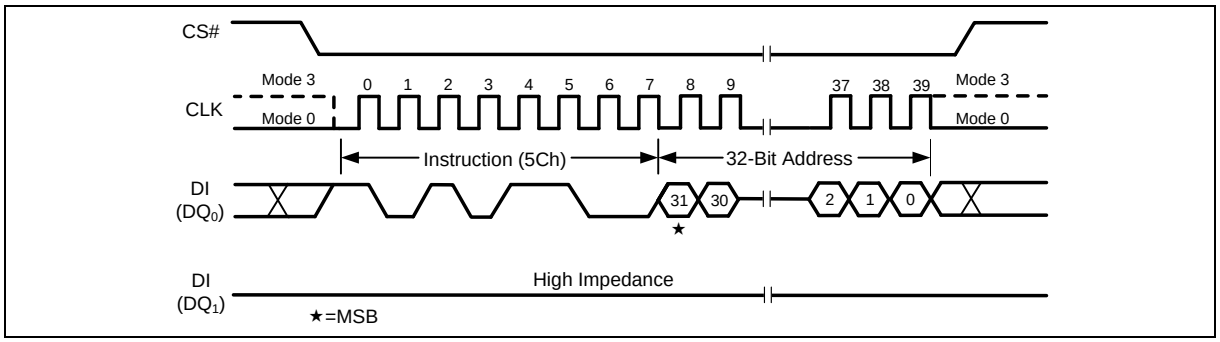


Figure 76 32KB Block Erase with 4-Byte Address Instruction (SPI Mode)

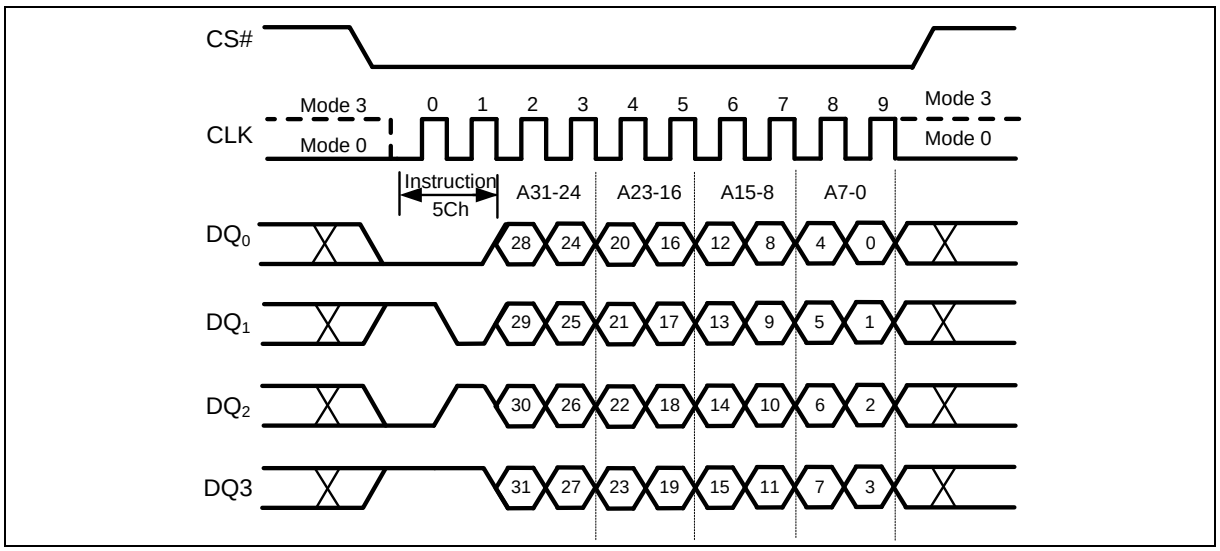


Figure 77 32KB Block Erase with 4-Byte Address Instruction (QPI Mode)

10.2.39. 64KB Block Erase (BE) (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed a 32/24-bit block address A31/A23-A0. The Block Erase instruction sequence is shown in Figure 78 & Figure 79.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See 11.6 AC Electrical Characteristics"). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.

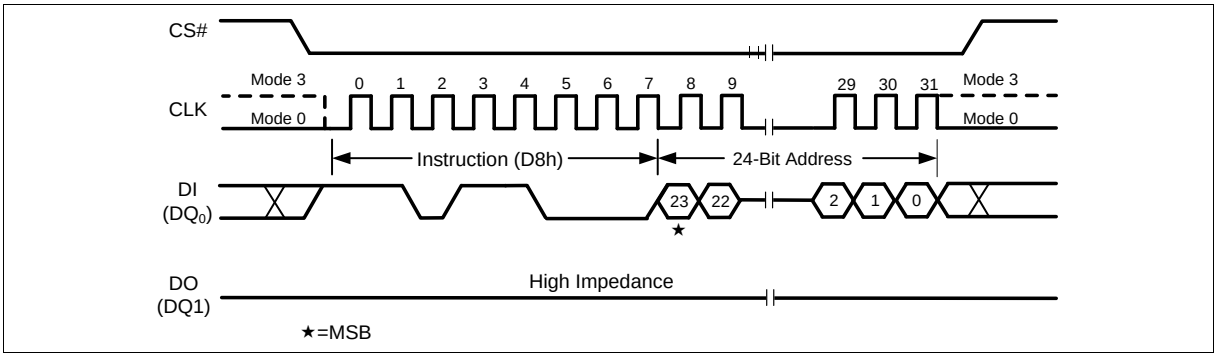


Figure 78 64KB Block Erase Instruction (SPI Mode)

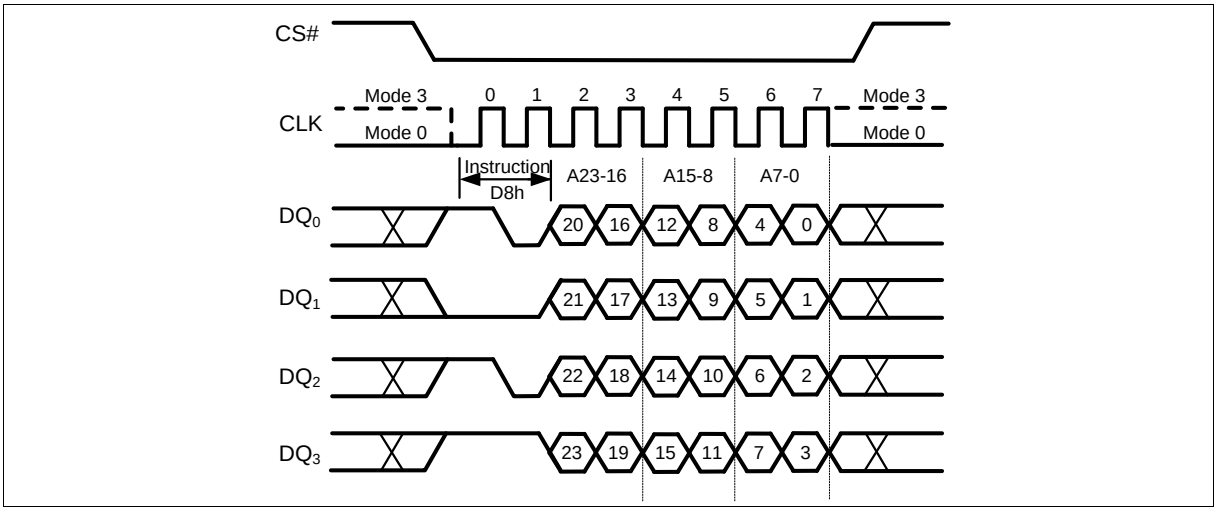


Figure 79 64KB Block Erase Instruction (QPI Mode)

10.2.40. 64KB Block Erase with 4-Byte Address (BE) (DCh)

The 64KB Block Erase with 4-Byte Address instruction is similar to the 64KB Block Erase

instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-Byte Address Mode, the 64KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

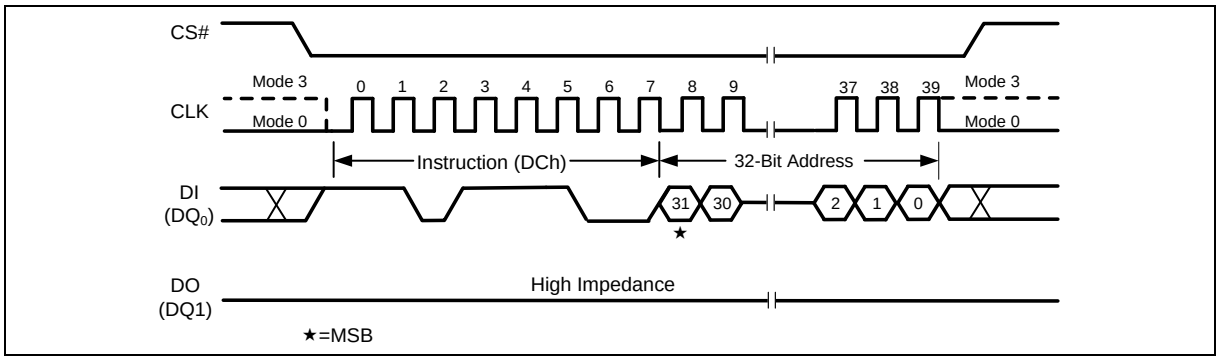


Figure 80 64KB Block Erase with 4-Byte Address Instruction (SPI Mode)

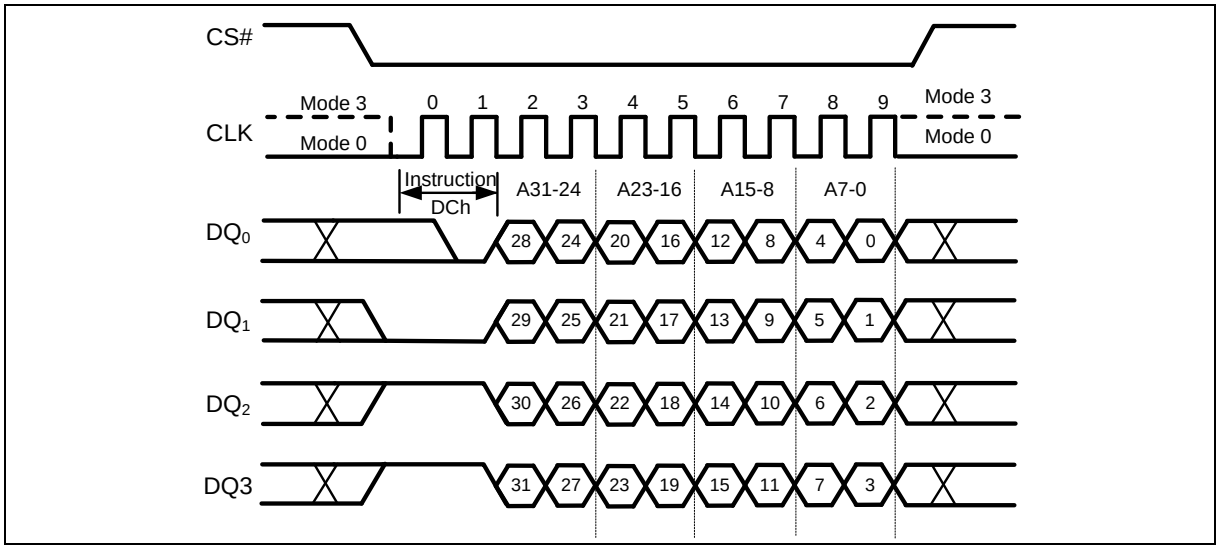


Figure 81 64KB Block Erase with 4-Byte Address Instruction (QPI Mode)

10.2.41. Chip Erase (CE) (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 82.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See “11.6 AC Electrical Characteristics”). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.

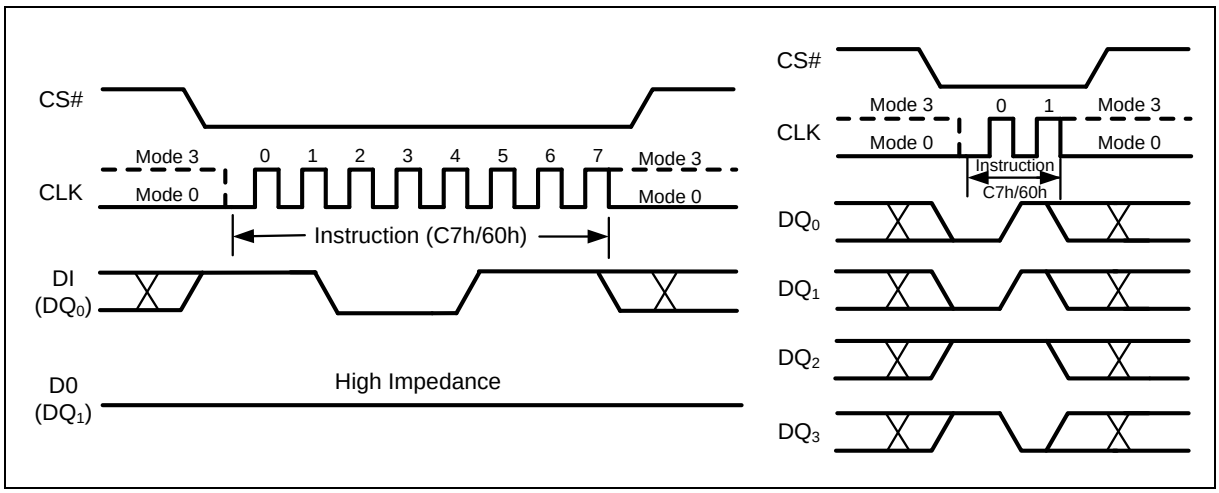


Figure 82 Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)

10.2.42. Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read data from any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 83 & Figure 84.

The Write Status Register instruction (01h, 31h), Program and Erase instructionsare not allowed during Program/Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Suspend instruction is ignored.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the WIP bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the WIP bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “t_{SUS}” (See”11.6 AC Electrical Characteristics”) is required to suspend the erase or program operation. The WIP bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “t_{SUS}” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

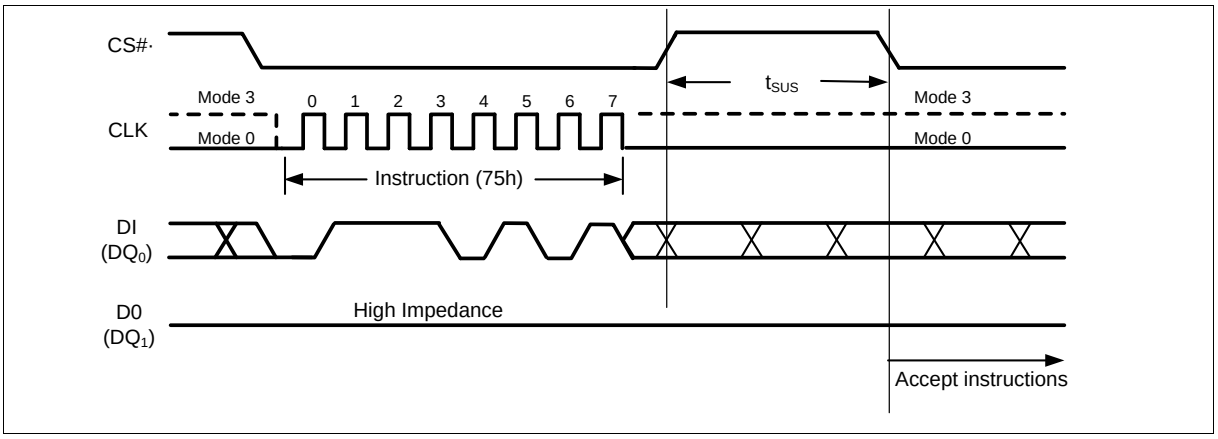


Figure 83 Erase/Program Suspend Instruction (SPI Mode)

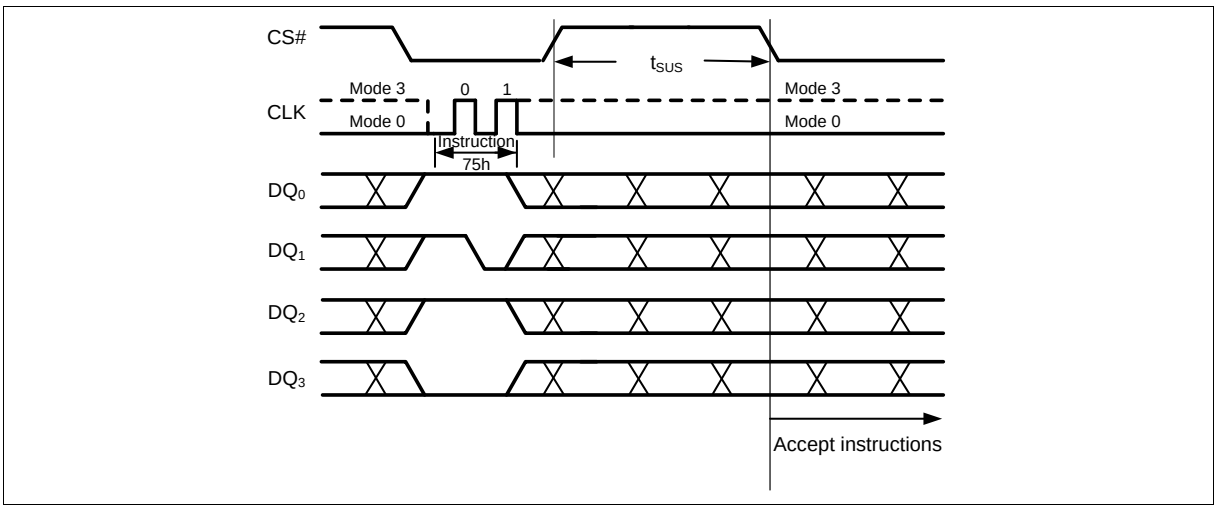


Figure 84 Erase/Program Suspend Instruction (QPI Mode)

10.2.43. Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 85 & Figure 86.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “t_{SUS}” following a previous Resume instruction.

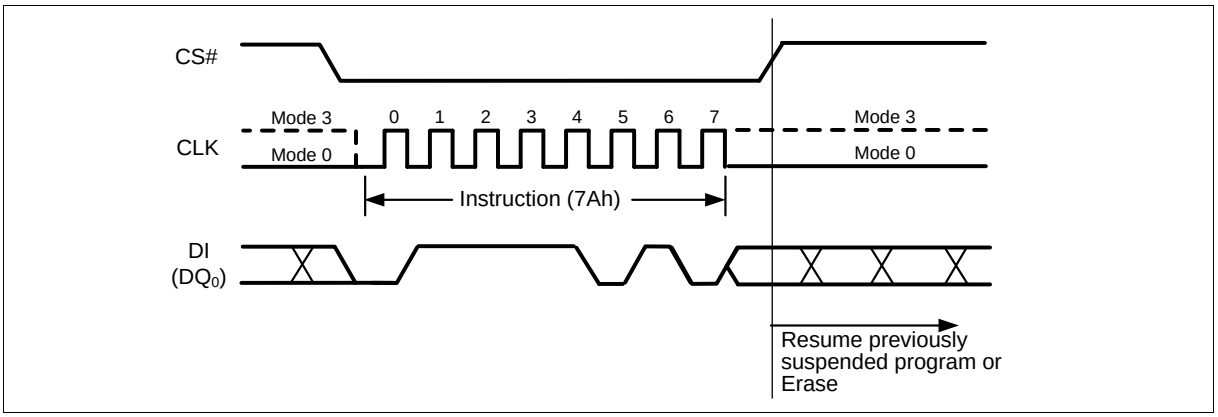


Figure 85 Erase/Program Resume Instruction (SPI Mode)

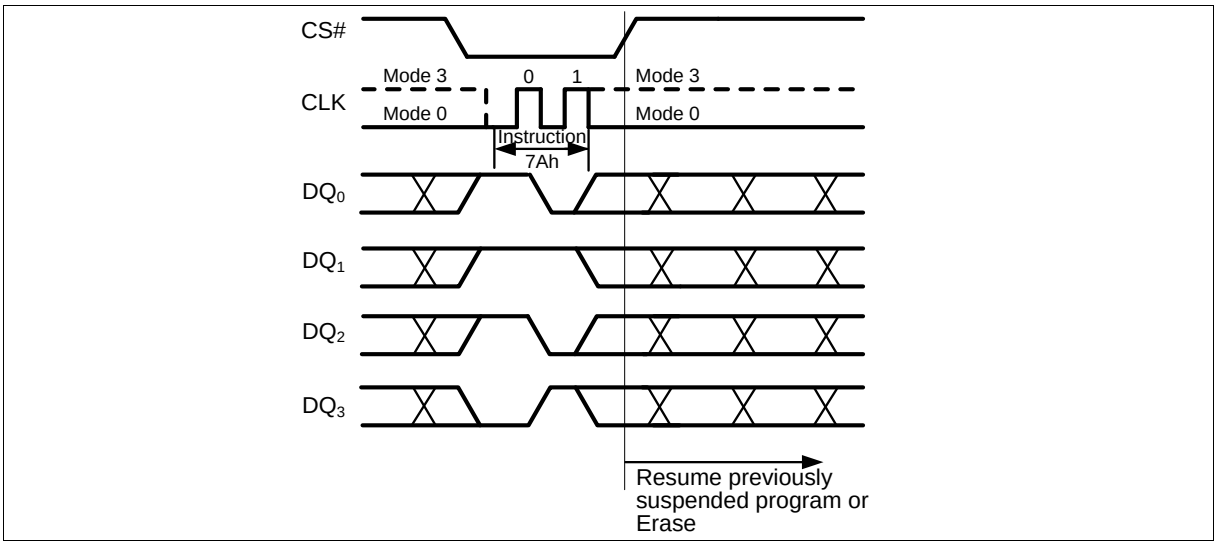


Figure 86 Erase/Program Resume Instruction (QPI Mode)

10.2.44. Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See I_{CC1} and I_{CC2} in

"11.4 DC Electrical Characteristics"). The instruction is initiated by driving the CS# pin low and shifting the instruction code "B9h" as shown in Figure 87 & Figure 88.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See "11.6 AC Electrical Characteristics"). While in the power-down state only the Release from Power- down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

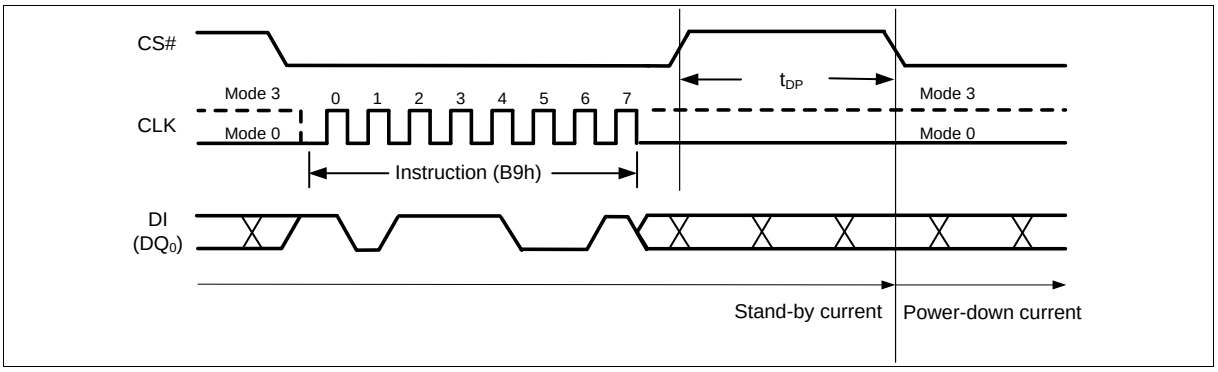


Figure 87 Deep Power-down Instruction (SPI Mode)

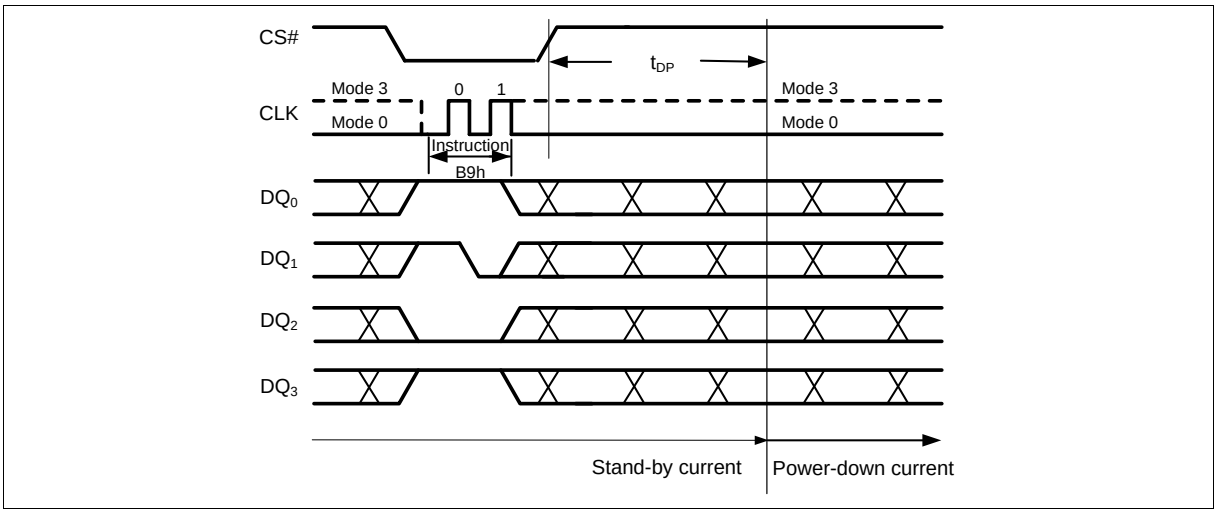


Figure 88 Deep Power-down Instruction (QPI Mode)

10.2.45. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in Figure 89 & Figure 90. Release from power-down will take the time duration of t_{RES1} (See "11.6 AC Electrical Characteristics") before the device will resume normal operation and other instructions are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 89 & Figure 90. The Device ID value for the FM25Q256I3 is listed in Table 7 Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 91 & Figure 92, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See “11.6 AC Electrical Characteristics”). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the instruction is ignored and will not have any effect on the current cycle.

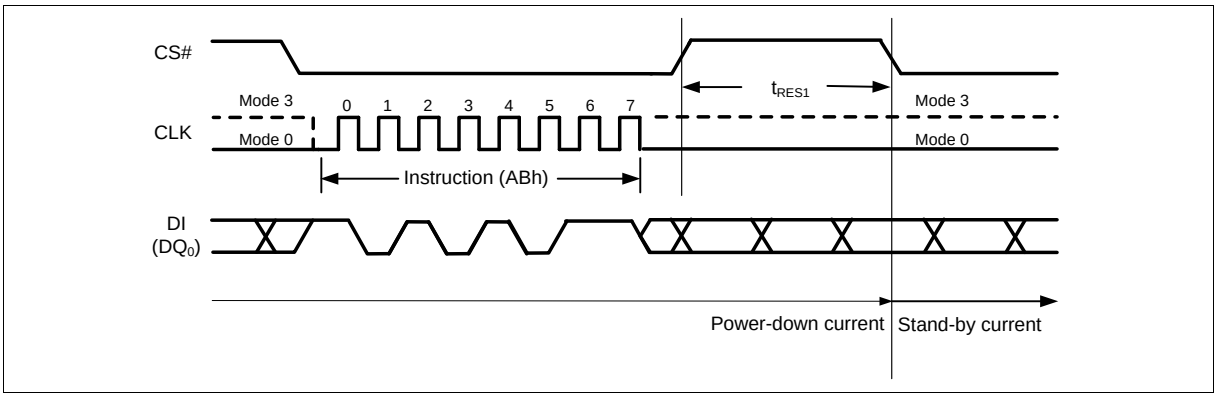


Figure 89 Release Power-down Instruction (SPI Mode)

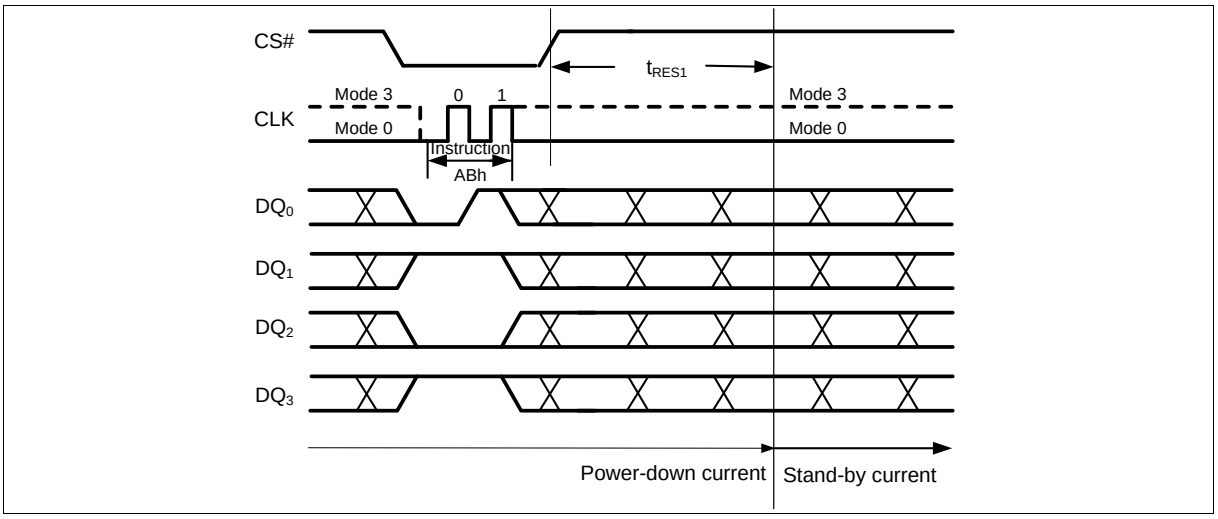


Figure 90 Release Power-down Instruction (QPI Mode)

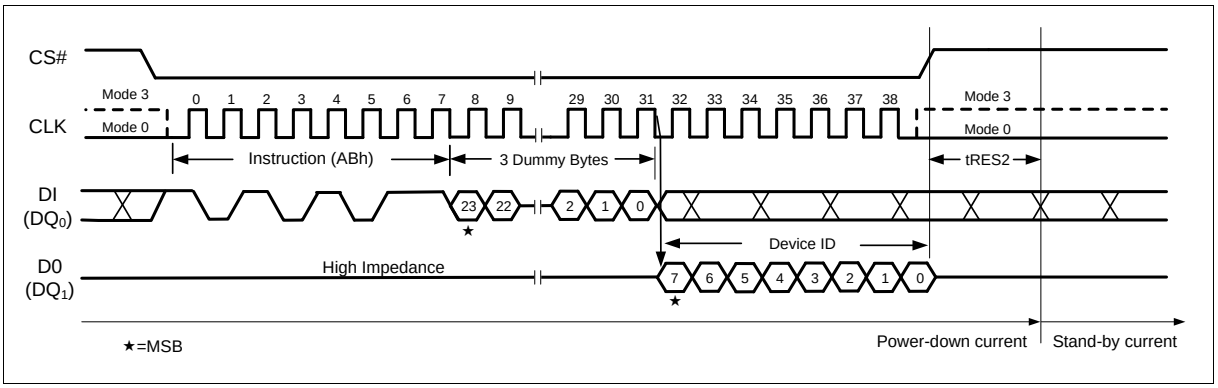


Figure 91 Release Power-down / Device ID Instruction (SPI Mode)

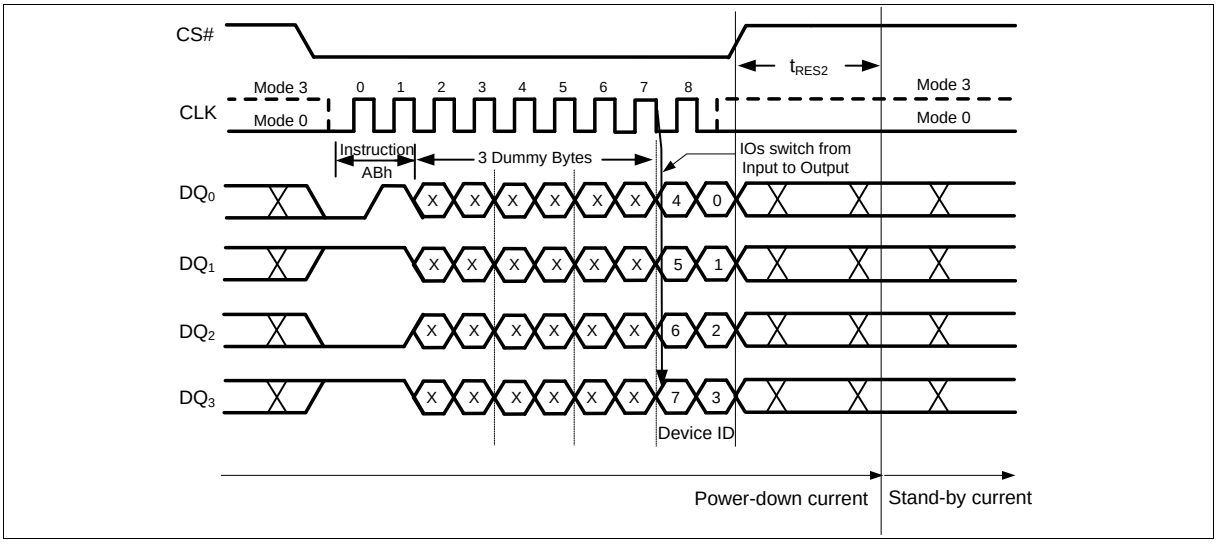


Figure 92 Release Power-down / Device ID Instruction (QPI Mode)

10.2.46. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address A23-A0 of 000000h. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 93 & Figure 94. The Device ID value for the FM25Q256I3 is listed in Table 7 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

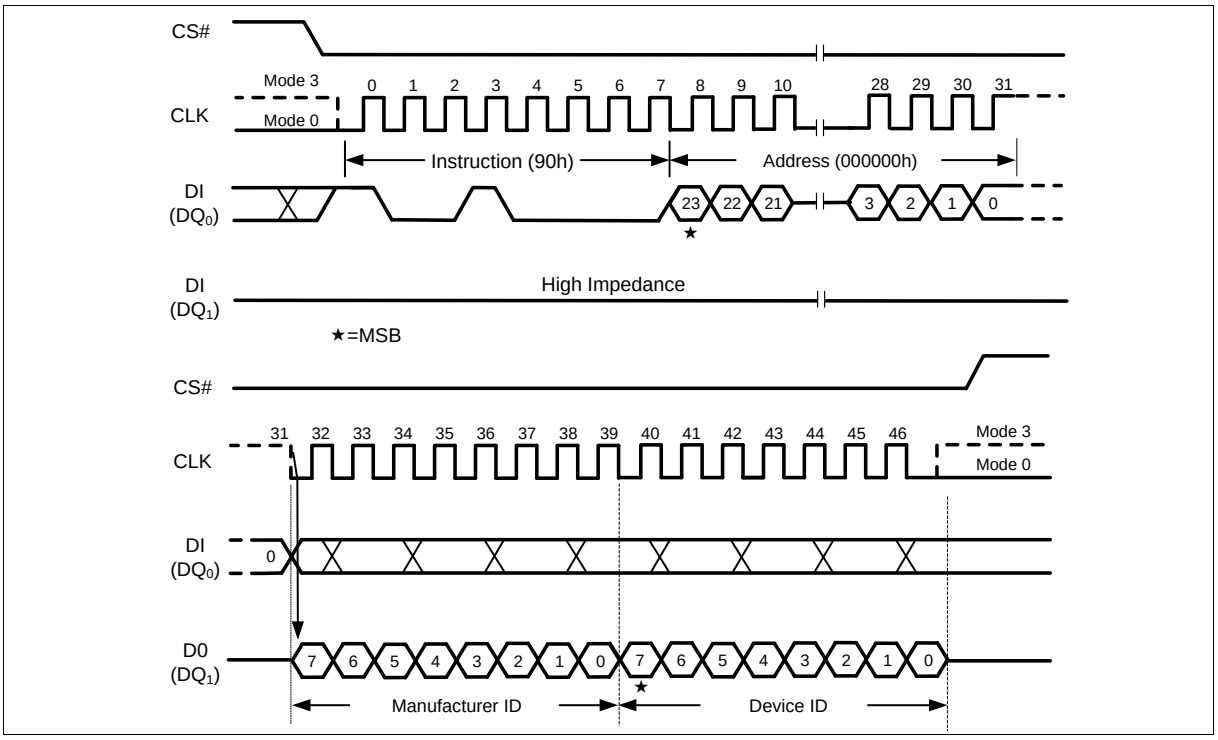


Figure 93 Read Manufacturer / Device ID Instruction (SPI Mode)

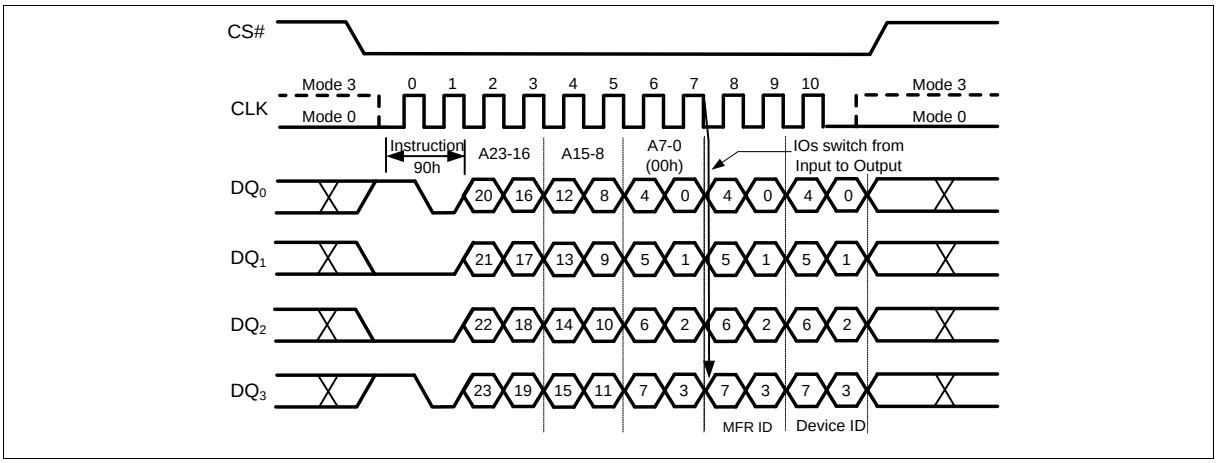


Figure 94 Read Manufacturer / Device ID Instruction (QPI Mode)

10.2.47. Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "92h" followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 95. The Device ID value for the FM25Q256I3 is listed in Table 7 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read

continuously, alternating from one to the other. The instruction is completed by driving CS# high.

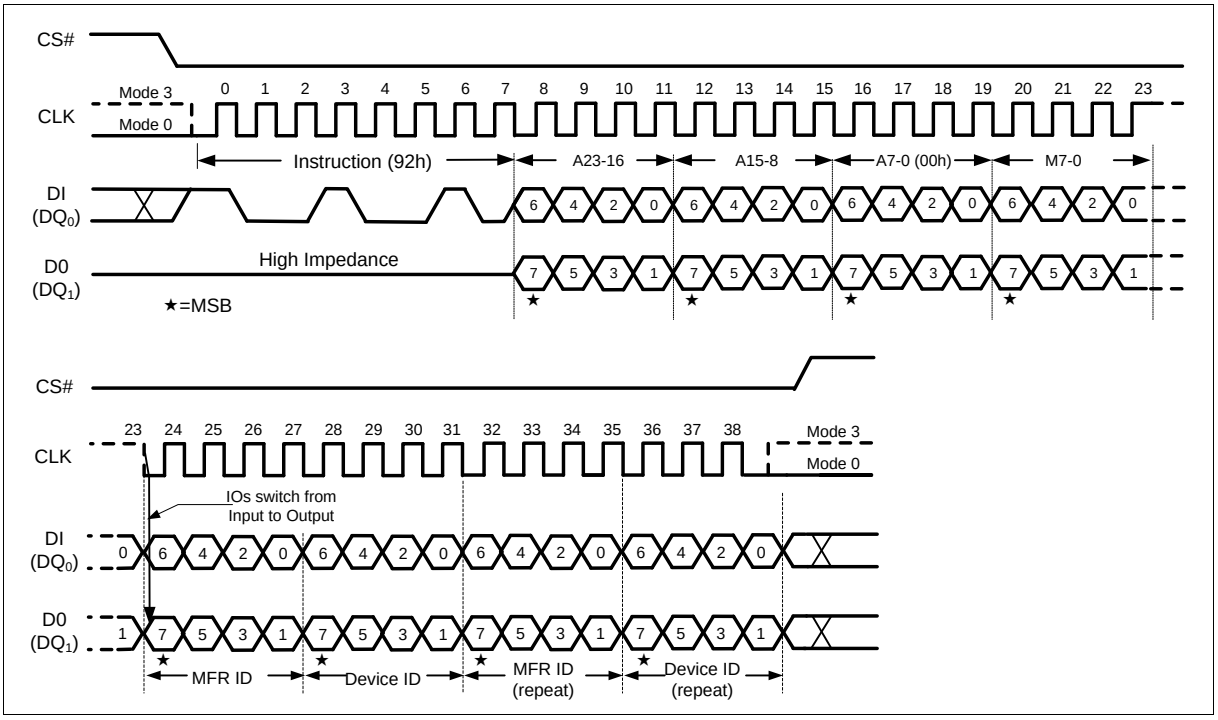


Figure 95 Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

Note:
The “Continuous Read Mode” bits M7-M0 must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

10.2.48. Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “94h” followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits and then four clock dummy cycles, with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 96. The Device ID value for the FM25Q256I3 is listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

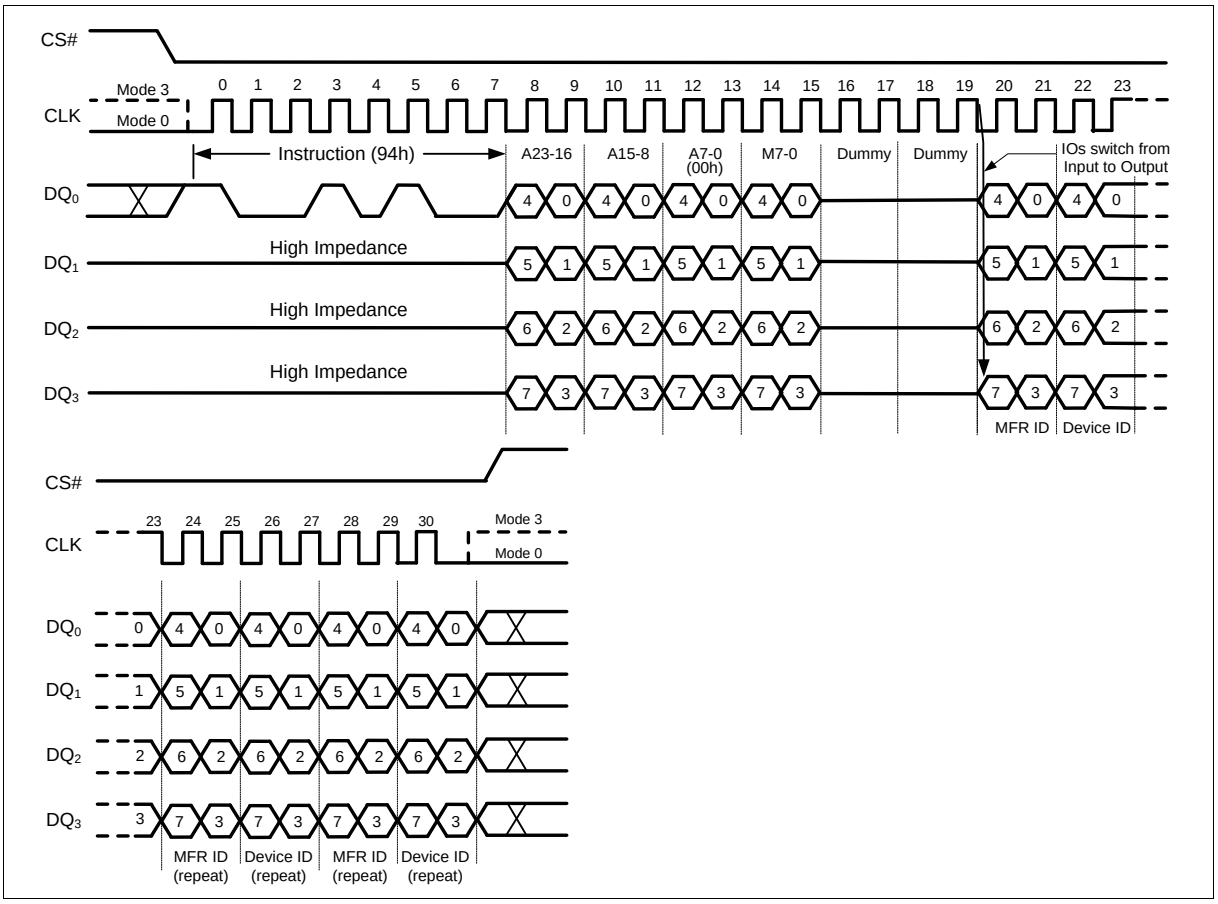


Figure 96 Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

Note:
The “Continuous Read Mode” bits M7-M0 must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

10.2.49. Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each FM25Q256I3 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “4Bh” followed by a 4 bytes or 5 bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 97.

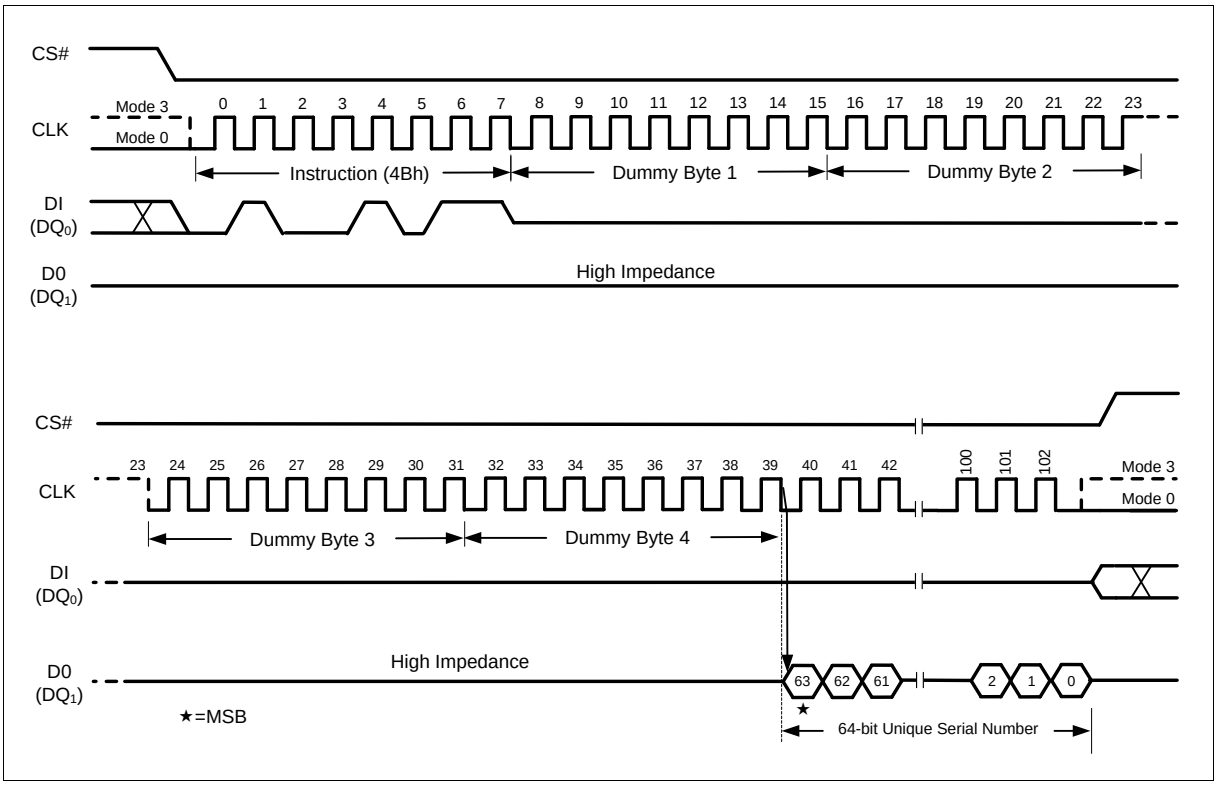


Figure 97 Read Unique ID Number Instruction (SPI Mode only)

5 Dummy Bytes are required when the device is operating in 4-Byte Address Mode

10.2.50. Read JEDEC ID (9Fh)

For compatibility reasons, the FM25Q256I3 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories. The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity ID7-ID0 are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 98 & Figure 99. For memory type and capacity values refer to Table 7 Manufacturer and Device Identification table.

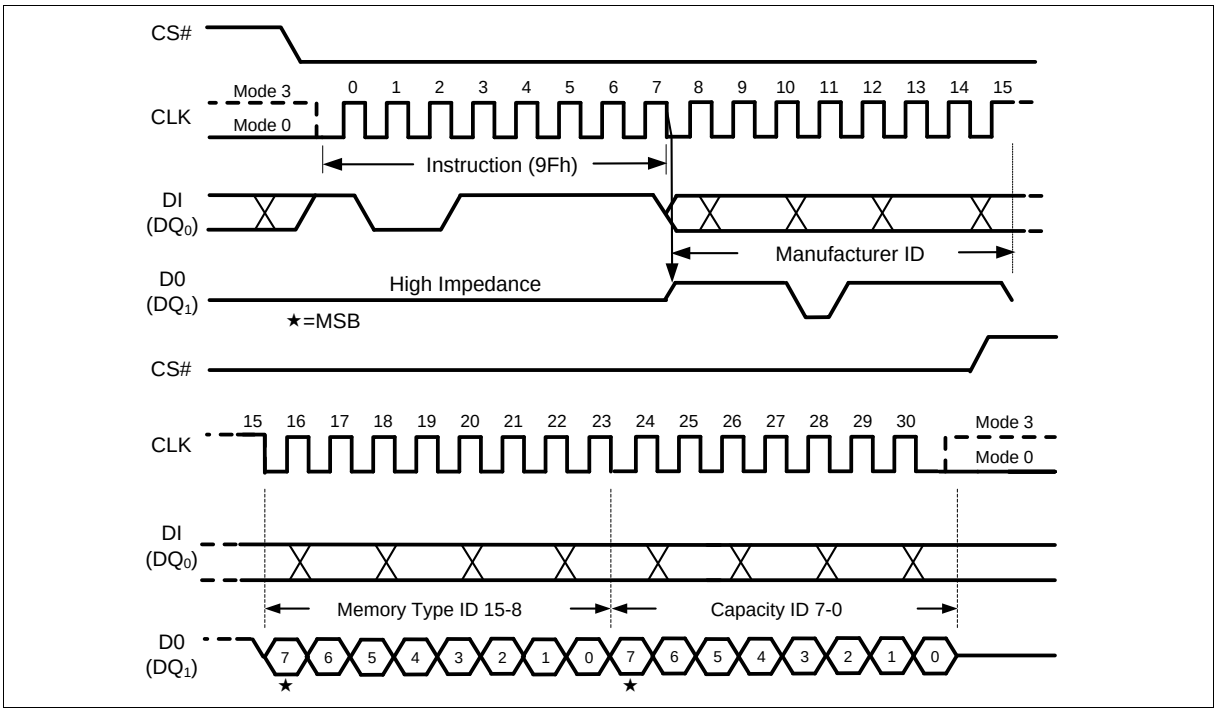


Figure 98 Read JEDEC ID Instruction (SPI Mode)

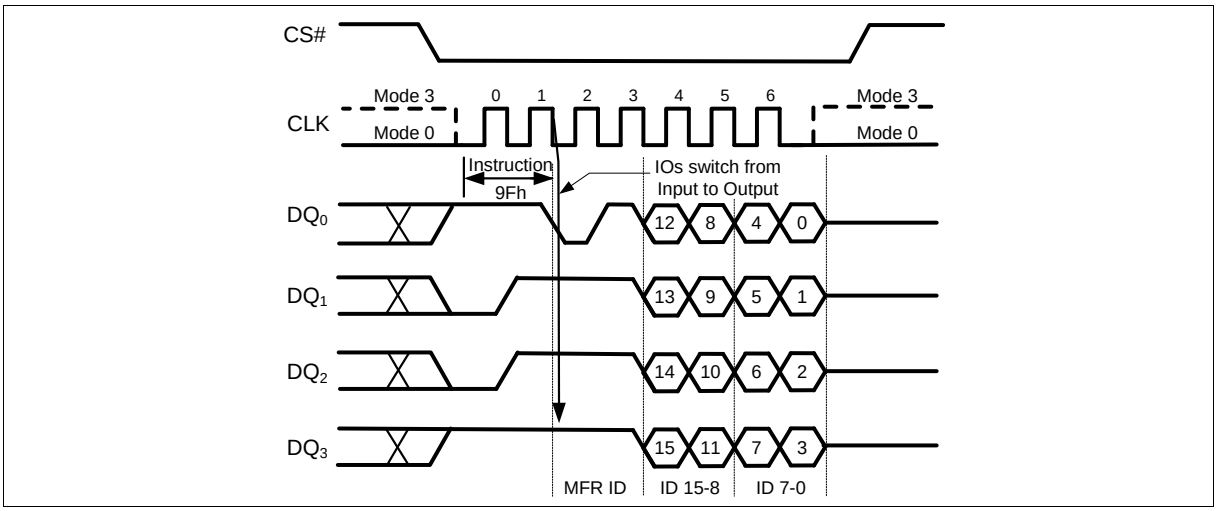


Figure 99 Read JEDEC ID Instruction (QPI Mode)

10.2.51. Read SFDP Register (5Ah)

The FM25Q256I3 features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard 1.0 that is published in 2011.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0) (1) into the DI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 100. For SFDP register values and descriptions, refer to the following SFDP Definition table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

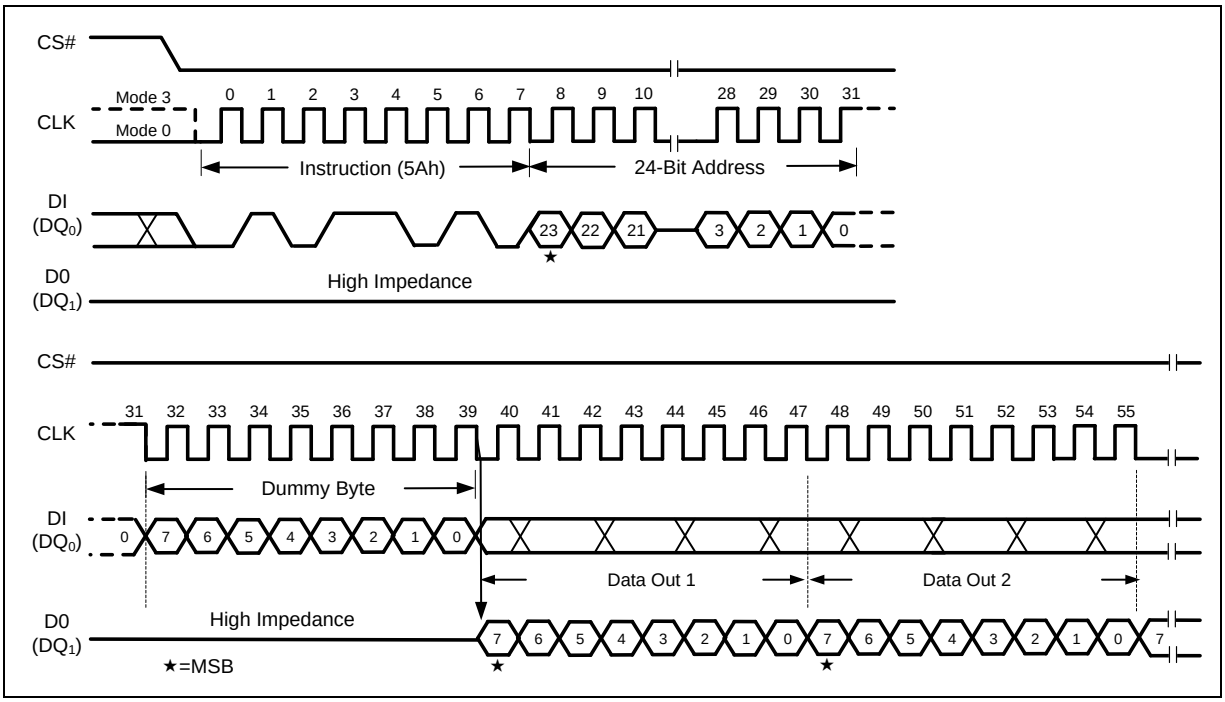


Figure 100 Read SFDP Register Instruction

Serial Flash Discoverable Parameter (JEDEC Revision 1.0) Definition Table

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
00h	53h	SFDP Signature	SFDP Signature = 50444653h
01h	46h	SFDP Signature	
02h	44h	SFDP Signature	
03h	53h	SFDP Signature	
04h	00h	SFDP Minor Revision Number	JEDEC Revision 1.0
05h	01h	SFDP Major Revision Number	
06h	00h	Number of Parameter Headers (NPH)	1 Parameter Header
07h	FFh	Reserved	
08h	00h	PID(3)(0): ID Number	00h = JEDEC specified
09h	00h	PID(0): Parameter Table Minor Revision Number	JEDEC Revision 1.0
0Ah	01h	PID(0): Parameter Table Major Revision Number	
0Bh	09h	PID(0): Parameter Table Length	9 Dwords(2)
0Ch	80h	PID(0): Parameter Table Pointer (PTP) (A7-A0)	PID(0) Pointer = 000080h
0Dh	00h	PID(0): Parameter Table Pointer (PTP) (A15-A8)	
0Eh	00h	PID(0): Parameter Table Pointer (PTP) (A23-A16)	
0Fh	FFh	Reserved	
10h	FFh	Reserved	
...(1)	FFh	Reserved	
7Fh	FFh	Reserved	
80h	E5h	Bit[7:5]=111 Reserved Bit[4:3]=00 Non-volatile Status Register Bit[2]=1 Page Programmable Bit[1:0]=01 Supports 4KB Erase	
81h	20h	4K-Byte Erase Opcode	
82h	F1h	Bit[7] =1 Reserved	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
		Bit[6] =1 Supports (1-1-4) Fast Read Bit[5] =1 Supports (1-4-4) Fast Read Bit[4] =1 Supports (1-2-2) Fast Read Bit[3] =0 Not support Dual Transfer Rate Bit[2:1]=01 3-Byte or 4-Byte Addressing Bit[0] =1 Supports (1-1-2) Fast Read	
83h	FFh	Reserved	
84h	FFh	Flash Size in Bits	256 Mega Bits = 0FFFFFFFh
85h	FFh	Flash Size in Bits	
86h	FFh	Flash Size in Bits	
87h	0Fh	Flash Size in Bits	
88h	44h	Bit[7:5]=010 8 Mode Bits are needed Bit[4:0]=00100 16 Dummy Bits are needed	Fast Read Quad I/O Setting
89h	EBh	Quad Input Quad Output Fast Read Opcode	
8Ah	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Quad Output Setting
8Bh	6Bh	Single Input Quad Output Fast Read Opcode	
8Ch	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Dual Output Setting
8Dh	3Bh	Single Input Dual Output Fast Read Opcode	
8Eh	80h	Bit[7:5]=100 8 Mode bits are needed Bit[4:0]=00000 No Dummy bits are needed	Fast Read Dual I/O Setting
8Fh	BBh	Dual Input Dual Output Fast Read Opcode	
90h	FEh	Bit[7:5]=111 Reserved Bit[4]=1 support (4-4-4) Fast Read Bit[3:1]=111 Reserved Bit[0]=0 Not support (2-2-2) Fast Read	
91h	FFh	Reserved	
92h	FFh	Reserved	
93h	FFh	Reserved	
94h	FFh	Reserved	
95h	FFh	Reserved	
96h	00h	No Mode Bits or Dummy Bits for (2-2-2) Fast Read	
97h	00h	Not support (2-2-2) Fast Read	
98h	FFh	Reserved	
99h	FFh	Reserved	
9Ah	08h	Bit[7:5]=000 No Mode bits are needed Bit[4:0]=01000 8 Dummy bits are needed	
9Bh	EBh	QPI Fast Read Opcode	
9Ch	0Ch	Sector Type 1 Size (4KB)	Sector Erase Type & Opcode
9Dh	20h	Sector Type 1 Opcode	
9Eh	0Fh	Sector Type 2 Size (32KB)	
9Fh	52h	Sector Type 2 Opcode	
A0h	10h	Sector Type 3 Size (64KB)	Sector Erase Type & Opcode
A1h	D8h	Sector Type 3 Opcode	
A2h	00h	Sector Type 4 Size (256KB) – Not supported	
A3h	00h	Sector Type 4 Opcode – Not supported	
...(1)	FFh	Reserved	
FFh	FFh	Reserved	

Notes:
1. Data stored in Byte Address 10h to 7Fh & A4h to FFh are reserved, the value is FFh.
2. 1 Dword = 4 Bytes
3. PID(x) = Parameter Identification Table (x)

10.2.52. Erase Security Sector (44h)

The FM25Q256I3 offers one 4x256-byte Security Sector. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Sector instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Sector Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “44h” followed by a 32/24-bit address A31/A23-A0 to erase the Security Sector.

A31/A23-16	A15-12	A11-8	A7-0
0000h/00h	0 0 0 0	0 0 0 0	Don’t Care

The Erase Security Sector instruction sequence is shown in Figure 101. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After CS# is driven high, the self-timed Erase Security Sector operation will commence for a time duration of t_{SE} (See “11.6_AC Electrical Characteristics”). While the Erase Security Sector cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Sector cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Sector Lock Bit (LB) in the Status Register-2 can be used to OTP protect the Security Sector. Once a lock bit is set to 1, the Security Sector will be permanently locked and Erase Security Sector instruction will be ignored.

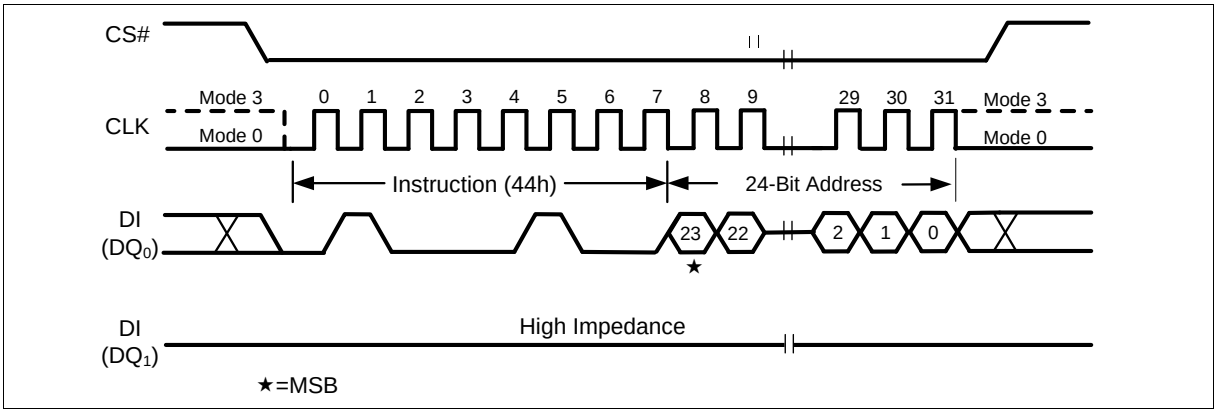


Figure 101 Erase Security Sector Instruction (SPI Mode only)

10.2.53. Program Security Sector (42h)

The Program Security Sector instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of Security Sector data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Sector Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “42h” followed by a 32/24-bit address A31/A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A31/A23-16	A15-12	A11-8	A7-0
Security Sector page0	0000h/00h	0 0 0 0	0 0 0 0	Don’t Care
Security Sector page1	0000h/00h	0 0 0 0	0 0 0 1	Don’t Care
Security Sector page2	0000h/00h	0 0 0 0	0 0 1 0	Don’t Care
Security Sector page3	0000h/00h	0 0 0 0	0 0 1 1	Don’t Care

The Program Security Sector instruction sequence is shown in Figure 102. The Security Sector Lock Bit (LB) in the Status Register-2 can be used to OTP protect the Security Sector. Once a lock bit is set to 1, the Security Sector will be permanently locked and Program Security Sector instruction will be ignored.

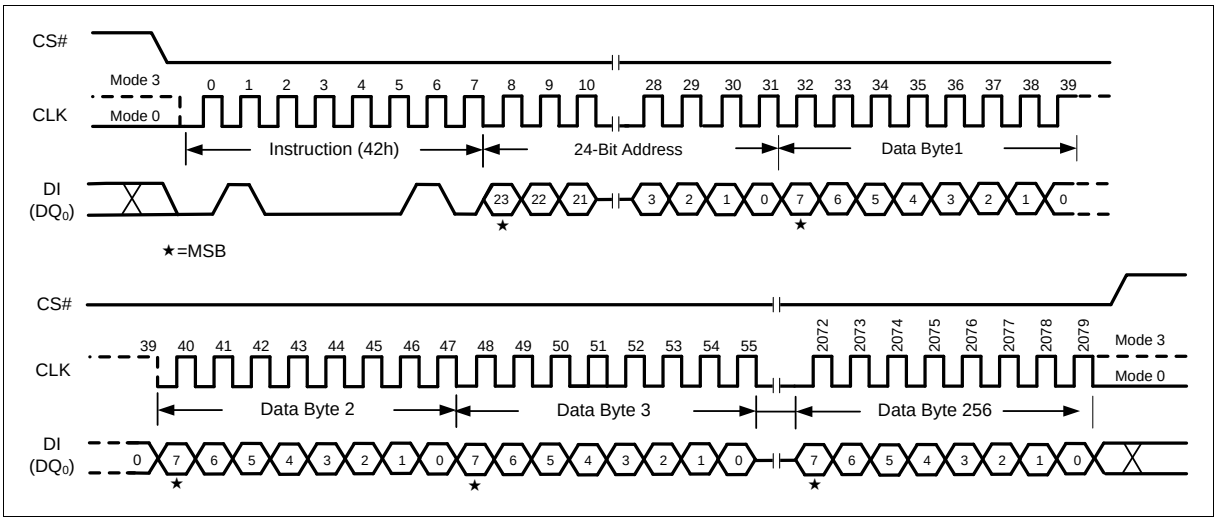


Figure 102 Program Security Sector Instruction (SPI Mode only)

10.2.54. Read Security Sector (48h)

The Read Security Sector instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from the Security Sector. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “48h” followed by a 32/24-bit address A31/A23-A0 and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin.

After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will be reset to 00h, the first byte of the register, and continues to increment. The instruction is completed by driving CS# high. The Read Security Sector instruction sequence is shown in Figure 103.

If a Read Security Sector instruction is issued while an Erase, Program or Write cycle is in process (WIP =1), the instruction is ignored and will not have any effect on the current cycle. The Read Security Sector instruction allows clock rates from D.C. to a maximum of FR (see “11.6 AC Electrical Characteristics”).

ADDRESS	A31/A23-16	A15-12	A11-8	A7-0
Security Sector page0	0000h/00h	0 0 0 0	0 0 0 0	Don’t Care
Security Sector page1	0000h/00h	0 0 0 0	0 0 0 1	Don’t Care
Security Sector page2	0000h/00h	0 0 0 0	0 0 1 0	Don’t Care
Security Sector page3	0000h/00h	0 0 0 0	0 0 1 1	Don’t Care

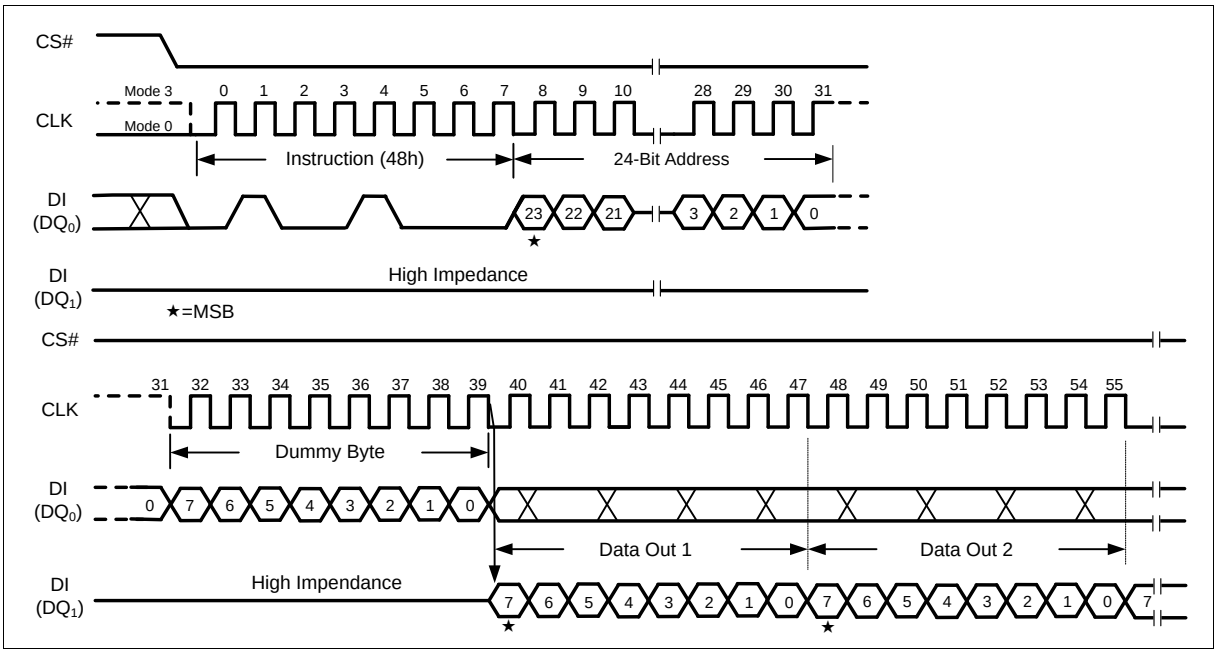


Figure 103 Read Security Sector Instruction (SPI Mode only)

10.2.55. Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks(include continuous mode bit clocks) for “Fast Read (0Bh)”, “Fast Read with 4-Byte Address (0Ch)”, “Fast Read Quad I/O

(EBh)" and "Fast Read Quad I/O with 4-Byte Address (ECh)" instructions.

In Standard SPI mode, the "Set Read Parameters (C0h)" instruction is not accepted. The dummy clocks for various Fast Read instructions in DIO/QIO mode are set by LC bits in SR3, please refer to Table 8 for details. This setting will be cleared when the device is switched from Standard SPI mode to QPI mode.

The "Wrap Length" is set by W5-4 bit in the "Set Burst with Wrap (77h)" instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default "Wrap Length" after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 2.

P6 – P4 (LC1-0)=00b	DUMMY CLOCKS	MAXIMUM READ FREQ.
0 0 0	2	50MHz
0 0 1	4	80MHz
0 1 0	6	100MHz
0 1 1	8	100MHz

P2 – P0	WRAP LENGTH
1 x x	No wrap
0 0 0	8-byte
0 0 1	16-byte
0 1 0	32-byte
0 1 1	64-byte

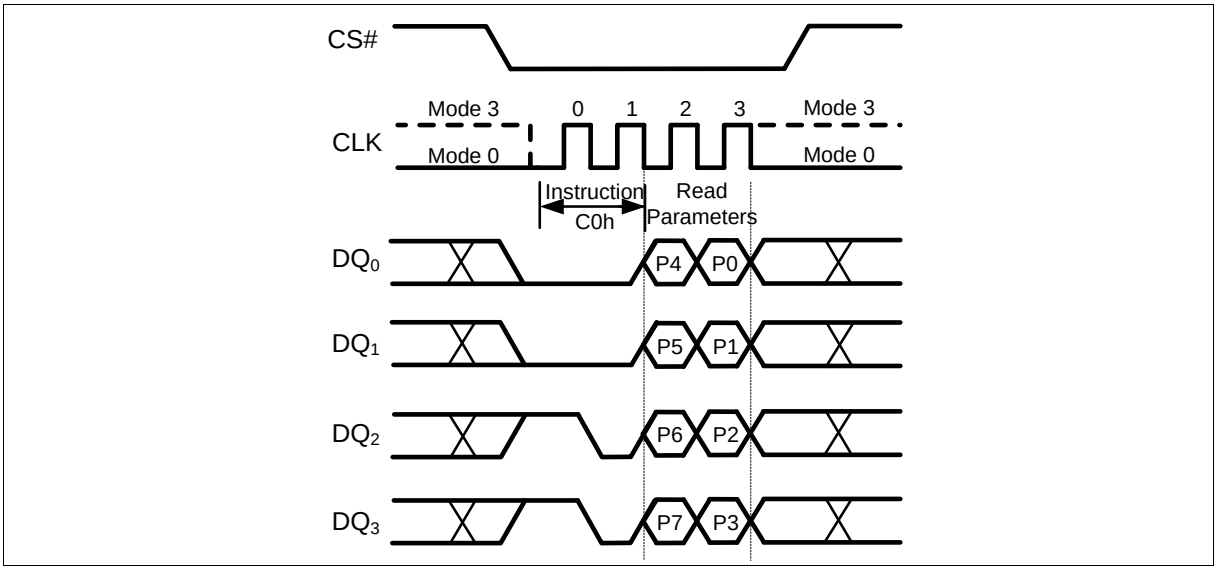


Figure 104 Set Read Parameters Instruction (QPI Mode only)

10.2.56. Enable QPI (38h)

The FM25Q256I3 support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode can not be used at the same time. "Enable QPI (38h)" instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set to 1 first, and an "Enable QPI (38h)" instruction must be issued. If the Quad Enable (QE) bit is 0, the "Enable QPI (38h)" instruction will be ignored and the device will remain in SPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

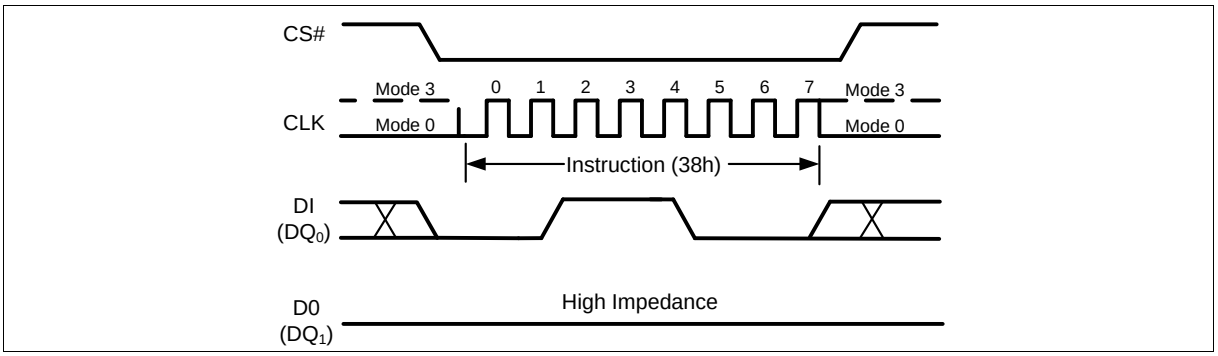


Figure 105 Enable QPI Instruction (SPI Mode only)

10.2.57. Disable QPI (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, a “Disable QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status and the Wrap Length setting will remain unchanged.

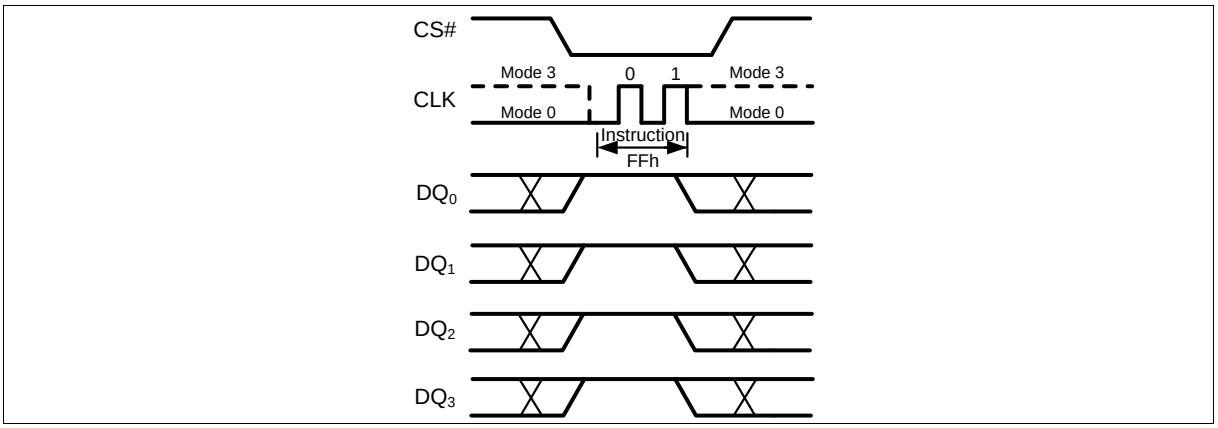


Figure 106 Disable QPI Instruction (QPI Mode only)

10.2.58. Individual Block/Sector Lock(36h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP3, BP2, BP1 and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset is 1, so the entire memory array is being protected.

To lock a specific block or sector as illustrated in Figure 107, an Individual Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 32/24-bit address and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Unlock Instruction (Status Register bit WEL= 1).

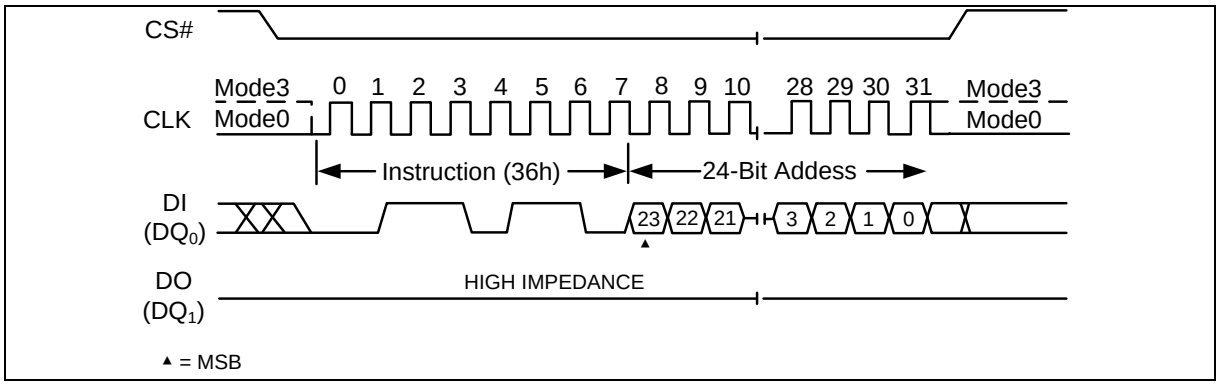


Figure 107 Read Block/Sector Lock Instruction(SPI)

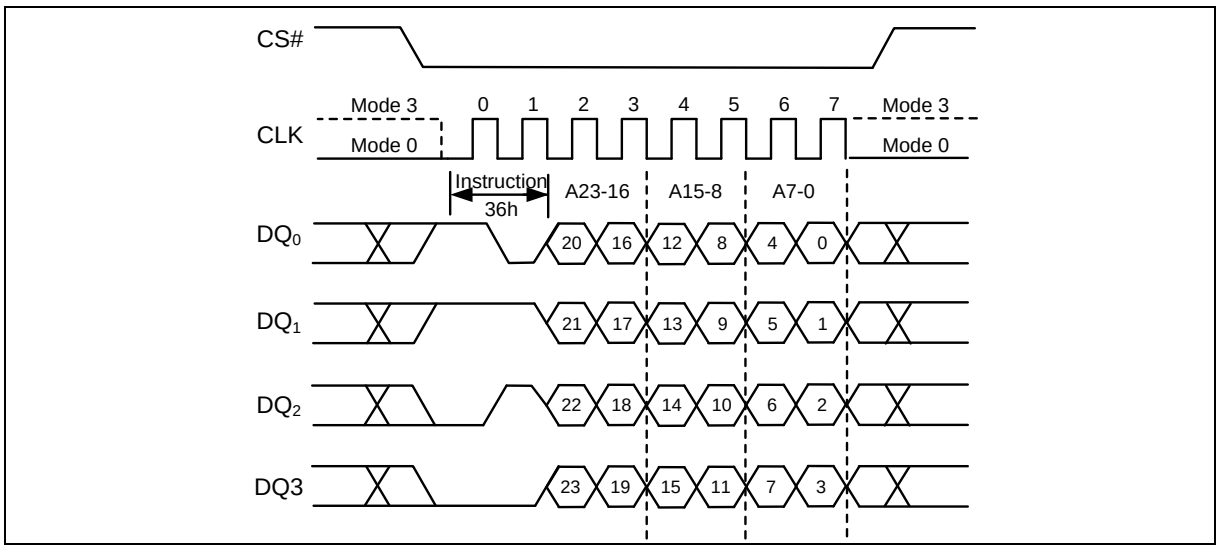


Figure 108 Read Block/Sector Lock Instruction(QPI Mode)

10.2.59. Individual Block/Sector Unlock(39h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP3, BP2, BP1 and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset is 1, so the entire memory array is being protected.

To unlock a specific block or sector as illustrated in Figure 109, an Individual Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 32/24-bit address and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Unlock Instruction (Status Register bit WEL= 1).

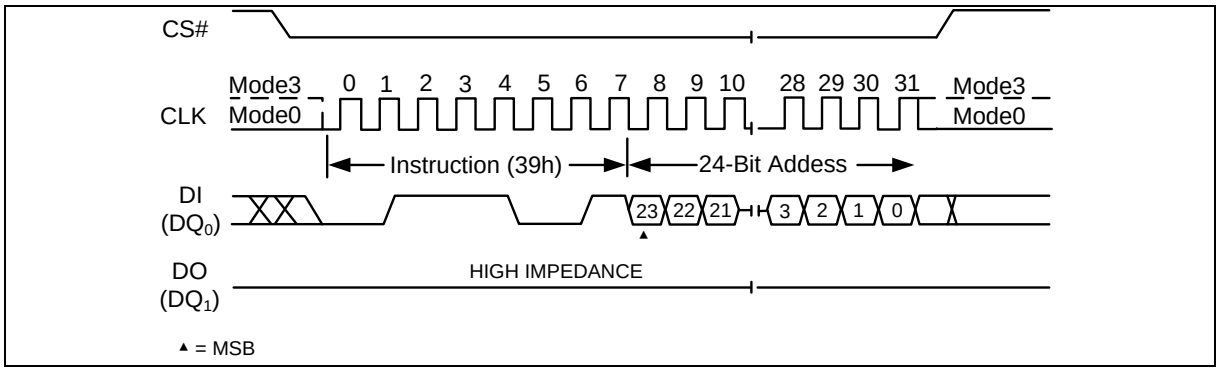


Figure 109 Individual Block/Sector Lock Instruction (SPI Mode)

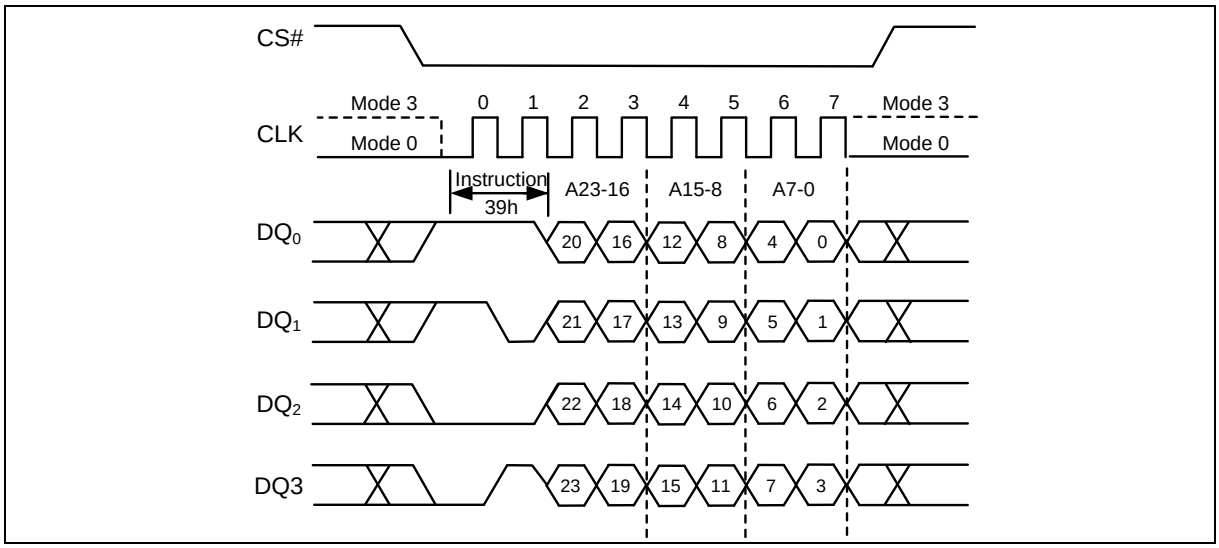


Figure 110 Individual Block/Sector Lock Instruction (QPI Mode)

10.2.60. Read Block/Sector Lock (3Dh)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP3, BP2, BP1 and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset is 1, so the entire memory array is being protected.

To read out the lock bit of a specific block or sector as illustrated in Figure 111, a Read Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 32/24-bit address and then driving CS# high. The Block/Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) as shown in. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

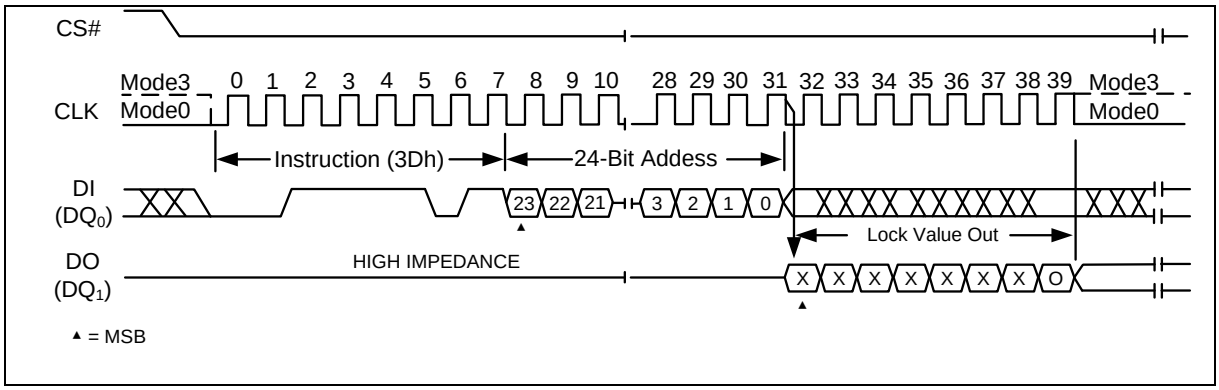


Figure 111 Read Block/Sector Lock Instruction (SPI Mode)

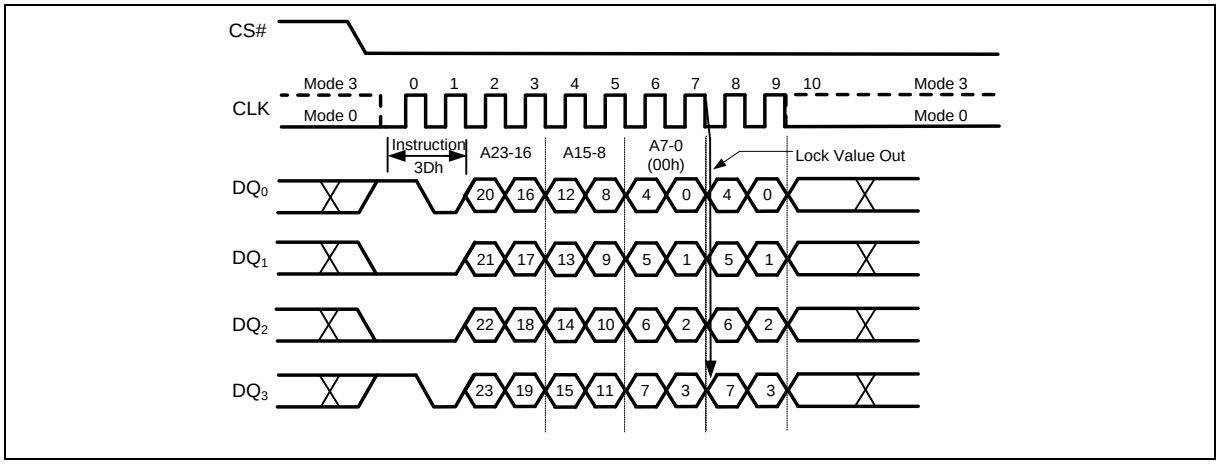


Figure 112 Read Block/Sector Lock Instruction (QPI Mode)

10.2.61. Global Block/Sector Lock (7Eh)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The command must be issued by driving CS# low, shifting the instruction code “7Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Unlock Instruction (Status Register bit WEL= 1).

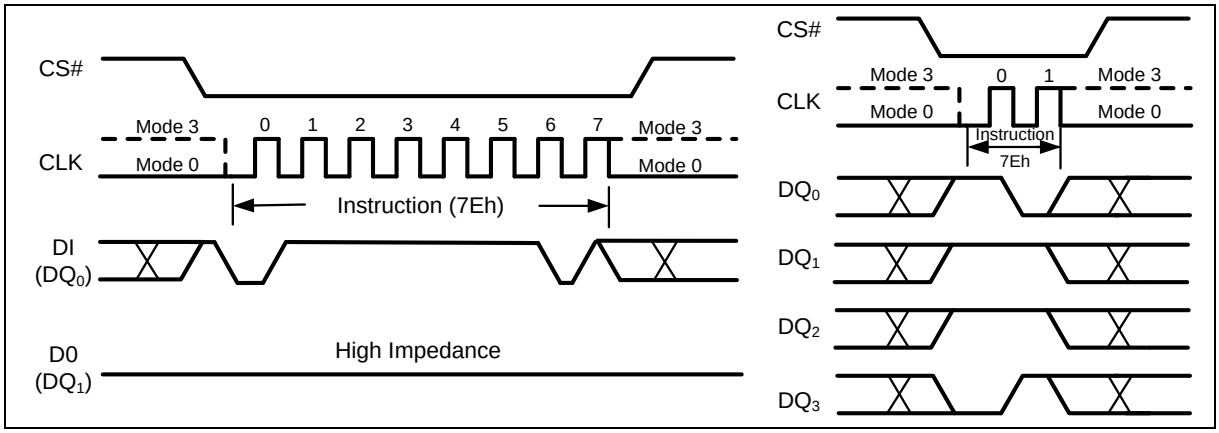


Figure 113 Global Block/Sector Lock Instruction for SPI Mode (left) or QPI Mode (right)

10.2.62. Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving CS# low, shifting the instruction code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Unlock Instruction (Status Register bit WEL= 1).

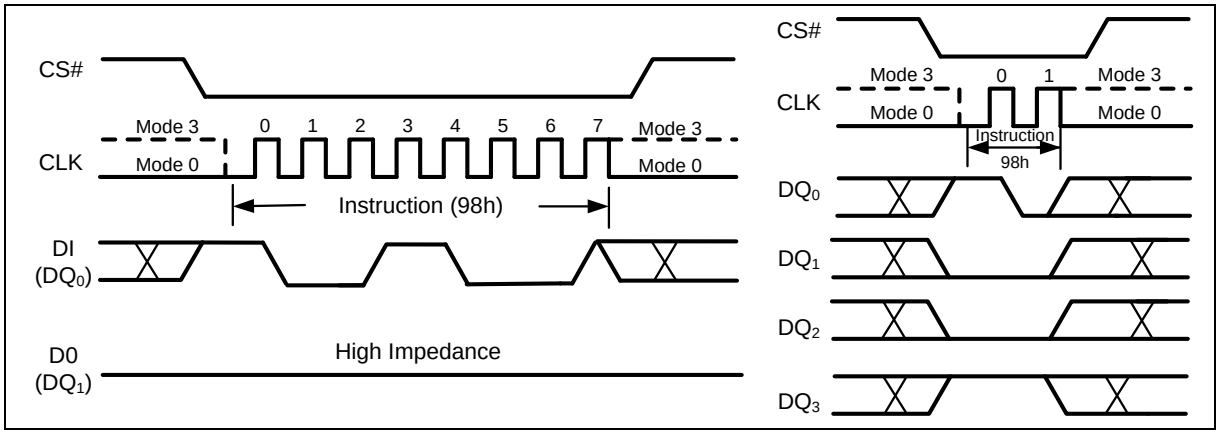


Figure 114 Global Block/Sector Unlock Instruction for SPI Mode (left) or QPI Mode (right)

10.2.63. PPB Read (E2h)

The instruction E2h is shifted into SI by the rising edges of the SCK signal, followed by the 32-bit address selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be zero) Then the 8-bit PPB access register contents are shifted out on SO.

It is possible to read the same PPB access register continuously by providing multiples of eight clock cycles. The address of the PPB register does not increment so this is not a means to read the entire PPB array. Each location must be read with a separate PPB Read command.

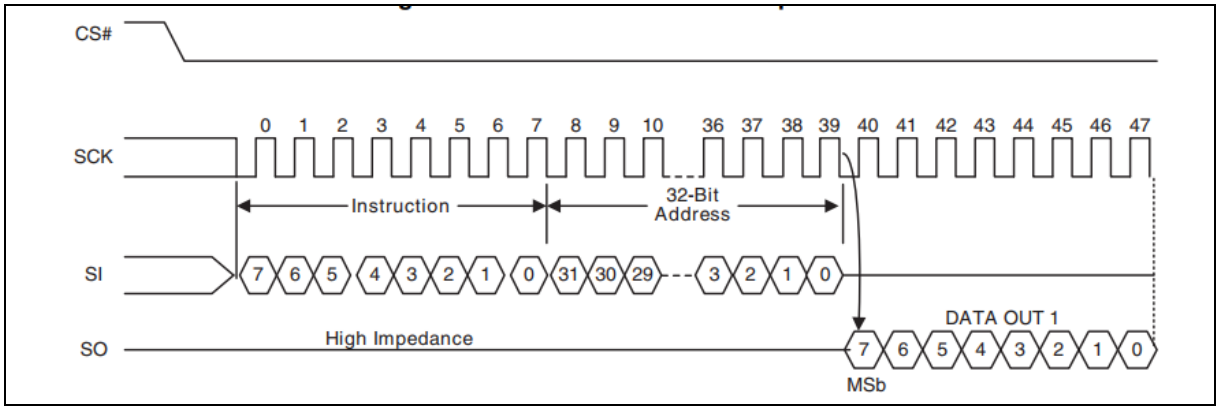


Figure 115 PPB Read Instruction for SPI Mode

10.2.64. PPB Program (PPBP E3h)

Before the PPB Program (PPBP) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The PPBP command is entered by driving CS# to the logic LOW state, followed by the instruction, followed by the 32-bit address selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be zero).

The PPBP command affects the P_ERR and WIP bits of the Status and Configuration Registers in the same manner as any other programming operation.

CS# must be driven to the logic HIGH state after the last bit of address has been latched in. If not, the PPBP command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PPBP operation is initiated. While the PPBP operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a 1 during the self-timed PPBP operation, and is a 0 when it is completed. When the PPBP operation is completed, the Write Enable Latch (WEL) is set to a 0

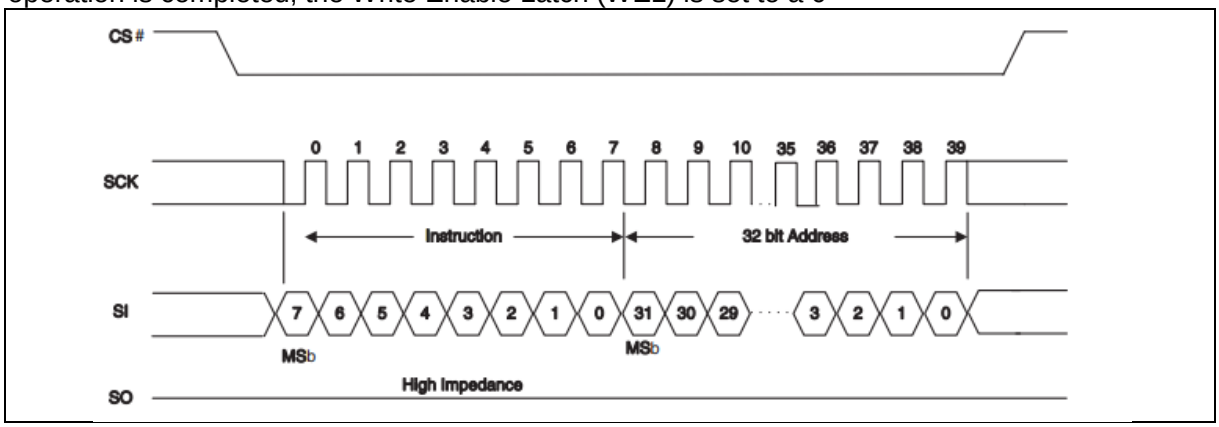


Figure 116 PPB Read Instruction for SPI Mode

10.2.65. PPB Erase (PPBE E4h)

The PPB Erase (PPBE) command sets all PPB bits to 1. Before the PPB Erase command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction E4h is shifted into SI by the rising edges of the SCK signal.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. This will initiate the beginning of internal erase cycle, which involves the pre-programming and erase of the entire PPB memory array. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction, the PPB erase operation will not be executed. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate a 1 when the erase cycle is in progress and a 0 when the erase cycle has been completed. Erase suspend is not allowed during PPB Erase.

10.2.66. Write PPB Lock Register(A6h)

The Write PPB Lock Bit (WRPLB) command clears the PPB Lock Register to zero. Before the WRPLB command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The WRPLB command is entered by driving CS# to the logic low state, followed by the instruction. CS# must be driven to the logic high state after the eighth bit of instruction has been latched in. If not, the WRPLB command is not executed. When the WRPLB operation is completed, the Write Enable Latch (WEL) is set to a 0.

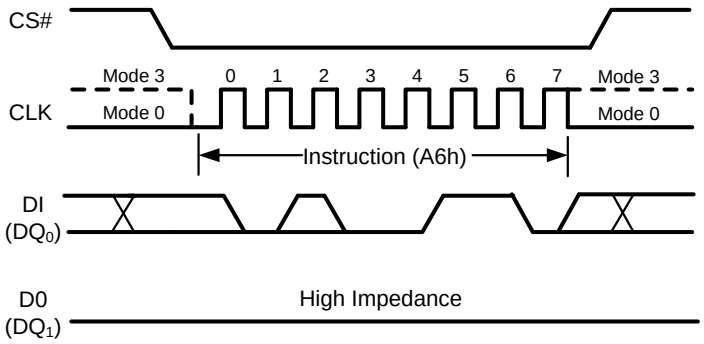


Figure 117 Write PPBL Register Instruction

10.2.67. Enable Reset (66h) and Reset (99h)

Because of the small package and the limitation on the number of pins, the FM25Q256I3 provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Read parameter setting P7-P0, Continuous Read Mode bit setting M7-M0 and Wrap Bit setting W6-W4.

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately 100μs to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit in Status Register before issuing the Reset command sequence.

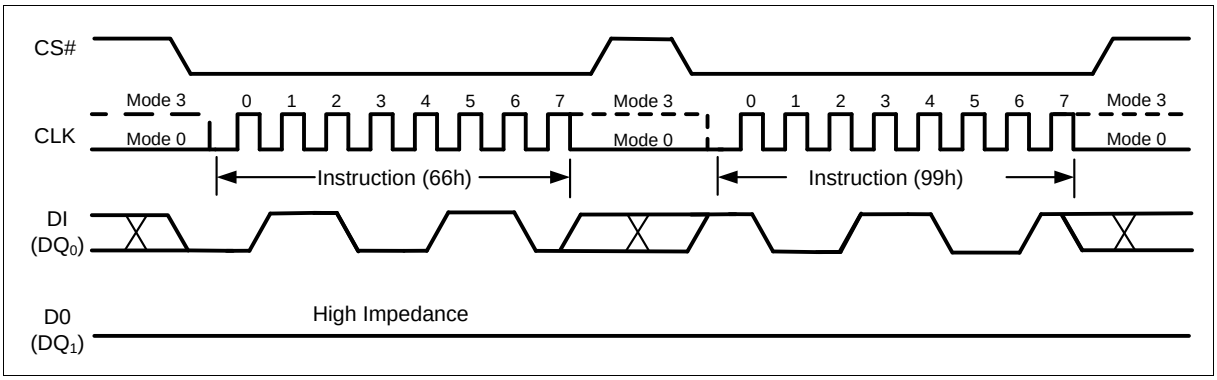


Figure 118 Enable Reset and Reset Instruction Sequence (SPI Mode)

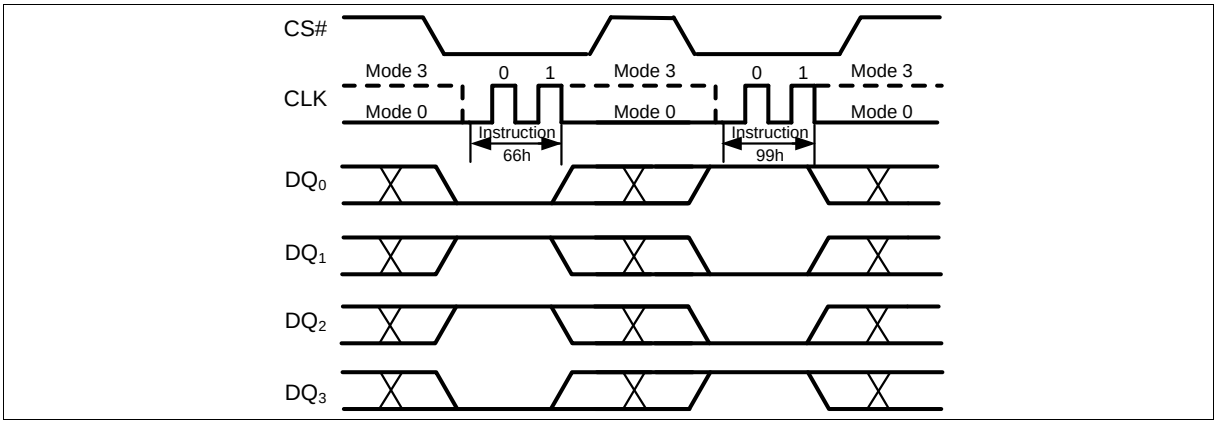


Figure 119 Enable Reset and Reset Instruction Sequence (QPI Mode)

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on I/O Pin with Respect to Ground	-0.5V to V_{CC}+0.4V
Transient Input/Output Voltage(note: overshoot <20ns)	-2.0V to V_{CC} +2.0V
V_{CC}	-0.5V to 4.0V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 120 Maximum Negative Overshoot Waveform

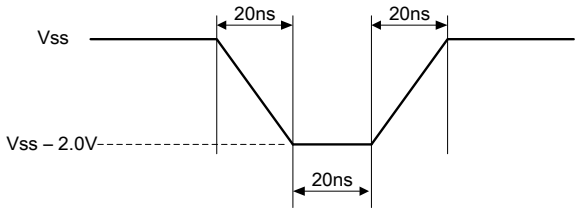
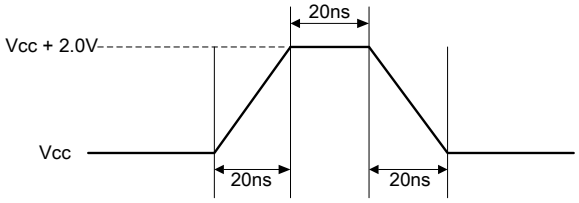


Figure 121 Maximum Positive Overshoot Waveform



11.2. Pin Capacitance

Applicable over recommended operating range from: T_A = 25°C, f = 1 MHz.

Symbol	Test Condition	Max	Units	Conditions
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}(1)	Output Capacitance	8	pF	V_{OUT} = 0V

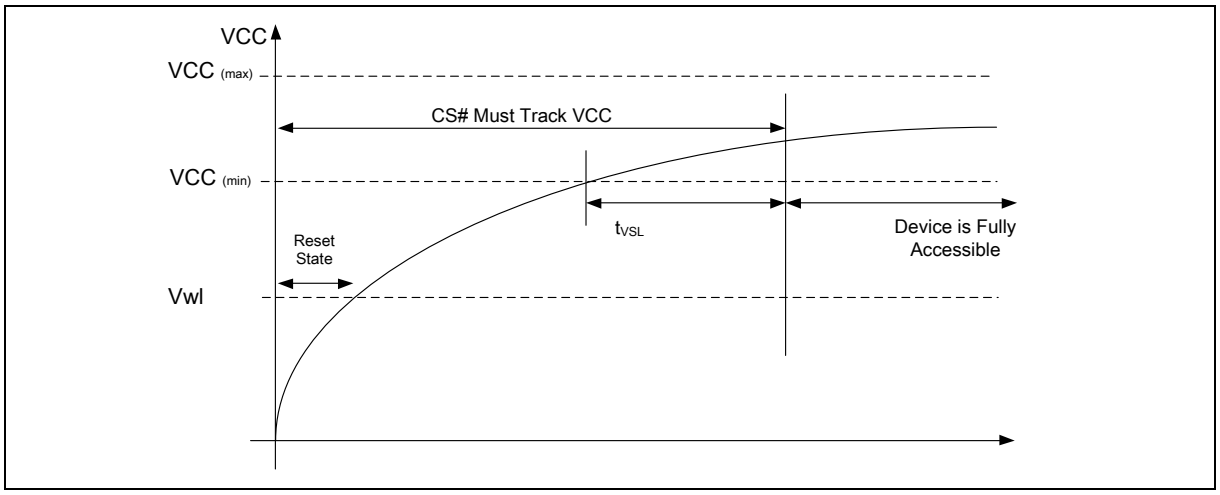
Note: 1. This parameter is characterized and is not 100% tested.

11.3. Power-up and Power-Down Timing

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER		SPEC		UNIT
			MIN	MAX	
t_{VSL}	VCC (min) to CS# Low		200		µs
V_{WI}	Write Inhibit Threshold Voltage		1	2	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur	Deep Power Down		0.4	V
		others		0.9	V
t_{PWD}	The minimum duration for ensuring initialization will occur		1		ms

Note: 1. this parameter is characterized and is not 100% tested.



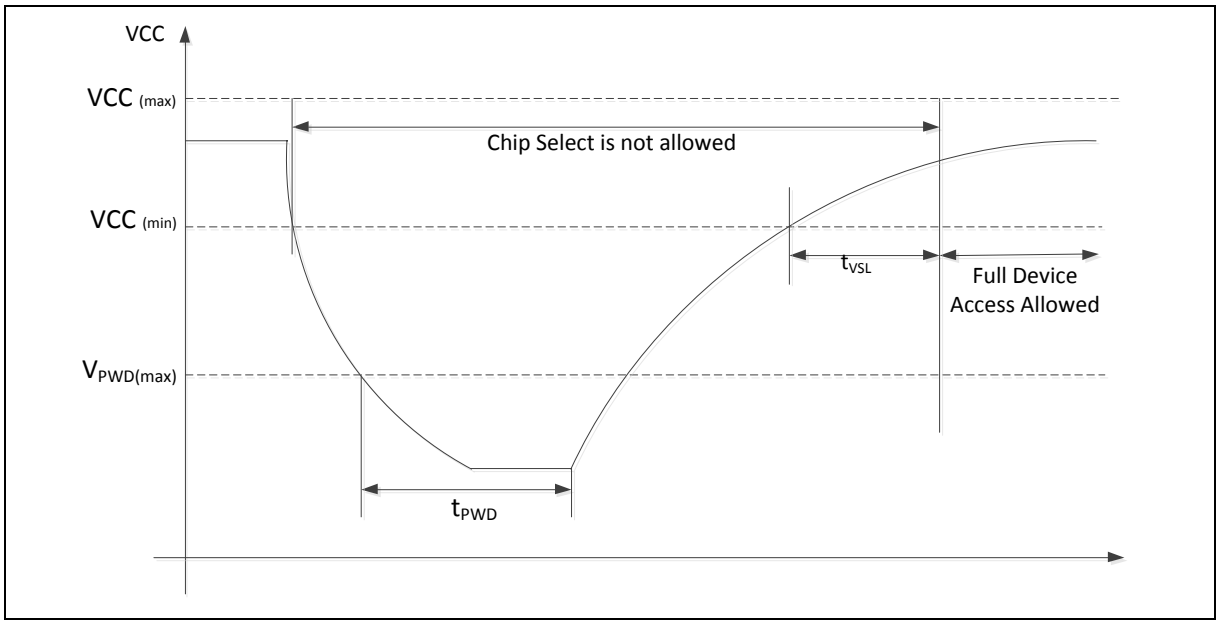


Figure 122 Power-up Timing& Power Up/Down and Voltage Drop

11.4. DC Electrical Characteristics

Table 9 DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Vcc	Supply Voltage		2.7		3.6	V
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	V_{CC}=3.6V, CS# = V_{CC}, V_{IN} = Vss or V_{CC}		5	10	μA
I_{CC2}	Deep Power-down Current			1	5	μA
I_{CC3}	Current Read Data / Dual / Quad 50MHz(1)	V_{CC}=3.6V CLK=0.1V_{CC}/0.9V_{CC} DQ open			15	mA
I_{CC3}	Current Read Data /				25	mA

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
	Dual / Quad 100MHz(1)					
I_{CC4}	Operating Current (WRSR)	V_{CC}=3.6V,CS#=V_{CC}		10	20	mA
I_{CC5}	Operating Current (PP)			10	20	mA
I_{CC6}	Operating Current (SE)			10	20	mA
I_{CC7}	Operating Current (BE)			10	20	mA
V_{IL}(2)	Input Low Voltage		-0.5		0.2V_{CC}	V
V_{IH}(2)	Input High Voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC}-0.2			V

Notes:
1. Checker Board Pattern.
2. V_{IL} min and V_{IH} max are reference only and are not tested.

11.5. AC Measurement Conditions

Table 10 AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load Capacitance		20	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

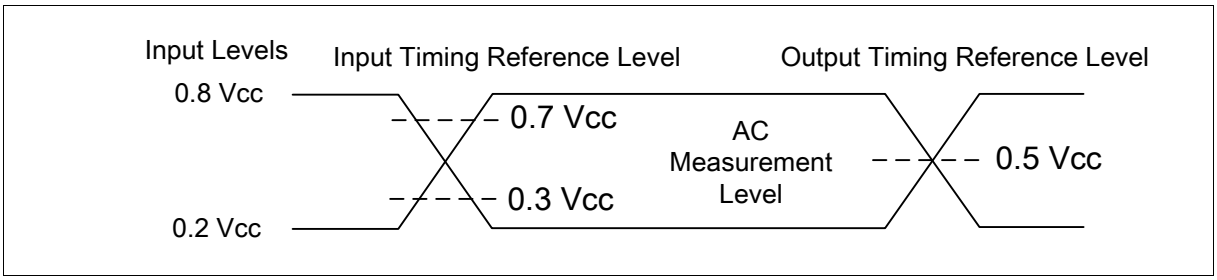


Figure 123 AC Measurement I/O Waveform

11.6. AC Electrical Characteristics

Table 11 AC Characteristics

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_{R1}	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR			100	MHz
F_{R2}	Serial Clock Frequency for DTR instructions			50	MHz

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
f_R	Serial Clock Frequency for READ, RDSR, RDID			50	MHz
t_{CH1}(1)	Serial Clock High Time	45% (1/ F_R)			ns
t_{CL1}(1)	Serial Clock Low Time	45% (1/ F_R)			ns
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time	20			ns
t_{SHQZ}(2)	Output Disable Time			7	ns
t_{CLQX}	Output Hold Time	1.5			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}(2)	HOLD# Low to High-Z Output			12	ns
t_{HHQX}(2)	HOLD# High to Low-Z Output			7	ns
t_{CLQV}	Output Valid from CLK			7	ns
t_{WHSL}	Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time after CS# High	100			ns
t_{DP}(2)	CS# High to Deep Power-down Mode			3	µs
t_{RES1}(2)	CS# High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2}(2)	CS# High to Standby Mode with Electronic Signature Read			3	µs
t_{SUS}(2)	CS# High to next Instruction after Suspend			40	µs
t_{RS}	Latency Between Resume And Next Suspend	100			µs
t_W	Write Status Register Cycle Time		10	15	ms
t_{BP}	Byte Program Time		30	50	ms
t_{PP}	Page Program Time		0.7	3	ms
t_{SE}	Sector Erase Time		45	500	ms
t_{BE}	Block Erase Time (32KB)		200	1500	ms
t_{BE}	Block Erase Time (64KB)		250	2000	ms
t_{CE}	Chip Erase Time		90	600	s
t_{RST}	Reset pulse width	1			us

Notes:

1. $T_{CH1}+T_{CL1} >= 1 / F_{CLK}$;
2. This parameter is characterized and is not 100% tested.

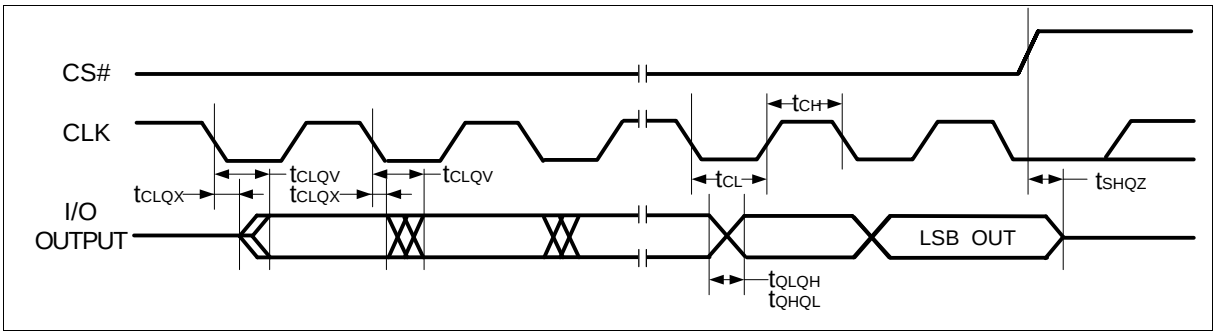


Figure 124 Serial Output Timing

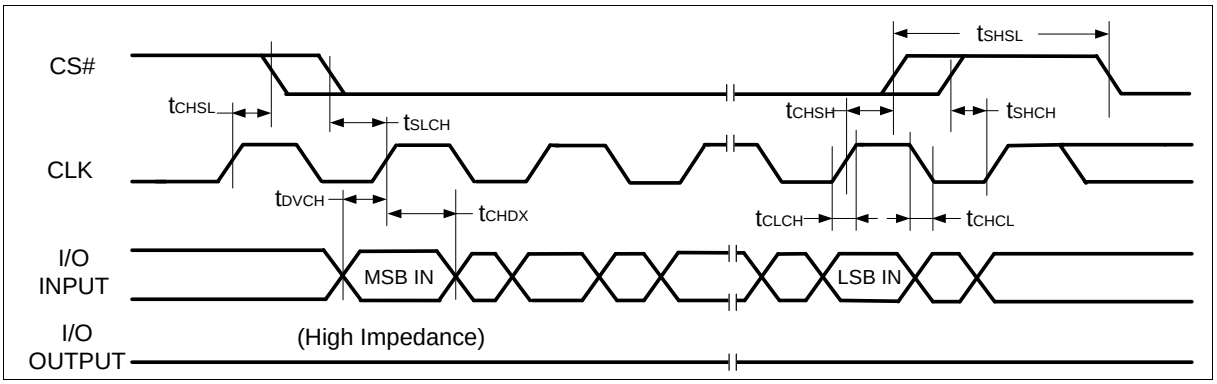


Figure 125 Serial Input Timing

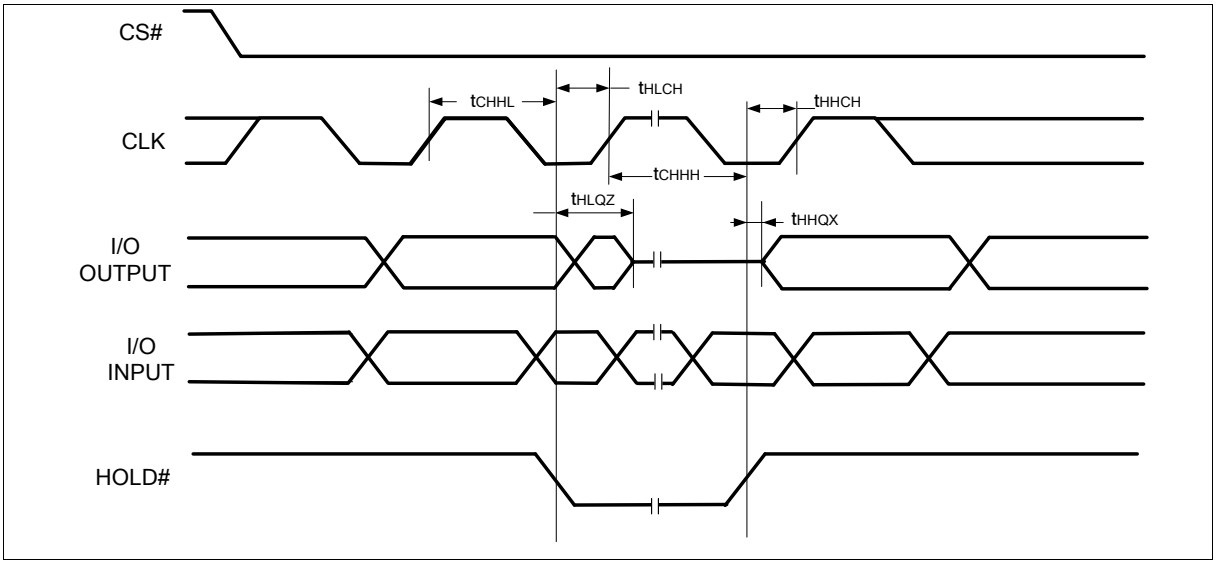


Figure 126 Hold Timing

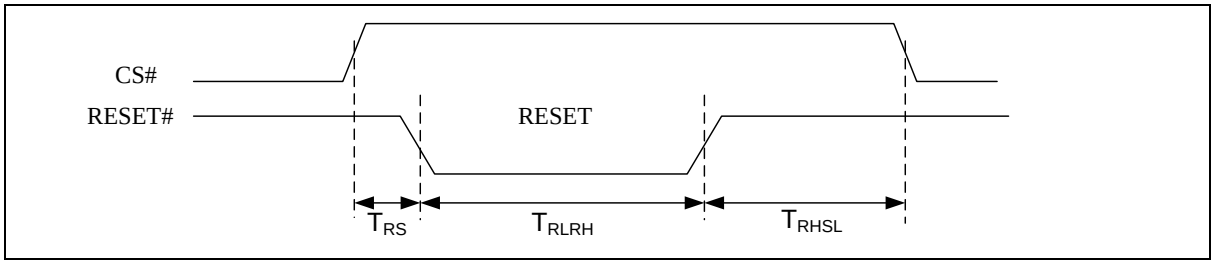


Figure 127 RESET Timing

12. Ordering Information

FM 25Q 256I3 -XXX -C -H M

Company Prefix

FM = Fudan Microelectronics Group Co.,ltd

Product Family

25Q =2.7~3.6V Serial Flash with 4KB Uniform-Sector,
Dual/Quad SPI & QPI

Product Density

256I3 = 256M-bit

Package Type

SOA = 16-pin SOP (300mil）
DNA = 8-pin TDFN (6mm x 5mm)
DND = 8-pin TDFN (8mm x 6mm)
BGB = 24-ball TFBGA (8mm x 6mm)
SOB = 8-pin SOP (208mil）

Product Carrier (1)

U = Tube
T = Tape and Reel
A = Tray

HSF ID Code

G = RoHS Compliant, Halogen-free, Antimony-free

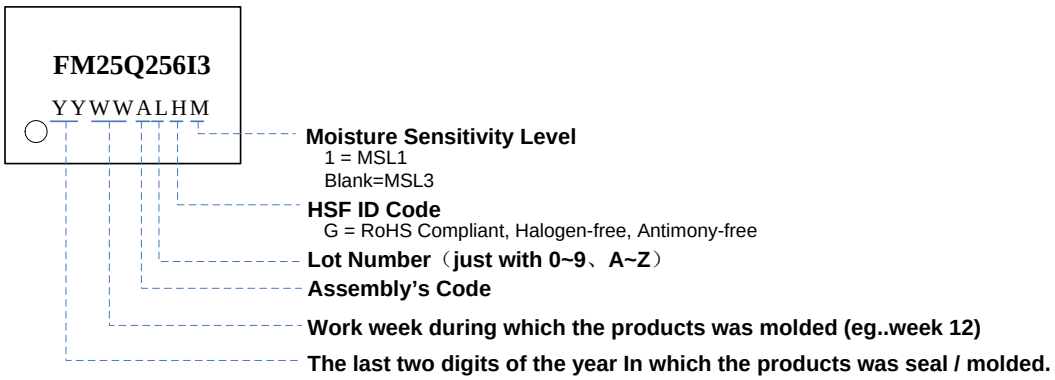
MSL Code

3 = MSL3

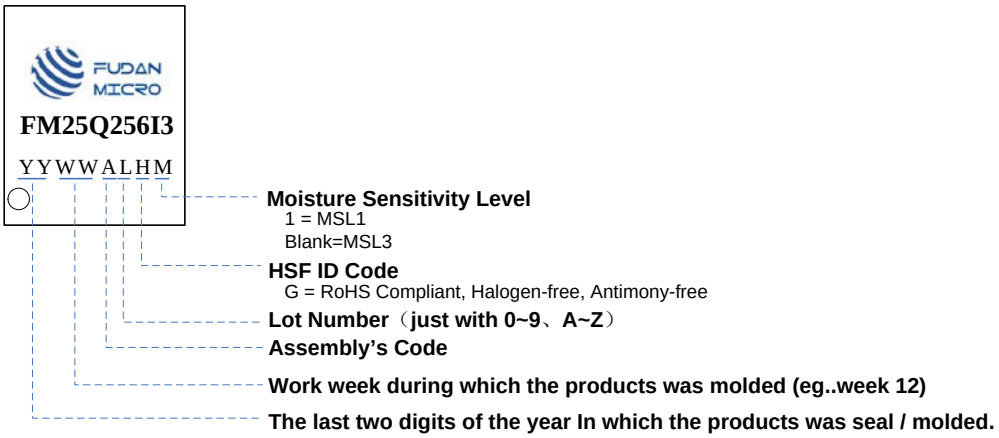
Note (1): Tube for SOA/SOB package type； Tap reel for SOA/DNA/DND/SOB package type；Tray for DND/BGB package type.

13. Part Marking Scheme

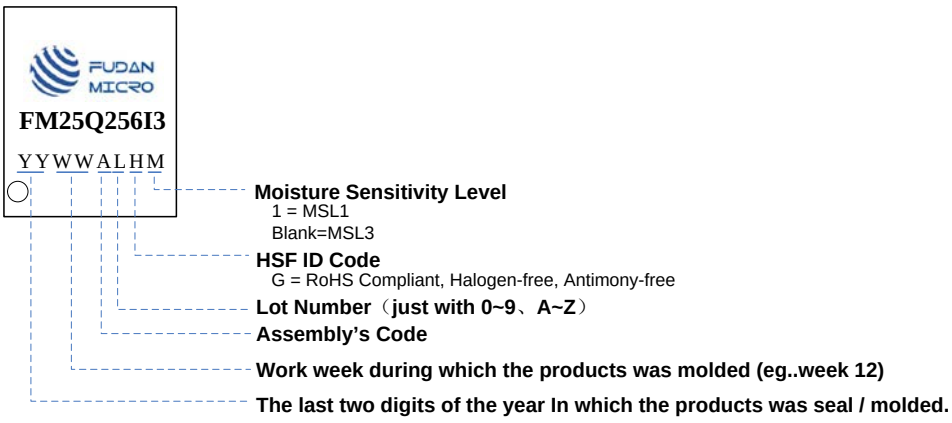
13.1. SOP16 (300mil)



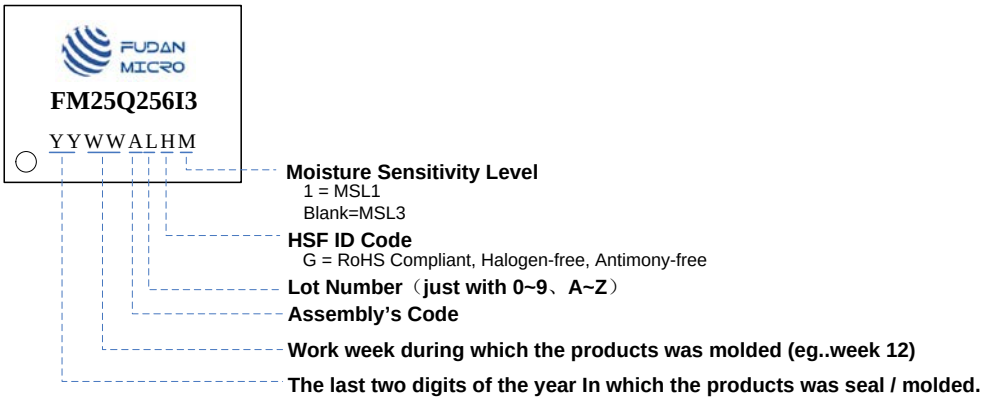
13.2. TDFN8 (6x5mm)



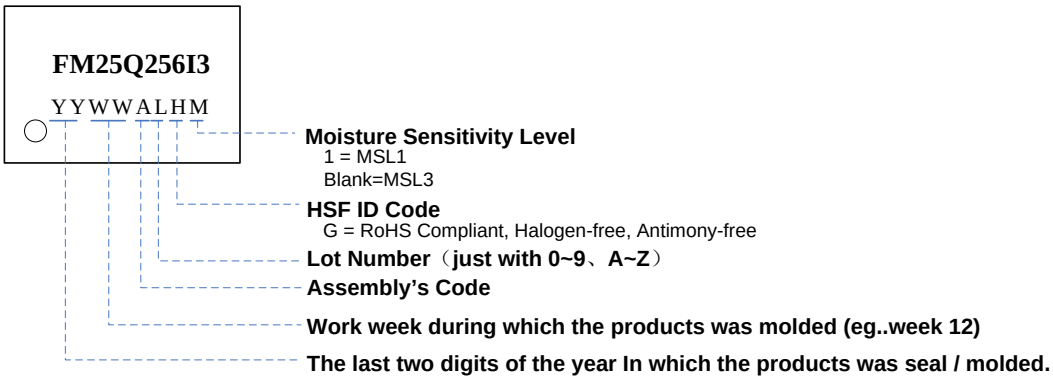
13.3. TDFN8 (8x6mm)



13.4. BGA24(8x6mm)

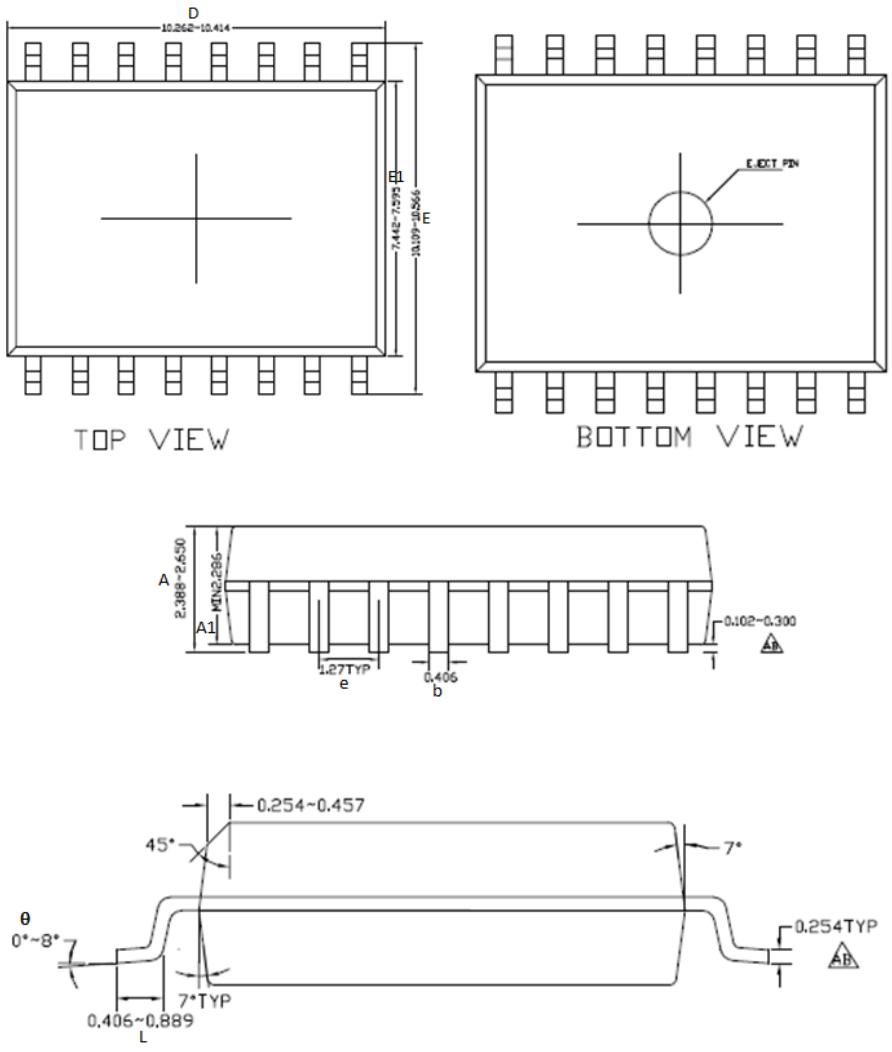


13.5. SOP8 (208mil)



14. Packaging Information

14.1. SOP16 (300mil)

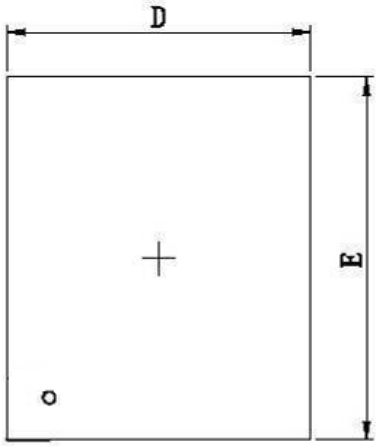


Symbol	MIN	MAX
A	2.388	2.650
A1	2.286	-
b	0.406(BSC)	
D	10.262	10.414
E1	7.442	7.595
E	10.109	10.566
e	1.270(BSC)	
L	0.406	0.889
θ	0°	8°

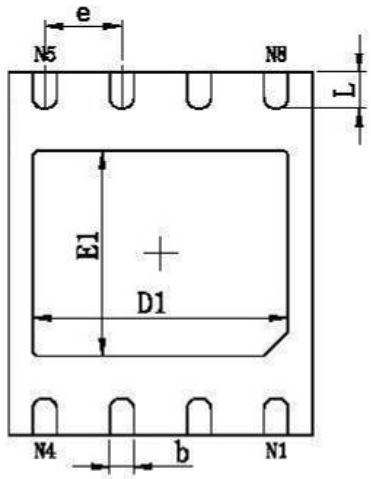
NOTE:

1. Dimensions are in Millimeters.

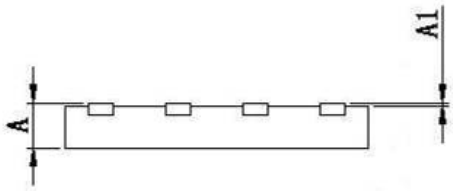
14.2. TDFN8 (6x5mm)



Top View



Bottom View



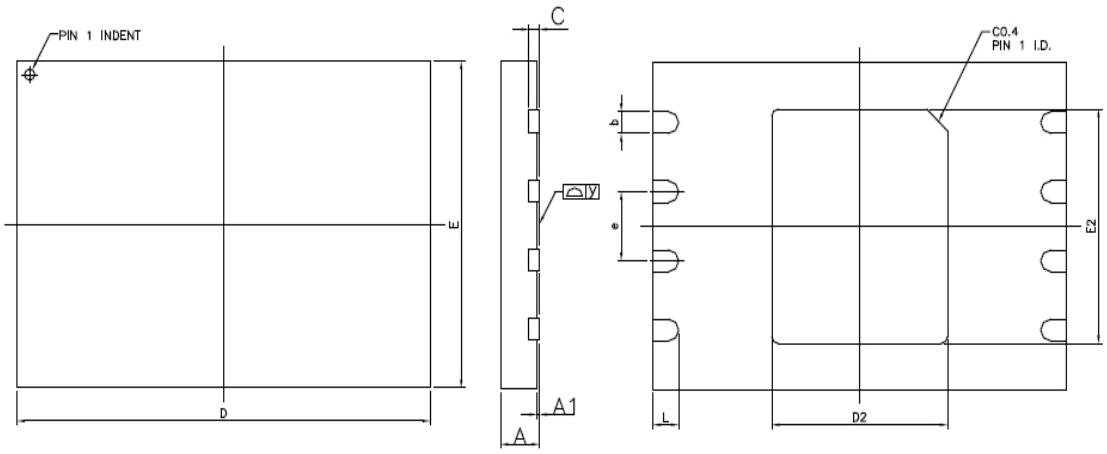
Side View

Symb□l	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
D1	4.10	4.30
D	4.90	5.10
E1	3.300	3.500
E	5.90	6.10
b	0.350	0.450
e	1.270TYP	
L	0.550	0.650

NOTE:

1. **Dimensions are in Millimeters.**

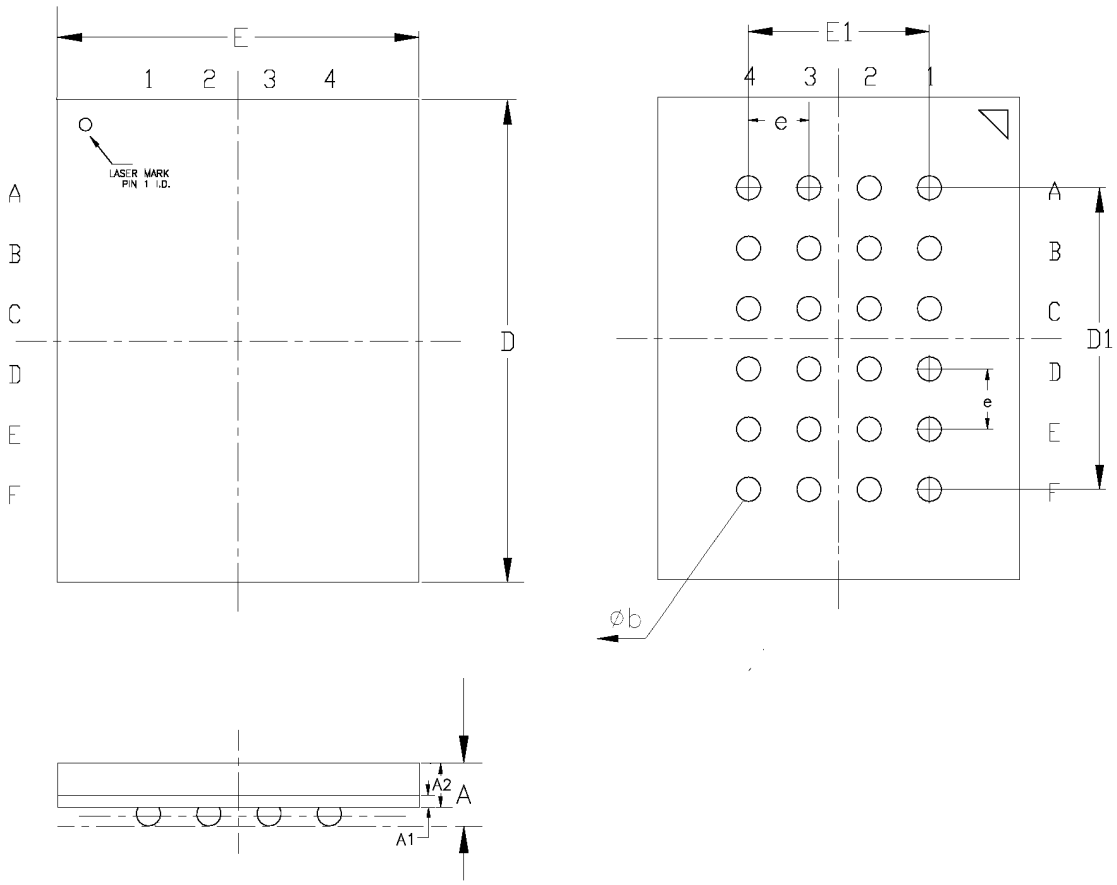
14.3. TDFN8 (8x6mm)



Symbol	MIN	MAX
e	1.270 BSC	
D	7.900	8.100
E	5.900	6.100
L	0.450	0.550
A	0.700	0.800
A1	0.000	0.050
C	0.180	0.250
b	0.350	0.450
D2	3.300	3.500
E2	4.200	4.400

Note:
1. Dimensions are in Millimeters.

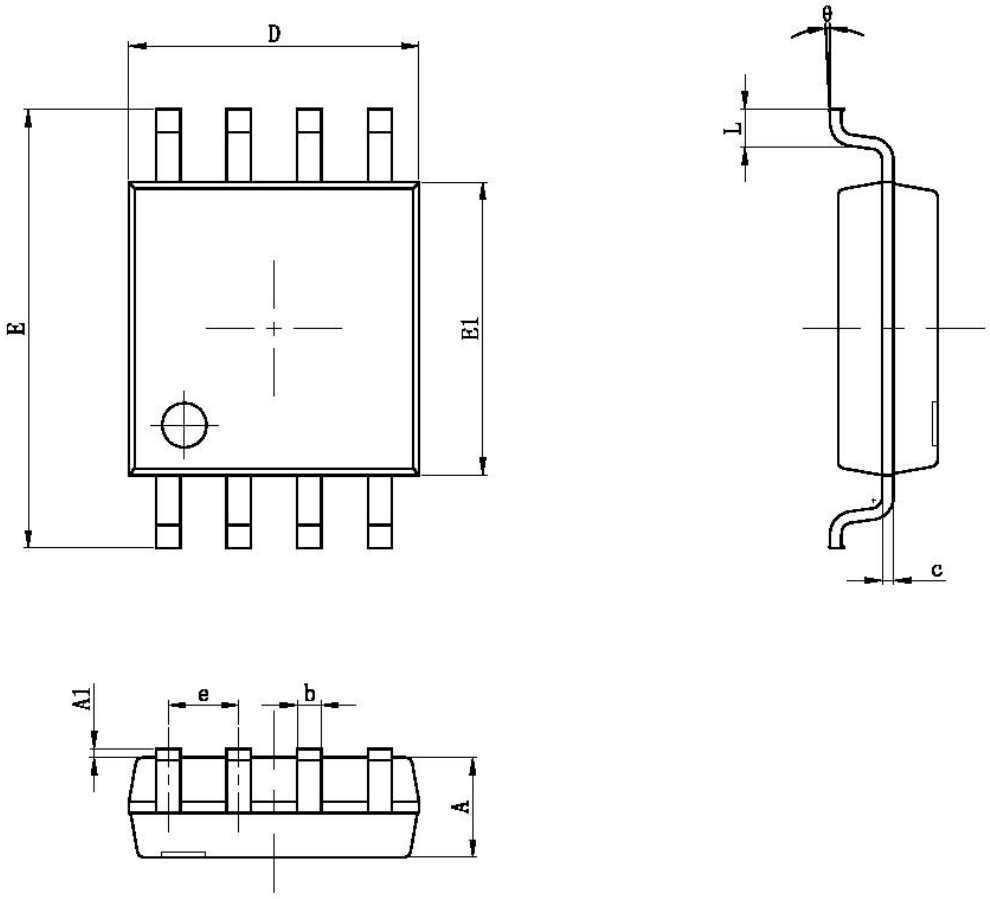
14.4. BGA24 (8x6mm)



Symbol	MIN	MAX
A	---	1.20
A1	0.17	0.25
A2	0.69	0.79
D	7.90	8.10
D1	5.00 BSC	
E	5.90	6.10
E1	3.00 BSC	
e	1.00 BSC	
b	0.350	0.450

Note:
1. Dimensions are in Millimeters.

14.5. SOP8 (208mil)



Symbol	MIN	MAX
A	– –	2.150
A1	0.050	0.250
b	0.350	0.500
c	0.100	0.250
D	5.130	5.330
E1	5.180	5.380
E	7.700	8.100
e	1.270(BSC)	
L	0.500	0.850
θ	0°	8°

NOTE:
1.Dimensions are in Millimeters.

15. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
preliminary	Apr. 2022	113		Initial Document Release.

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