The documentation and process conversion measures necessary to comply with this document shall be completed by 29 June 2024.

INCH-POUND

MIL-PRF-19500/545L
w/AMENDMENT 2
29 March 2024
SUPERSEDING
MIL-PRF-19500/545L
w/AMENDMENT 1
27 September 2022

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, PNP, SILICON, POWER, ENCAPSULATED (THROUGH-HOLE AND SURFACE MOUNT PACKAGES) AND UN-ENCAPSULATED (DIE), TYPES 2N5151, 2N5153, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for PNP, silicon, power transistors for use in high-speed power-switching applications. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type and Two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device type as specified in MIL-PRF-19500. Provisions for radiation hardness assurance (RHA) to eleven radiation levels (“E”, “K”, “U”,"M", "D", "P", "L", "R", "F", "G", and "H" are provided for JANTXV and JANS product assurance levels.

1.2 Package outlines. The device package outlines are as follows: similar to TO-205 in accordance with figure 1 and U3 in accordance with figure 2 for all encapsulated device types. See figures 3, 4, and 5 for unencapsulated devices.

1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C.

Types	P_T T_A = +25°C (1)	P_T T_C = +25°C (1)	$R_{\theta JA}$ (2)	$R_{\theta JC}$ (2)	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_C (3)	Reverse pulse energy (4)	T_{STG} and T_J
	W	W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc	mj	°C
2N5151, L	1	10	175	10	-100	-80	-5.5	-2	-10	15	-65 to + 200
2N5153, L	1	10	175	10	-100	-80	-5.5	-2	-10	15	
2N5151U3	1.16	100	150 (5)	1.75	-100	-80	-5.5	-2	-10	15	-65 to + 200
2N5153U3	1.16	100	150 (5)	1.75	-100	-80	-5.5	-2	-10	15	

(1) See figures 6, 7, 8, and 9 for temperature-power derating curves.
(2) See figures 10, 11, and 12 for transient thermal impedance graph.
(3) This value applies for Pw ≤ 8.3 ms, duty cycle ≤ 1 percent.
(4) This rating is based on the capability of the transistors to operate safely in the unclamped inductive load energy test circuit, see subgroup 5 of the group A inspection table and figure 13.
(5) Mounted on an FR4 printed circuit board.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A
FSC 5961

* 1.4 Primary electrical characteristics at T_C = +25°C.

Limits	h_{FE2} (1) V_{CE} = -5 V I_C = -2.5 A dc		$\|h_{fe}\|$ V_{CE} = -5 V I_C = -500 mA dc f = 10 MHz		$V_{BE(sat)2}$ (1) I_C = -5 A dc I_B = -500 mA dc	$V_{CE(sat)2}$ (1) I_C = -5 A dc I_B = -500 mA dc	C_{obo} V_{CB} = -10 V dc I_E = 0 f = 1 MHz
	2N5151 (2)	2N5153 (2)	2N5151 (2)	2N5153 (2)			
					V dc	V dc	pF
* Min	30	70	6	7			
Max	90	200			-2.2	-1.5	250
(TO-205) * Max (U3)	90	200			-2.2	-1.5	250

(1) Pulsed, see 4.5.1.
(2) The limits specified apply to all package outlines unless otherwise stated.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

1.5.1 JAN certification mark and quality level.

1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: “E”, “K”, “U”, "M", "D", "P", "L", "R", "F", "G", and "H").

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "5151" and "5153".

1.5.3.3 Suffix letters. The suffix letter "L" is used on devices that are packaged in the TO-205 package of figure 1 that have a long lead length: 1.500 inches (38.10 mm) minimum and 1.750 inches (44.45 mm) maximum. Devices with no suffix have standard length leads of 0.5 inch (12.7 mm) minimum to .75 inch (19.1 mm) maximum in figure 1. The suffix letters "U3" are used on devices that are packaged in the surface mount package of figure 2.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

1.5.5 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "B", "C" and "D".

1.6 Radiation features. The following radiation features are applicable for RHA devices supplied to this specification sheet.

1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750 are as follows:

For device type 2N5151, 2N5151L, AND 2N5151U3:.....300 krads(Si) 1/
For device type 2N5153, 2N5153L, AND 2N5153U3:.....300 krads(Si) 1/

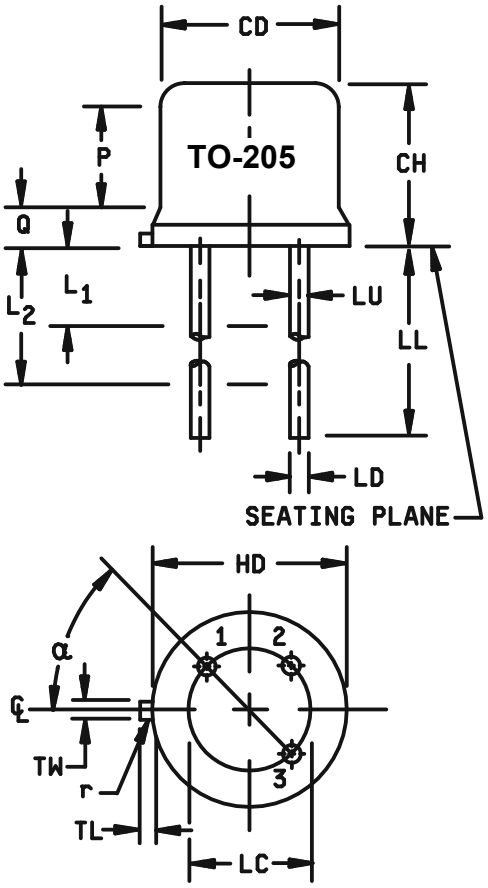
* 1.6.2 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition D (dose rate ≤ 10 mrad(Si)/s) of method 1019 of MIL-STD-750 are as follows:

* For device type 2N5153, 2N5153L, AND 2N5153U3: .....100 krads(Si) 2/

1/ The manufacturers supplying these device types have performed characterization testing in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750. The radiation end point limits are guaranteed only to a maximum TID level of 300 krads(Si).

* 2/ The manufacturers supplying these device types have performed characterization testing in accordance with condition D (dose rate ≤ 10 mrad(Si)/s) of method 1019 of MIL-STD-750. The radiation end point limits are guaranteed only to a maximum TID level of 100 krads(Si).

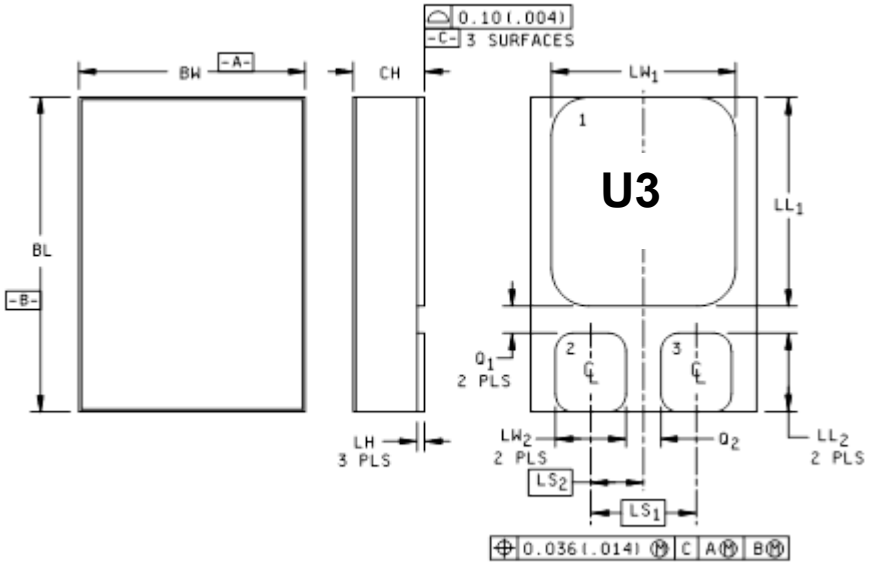
Symbol	Dimensions				Notes
	IN	IN	mm	mm	
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	6
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		7
LD	.016	.021	0.41	0.53	8, 9
LL					8, 9, 13, 14
LU	.016	.019	0.41	0.48	8, 9
L_1		.050		1.27	8, 9
L_2	.250		6.35		8, 9
Q		.050		1.27	6
TL	.029	.045	0.74	1.14	4, 5
TW	.028	.034	0.71	0.86	3
r		.010		0.25	11
α	45° TP		45° TP		7
P	.100		2.54		



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
4. TL measured from maximum HD.
5. Outline in this zone is not controlled.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
8. LU applied between L_1 and L_2. LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
9. All three leads.
10. The collector shall be electrically and mechanically connected to the case.
11. r (radius) applies to both inside corners of tab.
12. * For transistor types 2N5151 and 2N5153, LL is .5 inch (13 mm) minimum, and .75 inch (19 mm) maximum.
13. * For transistor types 2N5151L and 2N5153L, LL is 1.5 inch (38 mm) minimum and 1.75 inch (44.4 mm). maximum.
14. * Lead designation, depending on device type, shall be as follows: lead numbering; lead 1 = emitter, lead 2 = base, and lead 3 = collector.

FIGURE 1. Physical dimensions (TO-205).



Symbol	Dimensions			
	IN	IN	mm	mm
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH	.1085	.1205	2.76	3.06
LH	.010	.020	0.25	0.51
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
Q1	.030		0.762	
Q2	.030		0.762	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Terminal 1 - collector, terminal 2 - base, terminal 3 - emitter.

SCHEMATIC

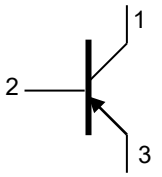
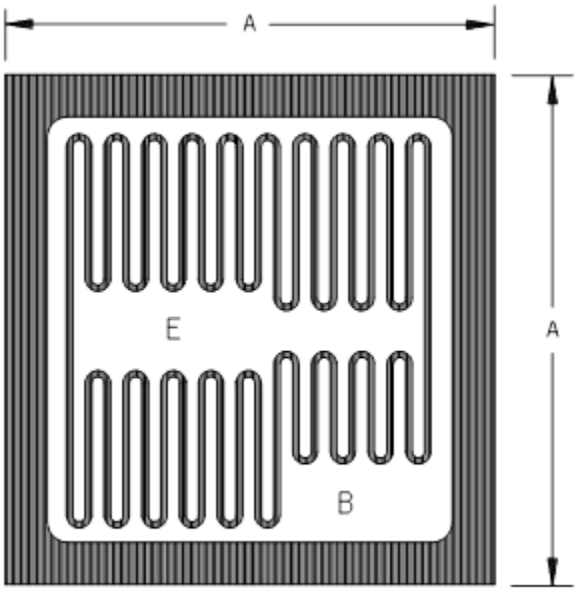


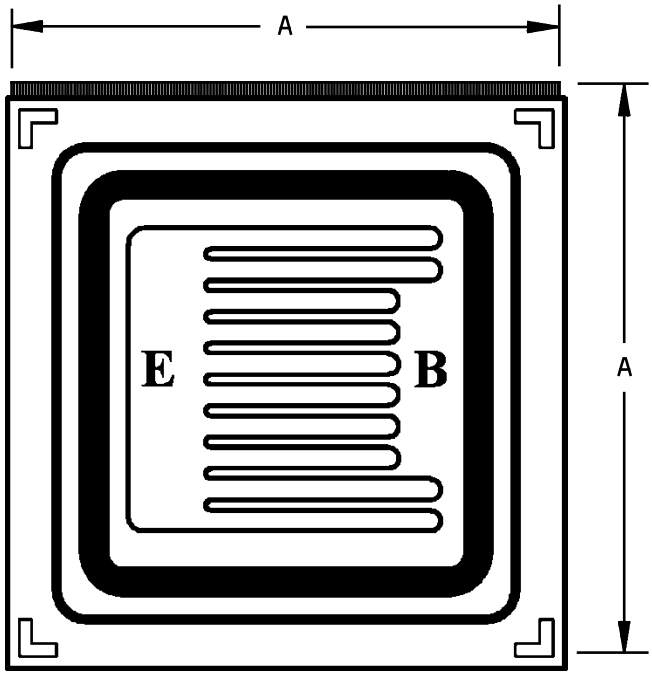
FIGURE 2. Physical dimensions and configuration for surface mount (U3).



Ltr	Dimensions			
	in	in	mm	mm
	Min	Max	Min	Max
A	.100	.105	2.54	2.67

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 inch (0.13 mm).
4. The physical characteristics of the die are:
   Thickness: .0078 inch (0.198 mm) nominal, tolerance is ±.005 inch (0.13 mm).
   Top metal: Aluminum, 25,000 Å minimum, 33,000 Å nominal.
   Back metal: Gold 1,500 Å minimum, 2,500 Å nominal.
   Back side: Collector.
   Bonding pad: .012 inch (0.305 mm) min. x .030 inch (0.761 mm) minimum.

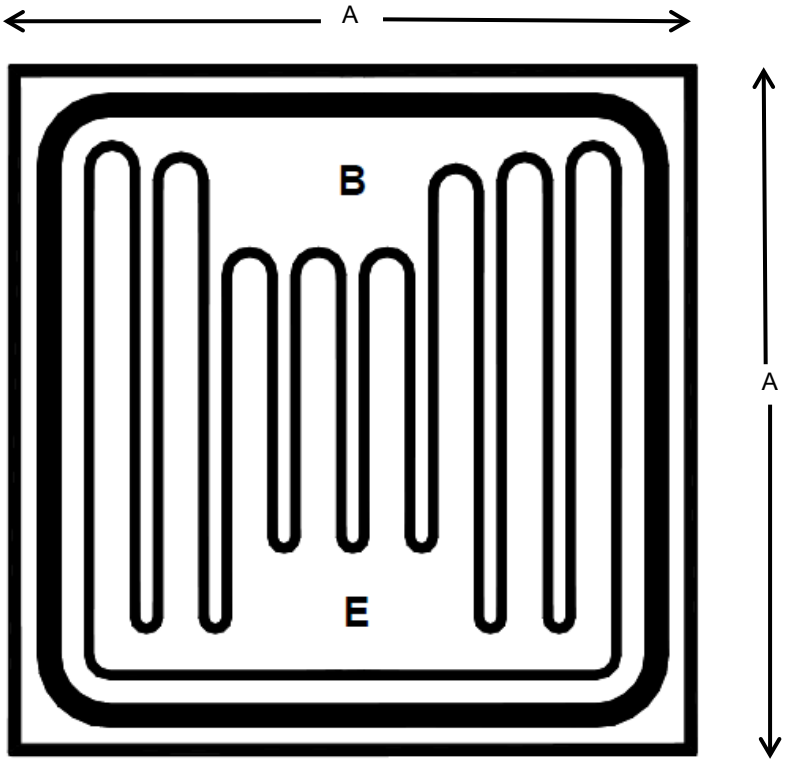
FIGURE 3. JANHC and JANKC (B-version) die dimensions.



Ltr.	Dimensions			
	IN	IN	mm	mm
	Min	Max	Min	Max
A	.126	.130	3.20	3.30

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
   Thickness: .010 inch (0.25 mm) ±.0015 inch (0.038 mm) nominal.
   Top metal: Aluminum 30,000 Å minimum, 33,000 Å nominal.
   Back metal: A. Al/Ti/Ni/Ag15kÅ/2kÅ/7kÅ/7kÅ min. 18kÅ/3kÅ/10kÅ/10kÅ nom.
   B. Gold 2,500 Å minimum, 3,000 Å nominal.
   Back side: Collector.
   Bonding pad: .012 inch (0.305 mm) min. x .030 inch (0.761 mm) minimum.

FIGURE 4. JANHC and JANKC (C-version) die dimensions.



Backside: Collector

Dimensions				
LTR	IN	IN	mm	mm
	Min	Max	Min	Max
A	.118	.122	3.0	3.1

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm).
4. The physical characteristics of the die are:
   - Thickness: .0135 inch (0.34 mm) nominal, tolerance is ±.0015 inch (0.04 mm).
   - Top metal: Aluminum, 54,000 Å minimum, 60,000 Å nominal.
   - Back metal: Gold 6,400 Å minimum, 8,000 Å nominal.
   - Back side: Collector.
   - Bonding pad: B = .038 x .022 inch (0.97 x 0.56 mm)
     E = .042 x .020 inch (1.07 mm x 0.51 mm)

FIGURE 5. JANHC and JANKC (D-version) die dimensions.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.3 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

(Copies of these documents are available online at https://www.asme.org)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML-19500) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 (similar to TO-205), figure 2 (U3), and figures 3, 4, and 5 (die dimensions) for JANHC and JANKC.

3.4.1 Current density. Current density of internal conductors shall be as specified in MIL-PRF-19500.

3.4.2 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I, II, III, and IV).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table IV tests, the tests specified in table IV herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANS levels	Measurements for JANTX and JANTXV levels
3b	Not applicable	Not applicable
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3)	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3.)
9	I_{CES1} and h_{FE2}	Not applicable
10	48 hours minimum.	48 hours minimum.
11	I_{CES1} and h_{FE2}; ΔI_{CES1} = 100 percent of initial value or -100 nA dc, whichever is greater. Δh_{FE2} = ±20 percent	I_{CES1} and h_{FE2}
12	See 4.3.2	See 4.3.2
13	Subgroups 2 and 3 of table I herein; ΔI_{CES1} = 100 percent of initial value or -100 nA dc, whichever is greater. Δh_{FE2} = ±20 percent	Subgroup 2 of table I herein; ΔI_{CES1} = 100 percent of initial value or -100 nA dc, whichever is greater. Δh_{FE2} = ±20 percent

(1) Shall be performed anytime after temperature cycling, screen 3a, and JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = -10 to -30 V dc, T_A = room ambient as defined in the general requirements of 4.5 of MIL-STD-750. Power shall be applied to the device to achieve a junction temperature, T_J = +175°C minimum and a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3 herein.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit used in screen 3c of 4.3 herein and table I shall comply with the thermal impedance graph on figures 10, 11, and 12 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA of MIL-PRF-19500 (JANS) and 4.4.2.1 herein. See 4.4.2.2 herein JAN, JANTX, and JANTXV group B testing. Delta measurements shall be in accordance with table III herein.

4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

Subgroup	Method	Conditions
B4	1037	V_{CB} = -40 V dc ±1 V, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1027	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample). V_{CB} = -10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3) $T_A \leq$ +35°C. Option 1: 96 hours minimum, sample size in accordance with table E-VIA of MIL-PRF-19500, adjust P_D to achieve T_J = +275°C minimum. Option 2: 216 hours, sample size = 45, c = 0; adjust P_D to achieve T_J = +225°C minimum.
B6	3131	See 4.5.2.

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIC of MIL-PRF-19500. Separate samples may be used for each step. In the event of a group B failure, the manufacturer may pull a new sample at double size from either the failed assembly lot or from another assembly lot from the same wafer lot. If the new assembly lot option is exercised, the failed assembly lot shall be scrapped.

Step	Method	Conditions
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = -10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed group A, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Delta measurements shall be in accordance with table III herein, and only apply to subgroup C6.

4.4.3.1 Quality level JANS (see table E-VII of MIL-PRF-19500).

Subgroup	Method	Condition
C2	2036	Test condition E; (method 2036 MIL-STD 750 not applicable for U3 devices).
C6	1026	1,000 hours at V_{CB} = -10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours. n = 45, c = 0.

4.4.3.2 Quality levels JAN, JANTX and JANTXV (see table E-VII of MIL-PRF-19500).

Subgroup	Method	Condition
C2	2036	Test condition E; not applicable for U3 devices.
C5	3131	$R_{\theta JA}$ for TO-205 (see 1.3), $R_{\theta JC}$ for U3 (see 1.3).
C6		Not applicable.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2 herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table IV herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2. Delta measurements shall be in accordance with table III herein.

4.5 Methods of inspection and test. Methods of inspection and test shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be conducted in accordance with method 3131 of MIL-STD-750. The following details shall apply:

a. Collector current magnitude during power application shall be -500 mA minimum dc.

b. Collector to emitter voltage magnitude shall be -10 V dc.

c. Reference temperature measuring point shall be the case.

d. Reference temperature measuring point shall be within the range +25°C ≤ T_R ≤ +35°C. The chosen reference temperature shall be recorded before the test is started.

e. Mounting arrangement shall be with heat sink to case.

f. See 1.3 for maximum limit of $R_{\theta JC}$.

4.5.3 Displacement damage characterization. For RHA devices, each supplier shall perform a displacement damage characterization. The characterization shall demonstrate exposure versus data and does not indicate pass or fail criteria. The exposure shall be conducted in accordance with method 1017 of MIL-STD-750. The following details shall apply:

a. Samples may be taken from any wafer of the qualification lot.

b. As a minimum, testing shall be at 2E+12 n/cm^2 plus two additional fluence levels chosen by the manufacturer.

c. If the device degrades less than 5 percent of the specification at the highest fluence level, a single data point may be sufficient.

Alternate package options may be substituted for characterization. The displacement damage characterization data shall be made available from the manufacturer.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071					
Solderability 3/ 4/	2026					
Resistance to solvents 3/ 4/ 5/	1022					
Salt atmosphere (corrosion)(For laser marked devices only) 4/	1041	n = 6 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles				
Hermetic seal 4/ 6/ Fine leak Gross leak	1071					
Electrical measurements 4/		Group A, subgroup 2				
Bond strength 3/ 4/	2037	Precondition: T_A = +250°C at t = 24 hrs. or T_A = +300°C at t = 2 hrs.				
De-cap internal visual	2075	n = 4, c = 0				
Subgroup 2						
Thermal impedance 7/	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to emitter	3011	Bias condition D, I_C = -100 mA dc; I_B = 0, pulsed (see 4.5.1)	$V_{(BR)CEO}$	-80		V dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -60 V dc; V_{BE} = 0	I_{CES1}		-1.0	µA dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -100 V dc; V_{BE} = 0	I_{CES2}		-1.0	mA dc
Collector to emitter cutoff current	3041	Bias condition D, V_{CE} = -40 V dc; I_B = 0	I_{CEO}		-50	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = -4 V dc; I_C = 0	I_{EBO1}		-1.0	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = -5.5 V dc; I_C = 0	I_{EBO2}		-1.0	mA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward current transfer ratio	3076	V_{CE} = -5 V dc; I_C = -50 mA dc, pulsed (see 4.5.1)	h_{FE1}			
2N5151, L, and U3 2N5153, L, and U3				20 50		
Forward current transfer ratio	3076	V_{CE} = -5 V dc; I_C = -2.5 A dc, pulsed (see 4.5.1)	h_{FE2}			
2N5151, L, and U3 2N5153, L, and U3				30 70	90 200	
Forward current transfer ratio	3076	V_{CE} = -5 V dc; I_C = -5 A dc, pulsed (see 4.5.1)	h_{FE3}			
2N5151, L, and U3 2N5153, L, and U3				20 40		
Base-emitter voltage (non-saturated)	3066	Test condition B, V_{CE} = -5 V dc; I_C = -2.5 A dc, pulsed (see 4.5.1)	V_{BE}		-1.45	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = -2.5 A dc; I_B = -250 mA dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.45	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = -5 A dc; I_B = -500 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.2	V dc
Collector-emitter saturation voltage	3071	I_C = -2.5 A dc; I_B = -250 mA dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		-0.75	V dc
Collector-emitter saturation voltage	3071	I_C = -5 A dc; I_B = -500 mA dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		-1.5	V dc
Subgroup 3						
High temperature operation:		T_C = +150°C				
Collector to emitter cutoff current	3041	Bias condition A, V_{CE} = -60 V dc; V_{BE} = +2 V dc	I_{CEX}		-25	µA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 3 - continued						
Low temperature operation		T_C = -55°C				
Forward - current transfer ratio	3076	V_{CE} = -5 V dc; I_C = -2.5 A dc; pulsed (see 4.5.1)	h_{FE4}			
2N5151, L, and U3				15		
2N5153, L, and U3				25		
Subgroup 4						
Common-emitter, small-signal, short-circuit, forward-current transfer ratio	3206	V_{CE} = -5 V dc; I_C = -100 mA dc; f = 1 KHz	h_{fe}			
2N5151, L, and U3				20		
2N5153, L, and U3				50		
Magnitude of common-emitter, small-signal short-circuit, forward-current, transfer ratio	3306	V_{CE} = -5 V dc; I_C = -500 mA dc, f = 10 MHz	$\lvert h_{fe} \rvert$			
2N5151, L, and U3				6		
2N5153, L, and U3				7		
Open-circuit output capacitance	3236	V_{CB} = -10 V dc; I_E = 0, f = 1 MHz	C_{obo}		250	pF
Switching time		I_C = -5 A dc; I_{B1} = -500 mA dc	t_{on}		0.5	µs
		I_{B2} = -500 mA dc	t_s		1.4	µs
		$V_{BE(off)}$ = -3.7 V dc	t_f		0.5	µs
		R_L = 6 Ω, (see figure 14)	t_{off}		1.5	µs

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area (dc)	3051	Pre-pulse condition for each test: T_C = +25°C, (see figure 15) Pulse condition for each test: t_p = 1 sec. 1 cycle T_C = +25°C				
Test # 1		V_{CE} = -5.0 V dc, I_C = -2 A dc for TO-205 V_{CE} = -5.8 V dc, I_C = -2 A dc for U3				
Test # 2		V_{CE} = -32 V dc, I_C = -310 mA dc for TO-205 V_{CE} = -32 V dc, I_C = -360 mA dc for U3				
Test # 3		V_{CE} = -80 V dc, I_C = -12.5 mA dc for TO-205 V_{CE} = -80 V dc, I_C = -14.5 mA dc for U3				
Safe operating area (unclamped inductive)	3053	Condition C T_C = +25°C; R_{BB1} = 10 Ω; R_{BB2} = 100 Ω; L = 0.3 mH; RL = 0.1 Ω; V_{CC} = -10 V dc; V_{BB1} = -10 V dc; V_{BB2} = 4 V dc; I_C = -10 A dc (see figure 13)				
End point electrical measurements		See table I, subgroup 2				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ Hermetic seal test is an end-point to temperature cycling in addition to electrical measurements.
7/ For end-point measurements, this test is required for the following subgroups:
Group B, steps 2 and 3 (JAN, JANTX, and JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0V				
Breakdown voltage, collector to emitter	3011	Bias condition D, I_C = -100 mA dc; I_B = 0, pulsed (see 4.5.1)	$V_{(BR)CEO}$	-80		V dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -60 V dc; V_{BE} = 0	I_{CES1}		-2.0	µA dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -100 V dc; V_{BE} = 0	I_{CES2}		-2.0	mA dc
Collector to emitter cutoff current	3041	Bias condition D, V_{CE} = -40 V dc; I_B = 0	I_{CEO}		-100	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = -4 V dc; I_C = 0	I_{EBO1}		-2.0	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = -5.5 V dc; I_C = 0	I_{EBO2}		-2.0	mA dc
Forward-current transfer ratio 2N5151 2N5153	3076	V_{CE} = -5 V dc; I_C = -50 mA dc	[h_{FE1}] 5/	 [10] [25]		
Forward-current transfer ratio 2N5151 2N5153	3076	V_{CE} = -5 V dc; I_C = -2.5 A dc, pulsed	[h_{FE2}] 5/	 [15] [35]	 90 200	
Forward-current transfer ratio 2N5151 2N5153	3076	V_{CE} = -5 V dc; I_C = -5 A dc, pulsed	[h_{FE3}] 5/	 [10] [20]		
Base-emitter voltage (non-saturated)	3066	Test condition B, V_{CE} = -5 V dc; I_C = -2.5 A dc, pulsed (see 4.5.1)	V_{BE}		-1.67	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = -2.5 A dc; I_B = -250 mA dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.67	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = -5 A dc; I_B = -500 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.53	V dc

See footnotes at end of table.

TABLE II. Group D inspection. Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 1 - Continued 4/						
Collector-emitter saturation voltage	3071	I_C = -2.5 A dc; I_B = -250 mA dc; pulsed	$V_{CE(sat)1}$		-0.86	V dc
Collector-emitter saturation voltage	3071	I_C = -5 A dc; I_B = -500 mA dc; pulsed	$V_{CE(sat)2}$		-1.73	V dc
Subgroup 2.						
* Total dose irradiation	1019	Gamma exposure, V_{CES} = -64 V, Condition A, for high dose rate. or Condition D, for low dose rate.				
Breakdown voltage, collector to emitter	3011	Bias condition D, I_C = -100 mA dc; I_B = 0, pulsed (see 4.5.1)	$V_{(BR)CEO}$	-80		V dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -60 V dc; V_{BE} = 0	I_{CES1}		-2.0	µA dc
Collector to emitter cutoff current	3041	Bias condition C, V_{CE} = -100 V dc; V_{BE} = 0	I_{CES2}		-2.0	mA dc
Collector to emitter cutoff current	3041	Bias condition D, V_{CE} = -40 V dc; I_B = 0	I_{CEO}		-100	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = -4 V dc; I_C = 0	I_{EBO1}		-2.0	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = -5.5 V dc; I_C = 0	I_{EBO2}		-2.0	mA dc
Forward-current transfer ratio	3076	V_{CE} = -5 V dc; I_C = -50 mA dc	[h_{FE1}] 5/			
2N5151				[10]		
2N5153				[25]		
Forward-current transfer ratio	3076	V_{CE} = -5 V dc; I_C = -2.5 A dc	[h_{FE2}] 5/			
2N5151				[15]	90	
2N5153				[35]	200	
Forward-current transfer ratio	3076	V_{CE} = -5 V dc; I_C = -5 A dc. pulsed	[h_{FE3}] 5/			
2N5151				[10]		
2N5153				[20]		

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Base-emitter voltage (non-saturated)	3066	Test condition B, V_{CE} = -5 V dc; I_C = -2.5 A dc, pulsed (see 4.5.1)	V_{BE}		-1.67	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = -2.5 A dc; I_B = -250 mA dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.67	V dc
Base-emitter saturation voltage	3066	Test condition A, I_C = -5 A dc; I_B = -500 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.53	V dc
Collector-emitter saturation voltage	3071	I_C = -2.5 A dc; I_B = -250 mA dc	$V_{CE(sat)1}$		-0.86	V dc
Collector-emitter saturation voltage	3071	I_C = -5 A dc; I_B = -500 mA dc	$V_{CE(sat)2}$		-1.73	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to all device types unless otherwise noted.
4/ Subgroup 1 is an optional test and shall be specified on the contract when required.
5/ See method 1019 of MIL-STD-750 for how to determine [h_{FE}] by first calculating the delta ($1/h_{FE}$) from the pre- and post-radiation h_{FE}. Notice that [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

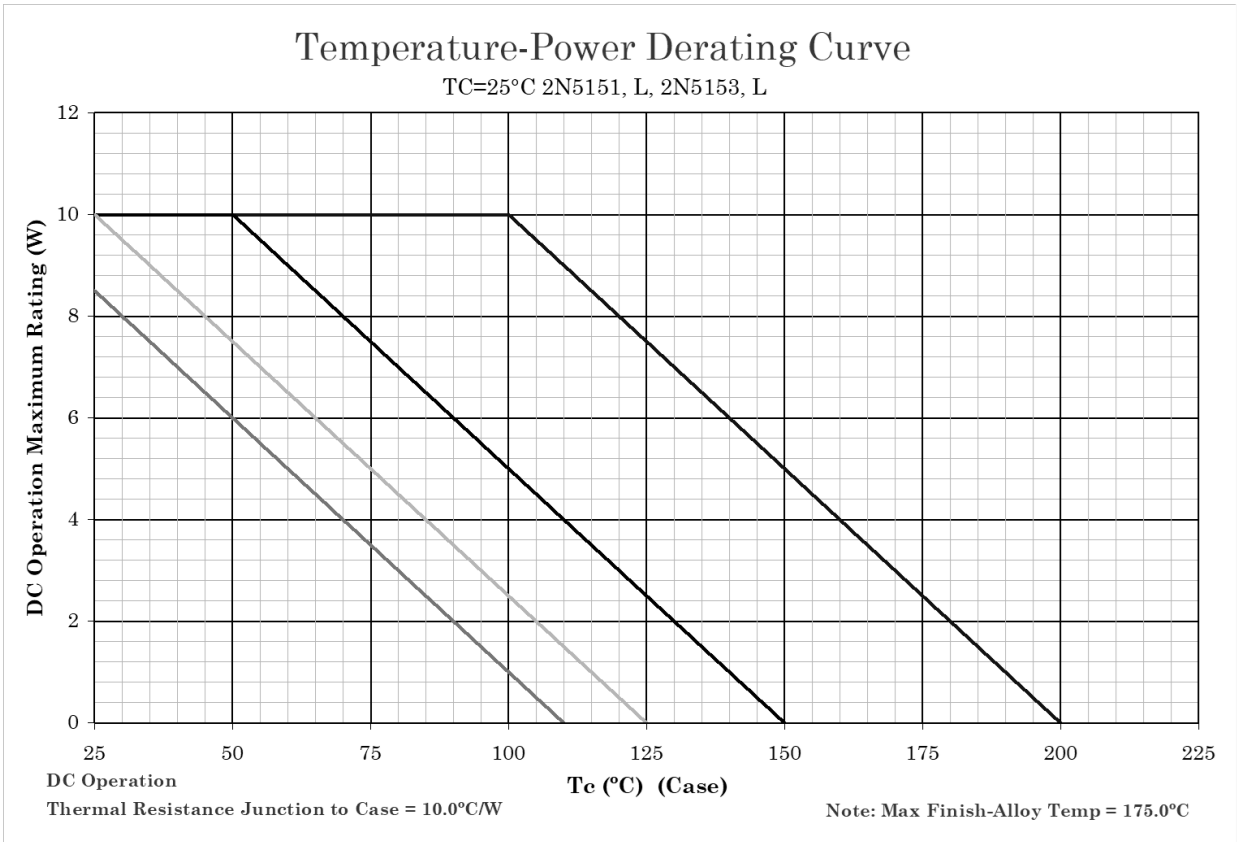
TABLE III. Groups B, C, and E delta and electrical measurements. 1/ 2/ 3/ 4/

Steps	Inspection	MIL-STD-750		Symbol	Limits	Limits	Unit
		Method	Conditions		Min	Max	
1.	Forward - current transfer ratio	3076	I_C = -2.5 A dc; V_{CE} = -5 V dc, pulsed (see 4.5.1).	Δh_{FE2}	±20 percent change from initial reading.		

1/ The delta measurements for table E-VIA (JANS) of MIL-PRF-19500 are as follows: Subgroups 4 and 5, see table III herein, step 1.
2/ The delta measurements for 4.4.2.2 (JAN, JANTX and JANTXV) for all steps; see table III herein, step 1.
3/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, see table III herein, step 1.
4/ The delta measurements for table E-IX of MIL-PRF-19500 and table III herein are as follows: Subgroups 1 and 2, see table III herein, step 1.

TABLE IV. Group E inspection (all quality levels) – for qualification or re-qualification only.

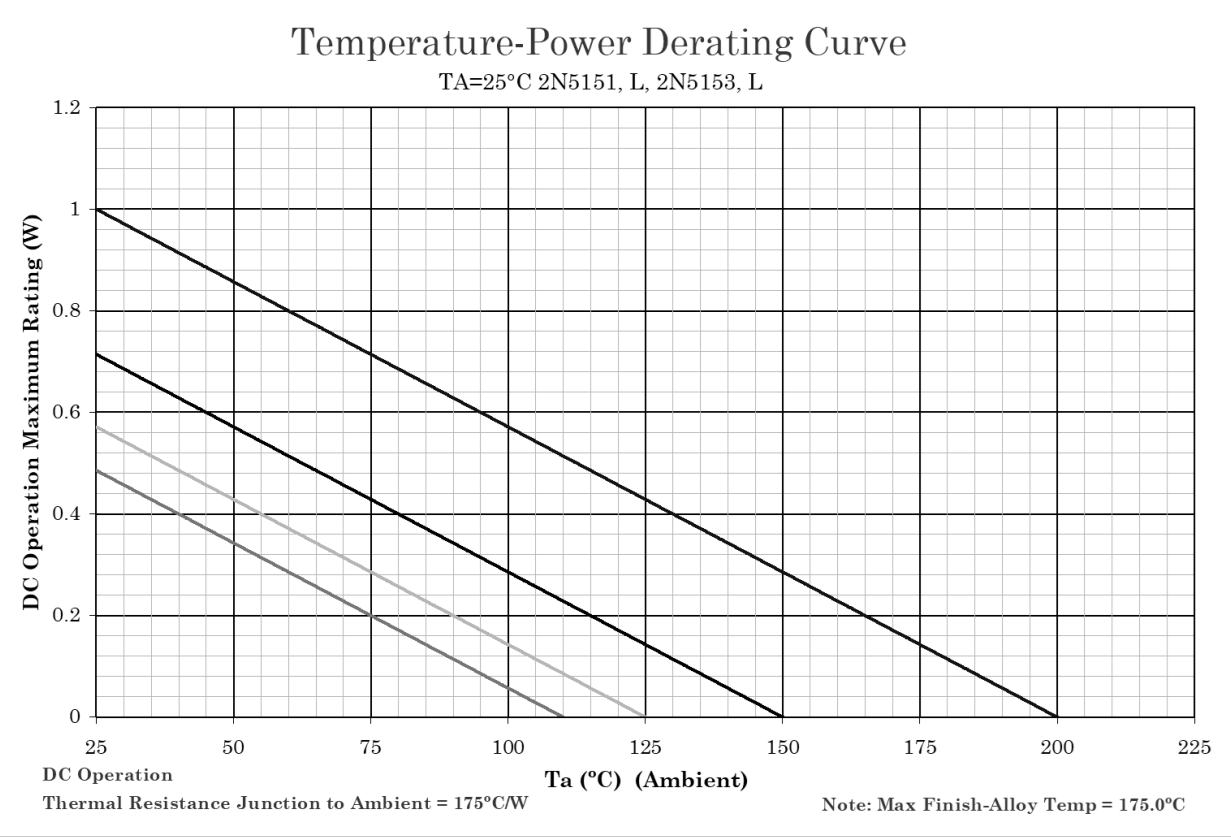
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 and table III herein	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = -10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C	
Electrical measurements		See table I, subgroup 2 and table III herein	
Subgroup 4			
Thermal impedance curves		See table E-IX of MIL-PRF-19500, group E, subgroup 4.	
Subgroup 5			
Not applicable			
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B	
Subgroup 12			
Neutron Irradiation	1017	See 4.5.3	



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

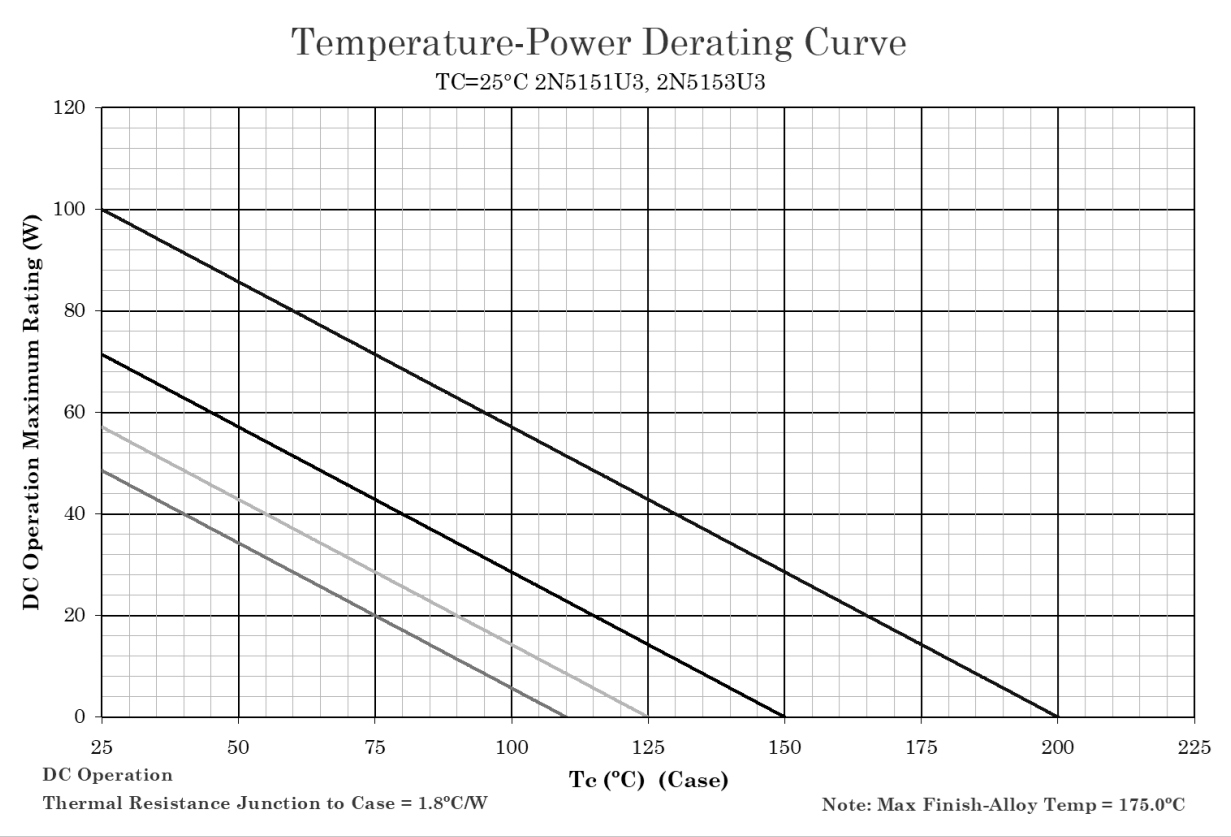
FIGURE 6. Temperature-power derating graph, TO-205, case temperature.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

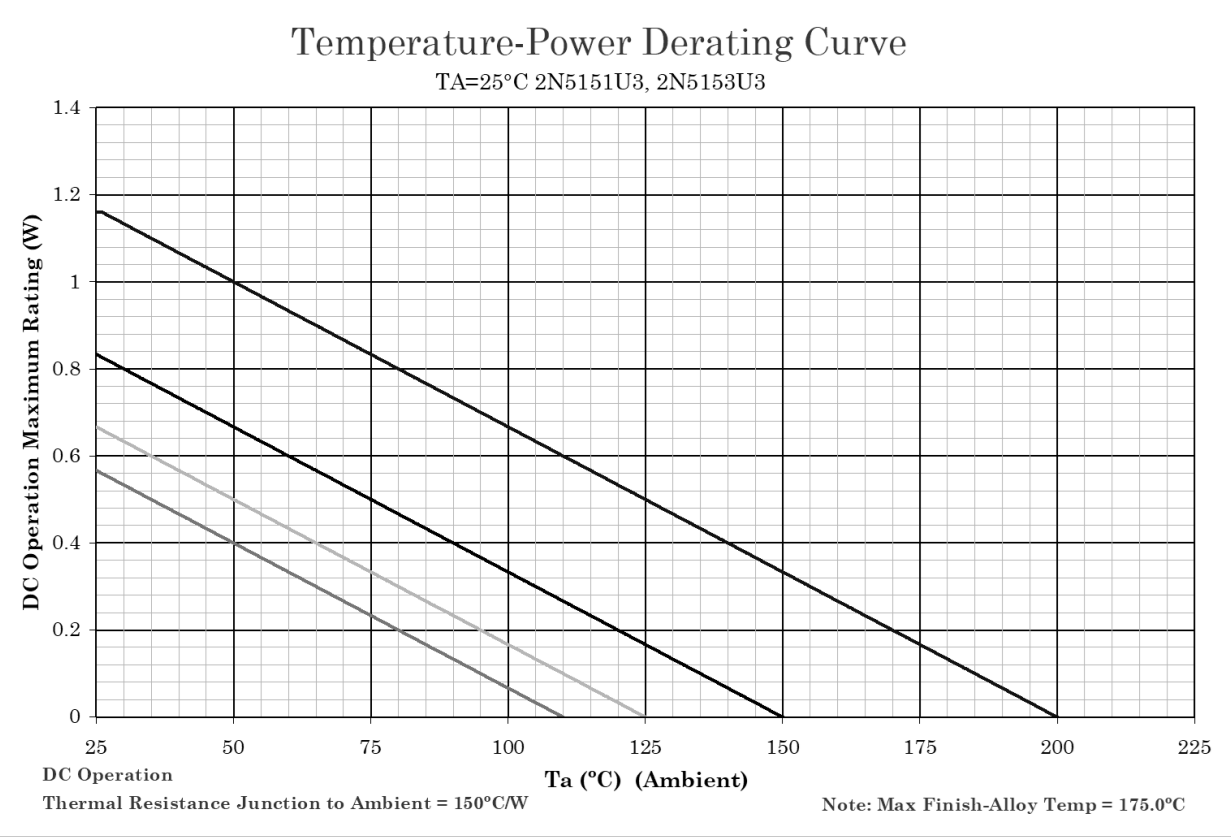
FIGURE 7. Temperature-power derating graphs, TO-205 ambient temperature.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

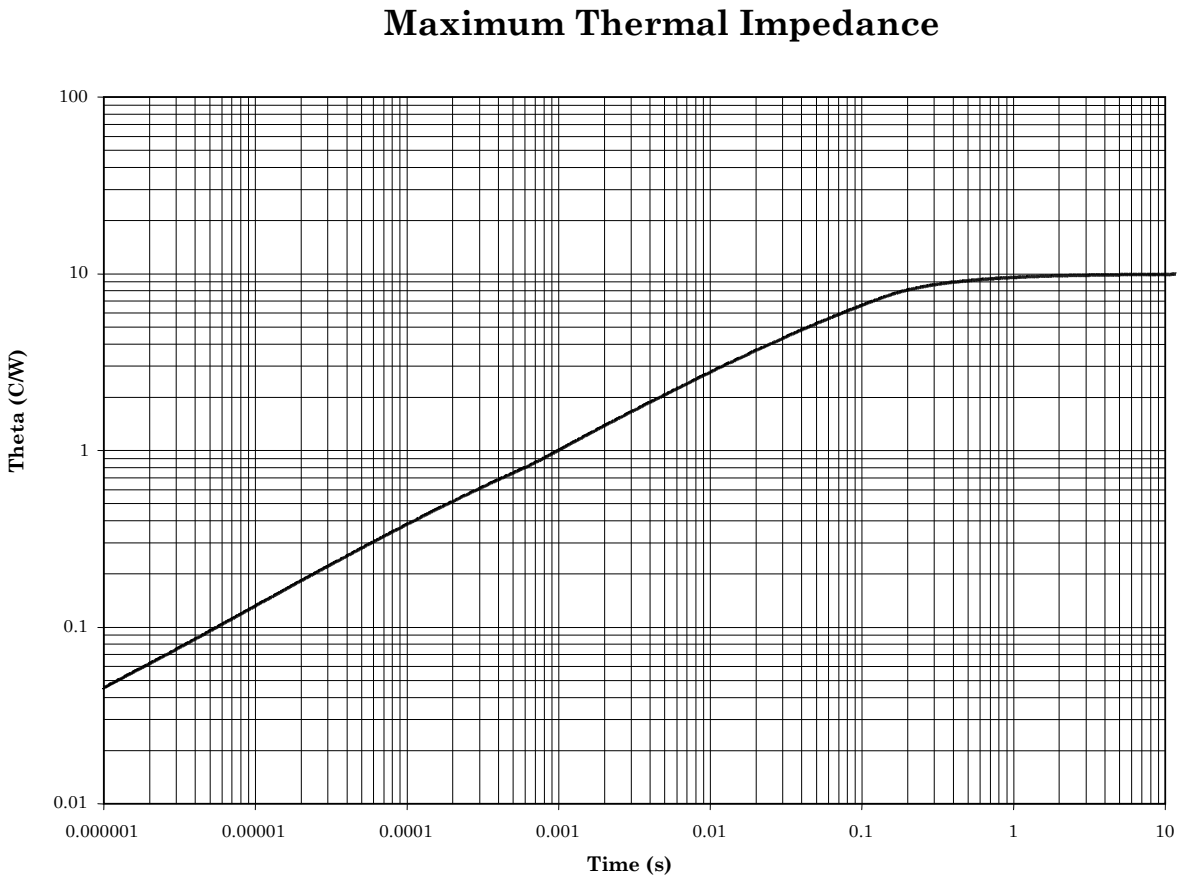
FIGURE 8. Temperature-power derating graph, U3 package, case temperature.



NOTES:

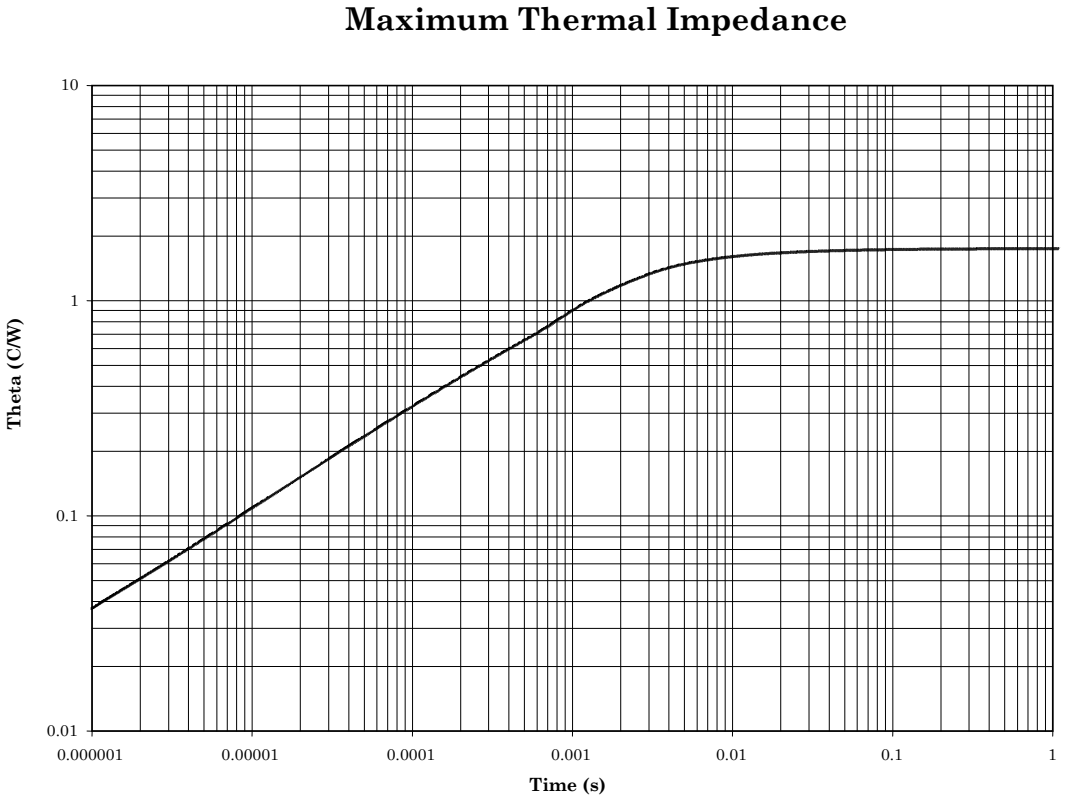
1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 9. Temperature-power derating graph, U3 package, ambient temperature.



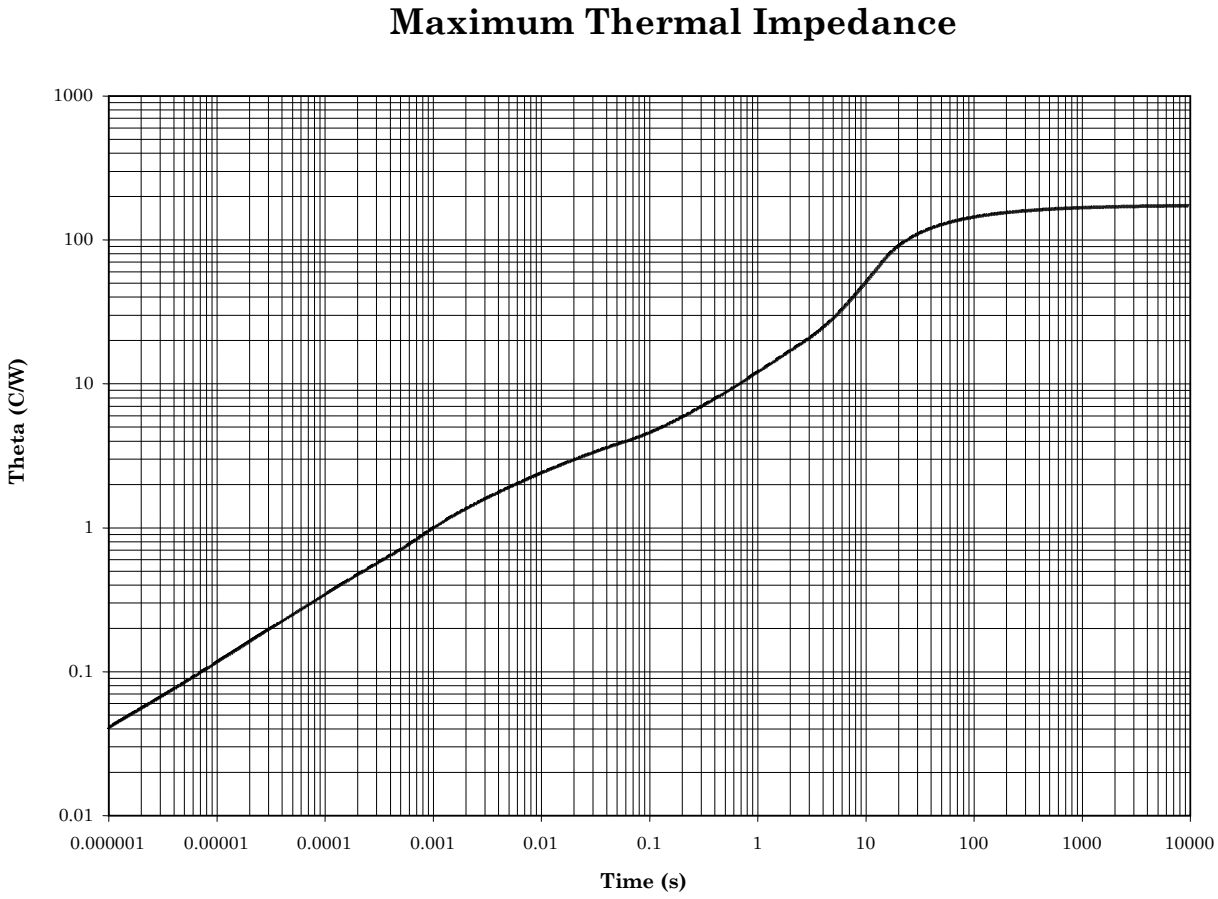
2N5151, 2N5151L, 2N5153, and 2N5153L at T_C = +25°C, $R_{\theta JC}$ = 10°C/W.

FIGURE 10. Thermal impedance graph, TO-205 package at case temperature.



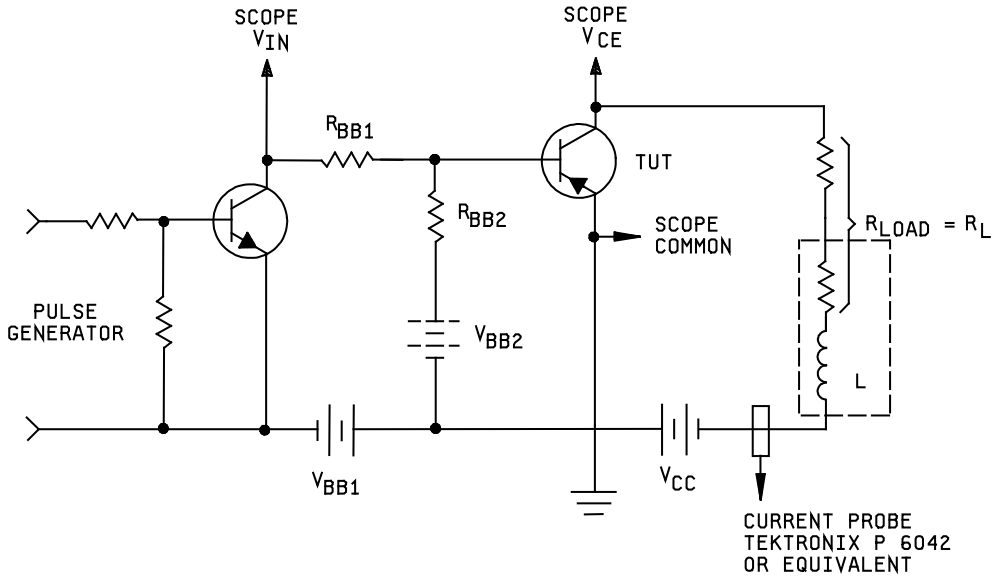
2N5151U3 and 2N5153U3 at T_C = +25°C, $R_{\theta JC}$ = 1.75°C/W.

FIGURE 11. Thermal impedance graph, U3 package at case temperature.



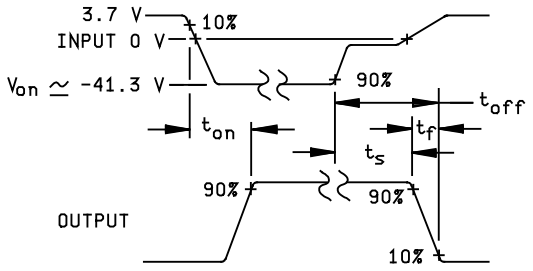
2N5151, 2N5151L, 2N5153, and 2N5153L at T_A = +25°C, $R_{\theta JA}$ = 175°C/W.

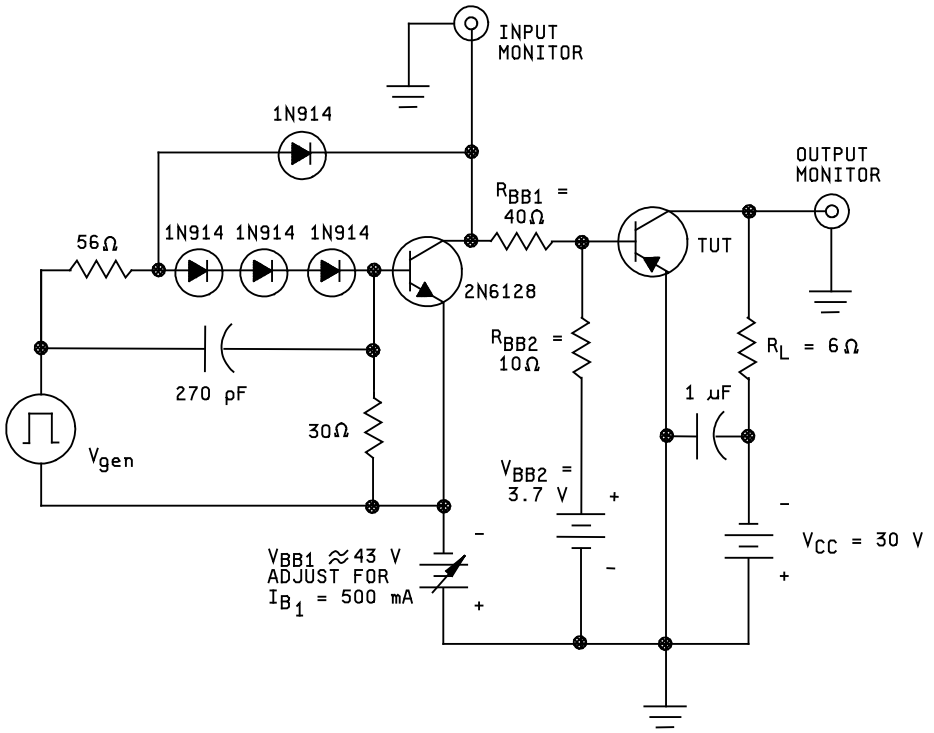
FIGURE 12. Thermal impedance graph, TO-205 package at ambient temperature.



R_{BB1} = 10 Ω
R_{BB2} = 100 Ω
L = 0.3 mH
R_L = 0.1 Ω
V_{CC} = -10 V dc
I_C = -10 A
V_{BB1} = -10 V dc
V_{BB2} = 4 V dc

FIGURE 13. Unclamped inductive load energy test circuit.





NOTES:

1. V_{gen} is -30 pulse (from 0 V) into a 50 ohm termination.
2. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f = 15$ ns, Z_{OUT} = 50 ohm, duty cycle ≤ 2 percent.
3. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{IN} \geq 10$ MΩ, $C_{IN} \leq 11.5$ pF.
4. Resistors shall be noninductive types.
5. The dc power supplies may require additional bypassing in order to minimize ringing.
6. An equivalent circuit may be used.

FIGURE 14. Switching time test circuit.

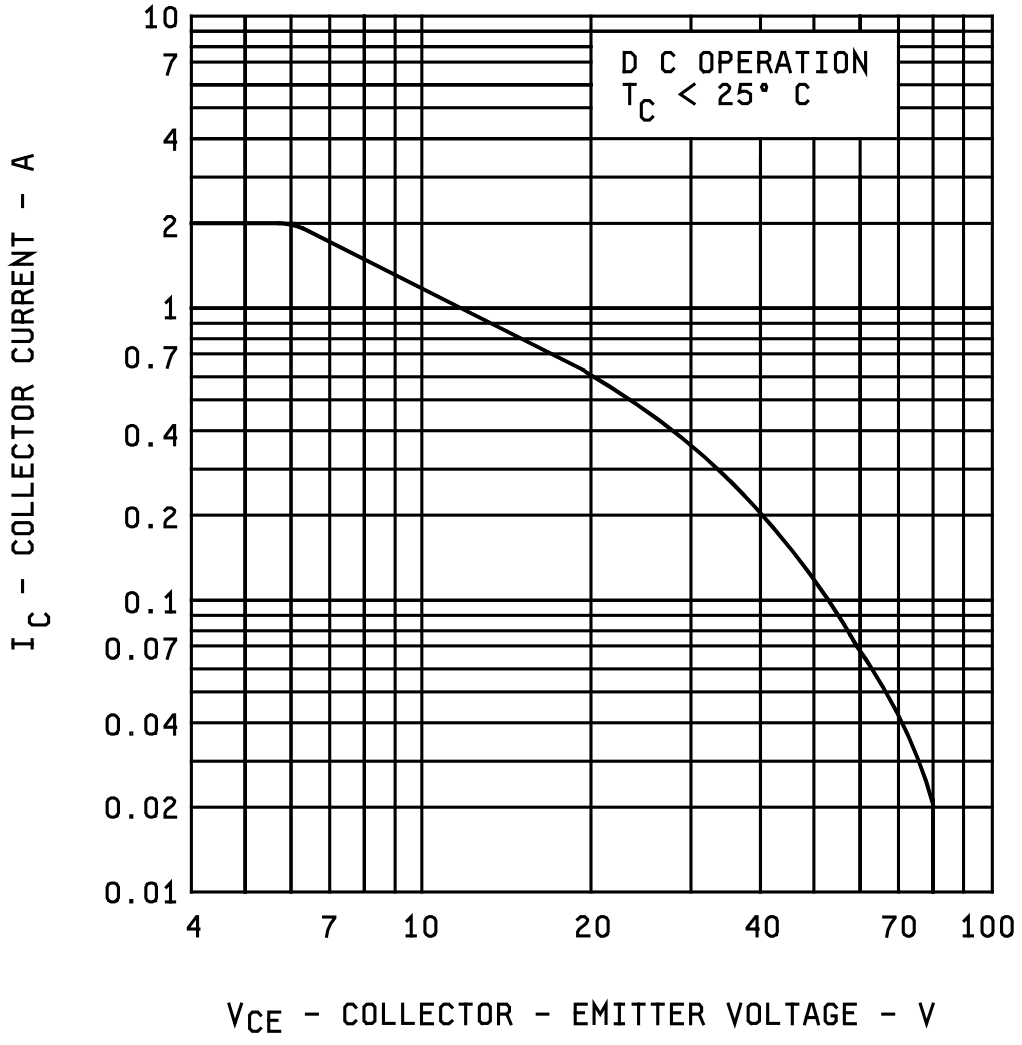


FIGURE 15. Maximum safe operating area.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.2).

d. The complete PIN, see 1.5 and 6.5.

e. For acquisition of RHA designed devices, table II herein, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it will be specified in the contract.

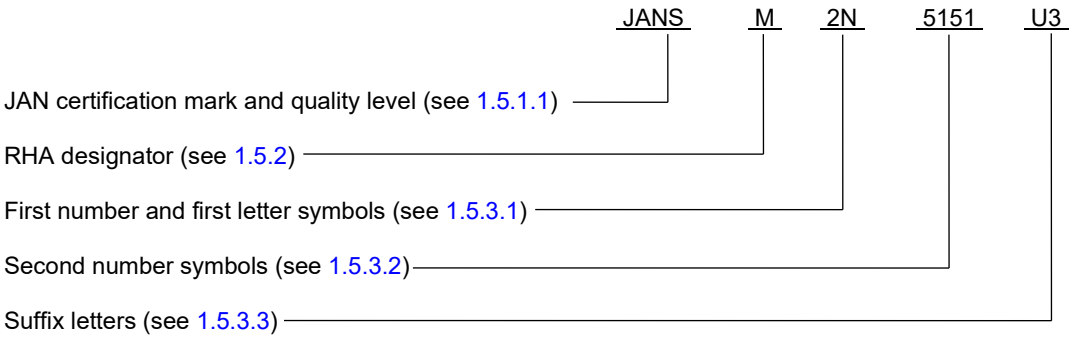
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4. Suppliers and PINs of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCB2N5151) will be identified on the QML.

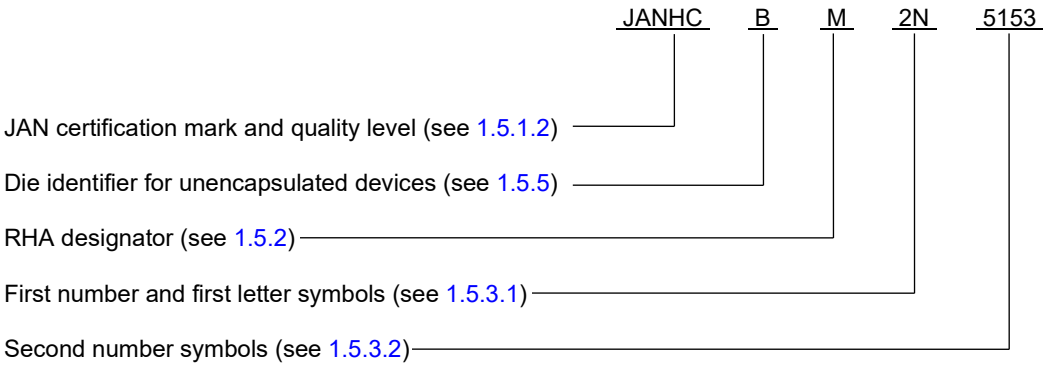
JANHC and JANKC ordering information			
PIN	Manufacturer		
	34156	43611	52GC4
2N5151 2N5153	JANHCB2N5151 JANHCB2N5153	JANHCC2N5151 JANHCC2N5153	JANHCD2N5151 JANHCD2N5153
2N5151 2N5153	JANKCB2N5151 JANKCB2N5153	JANKCC2N5151 JANKCC2N5153	JANKCD2N5151 JANKCD2N5153

6.5 PIN construction example.

6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.6 List of PINs.

6.6.1 PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for type 2N5151 and 2N5153.			
JAN2N5151	JANTX2N5151	JANTXV#2N5151	JANS#2N5151
JAN2N5151L	JANTX2N5151L	JANTXV#2N5151L	JANS#2N5151L
JAN2N5153	JANTX2N5153	JANTXV#2N5153	JANS#2N5153
JAN2N5153L	JANTX2N5153L	JANTXV#2N5153L	JANS#2N5153L
JAN2N5151U3	JANTX2N5151U3	JANTXV#2N5151U3	JANS#2N5151U3
JAN2N5153U3	JANTX2N5153U3	JANTXV#2N5153U3	JANS#2N5153U3

* (1) The number sign (#) represents one of eleven RHA designators available (E, K, U, M, D, P, L, R, F, G, or H). The PIN is also available without a RHA designator.

6.6.2 PINs for unencapsulated devices (die). The following is a list of possible PINs for unencapsulated devices available on this specification sheet.

Quality level HC	Quality level KC
JANHCB#2N5151	JANKCB#2N5151
JANHCB#2N5153	JANKCB#2N5153
JANHCC#2N5151	JANKCC#2N5151
JANHCC#2N5153	JANKCC#2N5153
JANHCD#2N5151	JANKCD#2N5151
JANHCD#2N5153	JANKCD#2N5153

* (1) The number sign (#) represents one of eleven RHA designators available (E, K, U, M, D, P, L, R, F, G, or H). The PIN is also available without a RHA designator.

6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - MI

Preparing activity:
DLA - CC

(Project 5961-2024-030)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.