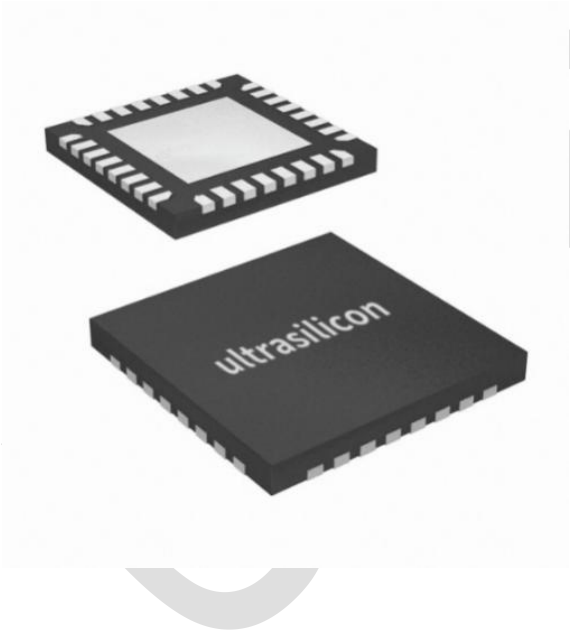
US5S310 1.8V, 2.5V, 3.3V LVCMOS Clock Buffer

Description

US5S310 is a widely used, low-jitter, low-power clock sector output buffer. It can allocate one of three inputs to ten low-jitter LVCMOS clock outputs. Its primary and secondary inputs can adopt differential or single-ended signals and crystal inputs. This buffer is suitable for various mobile and wired infrastructure, data communication, computing, low-power medical imaging and portable test and measurement applications. The core voltage of the device supports 2.5 V or 3.3 V, and the output voltage supports 1.5 V, 1.8 V, 2.5 V or 3.3 V. The overall additional jitter performance is 25 fs RMS (typical).



Features

- High-Performance 3:10 LVCMOS Clock Buffer
- Extremely low phase noise: -169dBc/Hz
- Transmission delay < 390 ps (Typical)
- Maximum operating frequency : 250MHz(VDDO=3.3V)
- Input supports LVPECL, LVDS, HCSL, SSTL or LVCMOS signal and crystal input
- Crystal input supports 10MHz-48MHz
- Differential and single terminal support 250MHz
- Supply voltage(VDD/VDDO):
  3.3V/3.3V, 2.5V,1.8V,1.5V
  2.5V/2.5V,1.8V,1.5V
- Industrial Temperature Range: -40°C to 85°C
- Available in 32-Pin QFN Package

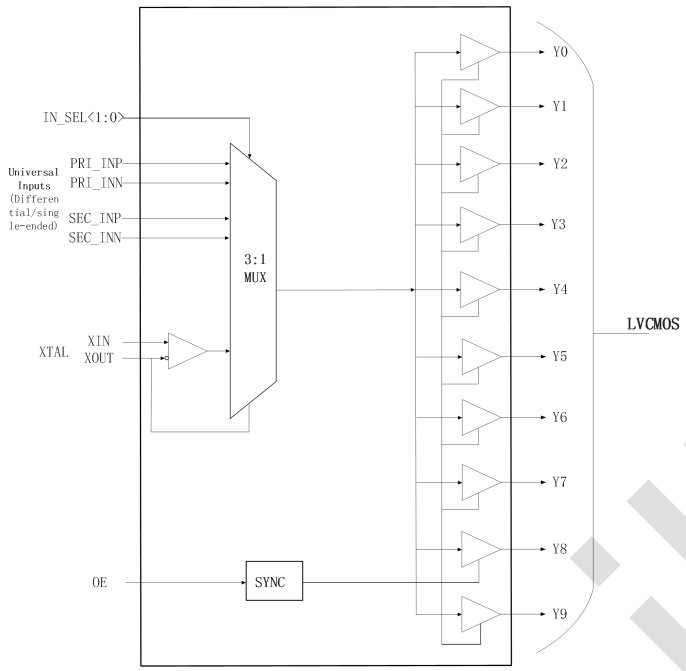
Applications

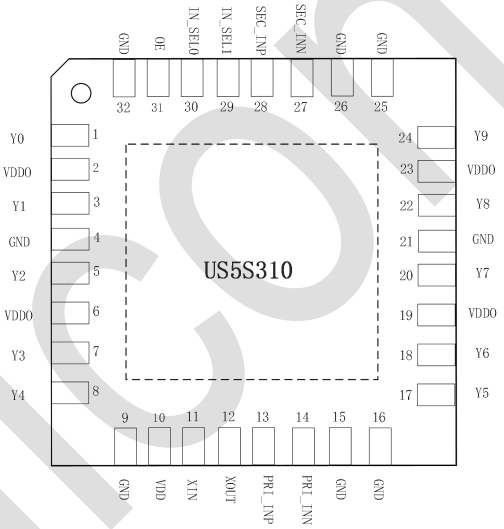
- General-Purpose Communication, Industrial, and Consumer Applications

Device Information

Part Number	Package	Body Size(NOM)
US5S310	QFN5*5-32	5.00mm x 5.00mm

Block Diagram





Pin Description and Function Table

管脚号	管脚名称	管脚类型	说明
1	Y0	Output	LVCMOS clock output 0
2	VDDO	Power	Output power supply, support 3.3V, 2.5V, 1.8V, 1.5V
3	Y1	Output	LVCMOS clock output 1
4	GND	Power	ground
5	Y2	Output	LVCMOS clock output 2
6	VDDO	Power	Output power supply, support 3.3V, 2.5V, 1.8V, 1.5V
7	Y3	Output	LVCMOS clock output 3
8	Y4	Output	LVCMOS clock output 4
9	GND	Power	ground
10	VDD	Power	Power supply, 3.3V or 2.5V
11	XTAL_I	Input	Crystal input
12	XTAL_O	Input	Crystal output
13	PRI_INP	Input	Main differential clock input positive end
14	PRI_INN	Input	Main differential clock input negative end
15	GND	Power	ground
16	GND	Power	ground
17	Y5	Output	LVCMOS clock output 5
18	Y6	Output	LVCMOS clock output 6
19	VDDO	Power	Output power supply, support 3.3V, 2.5V, 1.8V, 1.5V
20	Y7	Output	LVCMOS clock output 7
21	GND	Power	ground
22	Y8	Output	LVCMOS clock output 8
23	VDDO	Power	Output power supply, support 3.3V, 2.5V, 1.8V, 1.5V
24	Y9	Output	LVCMOS clock output 9
25	GND	Power	ground
26	GND	Power	ground
27	SEC_INN	Input	Subdifferential input negative end
28	SEC_INP	Input	Subdifferential input positive end
29	IN_SEL1	Input	Input clock select 1, internal 50K ohm pull-down
30	IN_SEL0	Input	Input clock select 0, internal 50K ohm pull-down
31	OE	Output	LVCMOS output control, internal 50K ohm pull-down
32	GND	Power	ground

Input logic

IN_sel1	IN_sel0	输入选择
0	0	PRI_IN
0	1	SEC_IN
1	0	XTAL
1	1	Hi Z

Input/Output Status Table

Input State	Output State
PRI_INx, SEC_INx open	Logic Low
PRI_INP, SEC_INP = HIGH, PRI_INN, SEC_INN = LOW	Logic High
PRI_INP, SEC_INP = LOW, PRI_INN, SEC_INN = HIGH	Logic Low

OE Control Table

OE	Yx
0	Hi Z
1	enable

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD} : Supply voltage	-0.5V to 4.6V
V_{IN} : Input voltage	-0.5V to V_{DD} + 0.5 V
V_{OUT} : Output voltage	
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

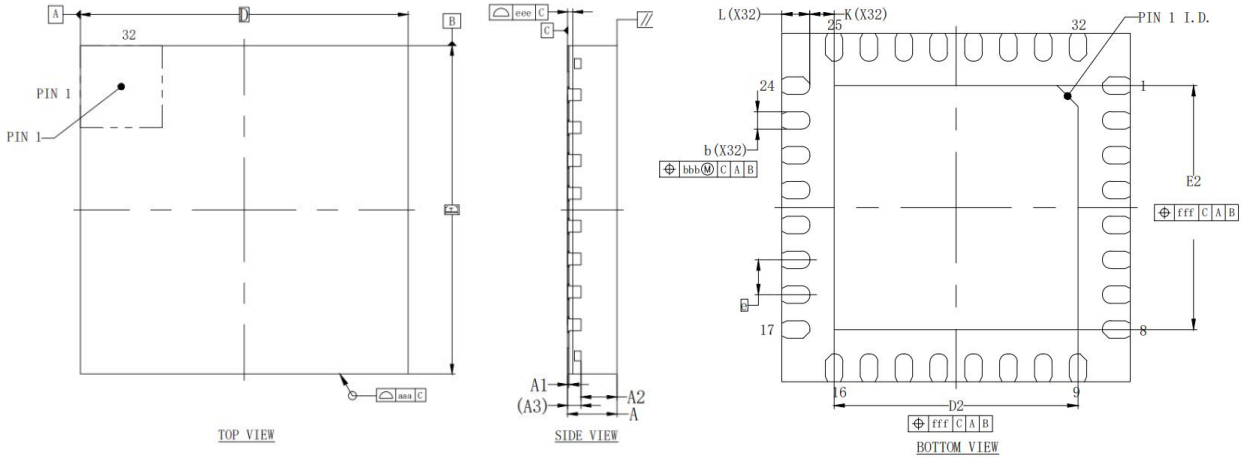
Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40	-	85	°C
T_J	Junction temperature		-	125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V
V_{DDO}	output voltage	3.3-5% 2.5-5% 1.8-5% 1.5-5%	3.3 2.5 1.8 1.5	3.3+5% 2.5+5% 1.8+5% 1.5+5%	V

Electrical Characteristics

VDD = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 85°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

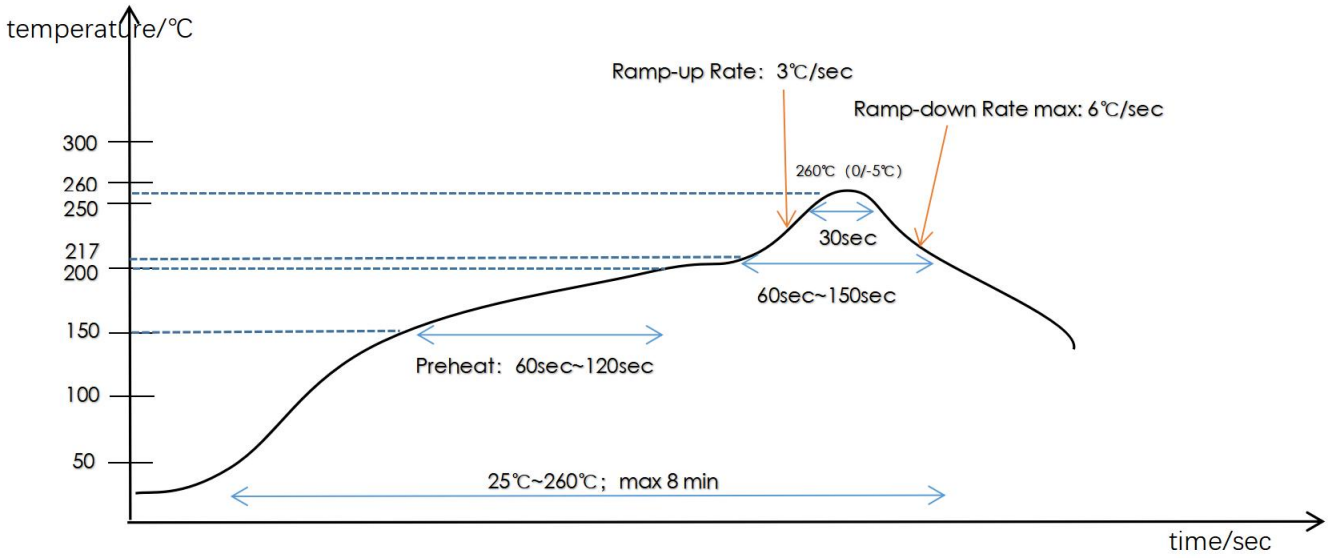
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input characteristics							
INPUT(OE, IN_SEL0, IN_SEL1, PRI_IN, SEC_IN)							
f_{CLKin}	Input frequency			0.1		250	MHz
V_{IHD}	Input high voltage	Differential input				VDD	V
V_{ILD}	Input low voltage			GND			V
V_{ID}	Differential input voltage swing			0.15		1.3	V
V_{CMD}	Differential input common mode voltage			0.5		VDD – 0.85	V
V_{IH}	Single-ended input high-level voltage	Single-ended input (DC or AC coupling)				VDD	V
V_{IL}	Single-end input low-level voltage			GND			V
V_{I_SE}	Single-end input voltage swing			0.3		2	V
V_{CM}	Single-ended input common mode voltage			0.25		VDD - 1.2	V
ISO_{MUX}	Input multiplexer isolation	f_{OFFSET} > 50 kHz, P_{CLKX} = 0 dBm	f_{CLK0} = 100MHz		-112.5		dBc
			f_{CLK0} = 200MHz		-82		
Crystal input（XTAL_I, XTAL_O）							
F_{CLK}	External clock frequency	XTAL_I :Single-ended input, XTAL_O:hanging		0.1		250	MHz
F_{XTAL}	Crystal frequency	The crystal is in fundamental mode		10		48	MHz
C_{IN}	On-chip load capacitance				4		pF
LVCMOS output characteristics							
f_{OUT}	Maximum output frequency			0.1		250	MHz
$Jitter_{ADD}$	Additional jitter (1MHz-20MHz)	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns			48.6		fs
noice	f_{OFFSET} ≥ 10 MHz	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns			-162.5		dBc/Hz
Duty Cycle	Duty Cycle			45%		55%	
V_{OH}	High voltage output	I_{OH} = -1 mA		2.8			V
V_{OL}	Low voltage output	I_{OH} = 1 mA				0.2	V
t_R	Output rise time （20% TO 80% ）	R_T = 160 Ω, R_L = 100 Ω, C_L ≤ 5 pF			0.33	0.8	ns
t_F	Output drop time （80% TO 20%）				0.33	0.8	ns
Transmission delay and output skew							
t_{PD}	Propagation delay				1.5	2.5	ns
$t_{SK(O)}$	output skew					50	ps
$t_{PART-SKEW}$	Part-to-part skew					400	ps

PACKAGE DIMENSIONS



symbol	Unit:mm		
	min	typ	max
D		5.0 BSC	
E		5.0 BSC	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2		0.55	
A3		0.203 REF	
b	0.20	0.25	0.30
L	0.30	0.40	0.50
e		0.50 BSC	
K		0.35 REF	
aaa		0.10	
bbb		0.10	
ccc		0.10	
eee		0.08	
fff		0.10	

Reflow profile



Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.05.05	First Draft.	1.0
2023.02.10	Operating frequency range change。	1.5
2023.03.28	Change chip program application information.	2.0