Description

The US5D1204D is a 2-GHz,4-output differential high-performance clock fanout buffer.

The US5D1204D clock buffer distributes one of two selectable clock inputs (IN0 and IN1) to 4 pairs of differential LVDS clock outputs (Q0 through Q3) with minimum skew for clock distribution. The US5D1204D can accept two clock sources into an input multiplexer. The inputs can either be LVDS,LVPECL, or LVCMOS. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 2.5V and 3.3V core power supply, and either a 2.5V and 3.3V output operating supply.

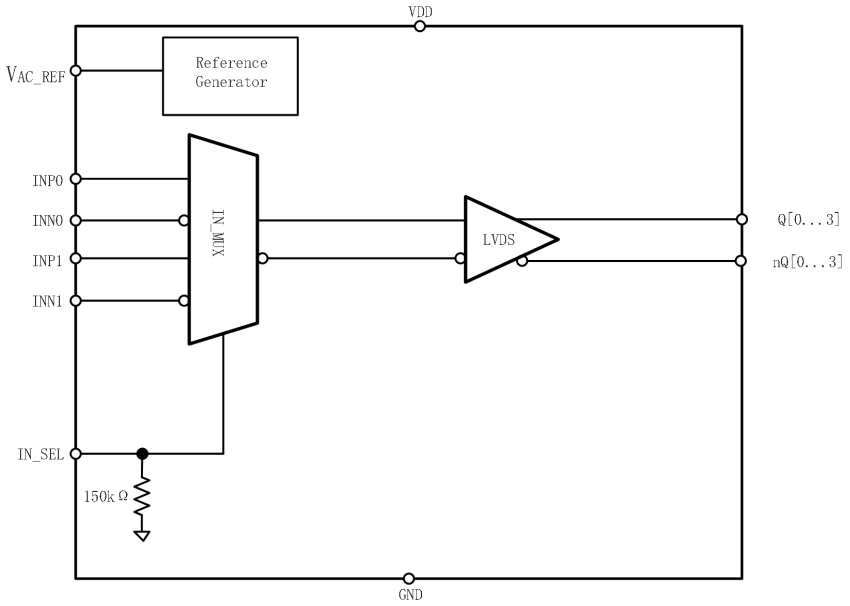
Features

- 2:4 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS，HCSL and LVCMOS
- Four LVDS output
- Maximum Output Frequency - LVDS 2-GHz
- Maximum Propagation Delay: 0.5 ns(typical)
- Output skew: 50 ps (Maximum)
- Part-to-part skew: 300ps(Maximum)
- Additive RMS phase jitter @ 156.25MHz: ＜100 fs RMS (10kHz - 20MHz)
- Supply voltage mode VDD: 2.375V to 3.465V
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-16 package

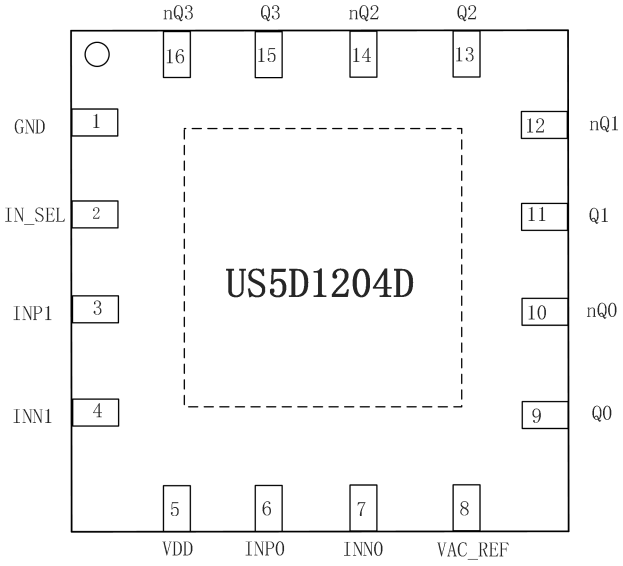
Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

Block Diagram



Pin Assignment for QFN-16 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	GND	Power	Ground.
2	IN_SEL	Input	Input selection with an internal 150-kΩ pulldown; selects input port
3	INP1	Input	differential input or single-ended input.
4	INN1	Input	differential clock input.
5	VDD	Power	Power supply for Core.
6	INP0	Input	Redundant differential input or single-ended input.
7	INN0	Input	Inverting differential clock.
8	VAC_REF	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1-μF to GND on this pin.
9	Q0	Output	Differential LVDS clock output pair.
10	nQ0	Output	Differential LVDS clock output pair.
11	Q1	Output	Differential LVDS clock output pair.
12	nQ1	Output	Differential LVDS clock output pair.
13	Q2	Output	Differential LVDS clock output pair.
14	nQ2	Output	Differential LVDS clock output pair.
15	Q3	Output	Differential LVDS clock output pair.
16	nQ3	Output	Differential LVDS clock output pair.

Table 2: Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	INP0,INN0
1	INP1,INN1

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	2.5-5% 3.3-5%	2.5 3.3	2.5+5% 3.3+5%	V

Electrical Characteristics

VDD = 2.375 V to 2.625 V and TA = –40°C to 85°C (unless otherwise noted).

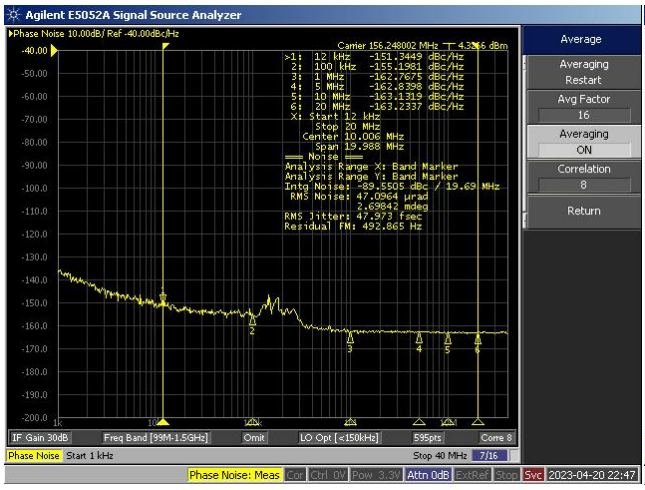
Parameter		Test Conditions	Min	Typ	Max	Unit
IN_SEL CONTROL						
VIH	Input high voltage		0.7*VDD			V
VIL	Input low voltage				0.3*VDD	V
IIH	Input high current	VDD =2.625V, VIH = 2.625 V			30	μA
IIL	Input low current	VDD = 2.625 V, VIL = 0 V			-30	μA
R_{pull}(IN_SEL)	Input pulldown resistor			150		kΩ
LVCMOS INPUT						
FIN	Input frequency		0.1		250	MHz
Vth	input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
VIH	Input high voltage		1.2		VDD	V
VIL	Input low voltage		0		1.4	V
IIH	Input high current	VDD = 2.625V, VIH = 2.625 V			10	μA
IIL	Input low current	VDD = 2.625V, VIL = 0 V			-10	μA
ΔV/ΔT	Slew rate	20% to 80%	1.5			V/ns
DIFFERENTIAL INPUT						
FIN	Input frequency		0.1		2000	MHz
V IN,DIFF	Differential input voltage Peak-to-peak	VICM=1.25V	0.3		1.6	VPP
V ICM	Input common mode voltage	VIN, DIFF, PP > 0.4 V	1		VDD-0.3	V
IIH	Input high current	VDD = 2.625V, VIH = 2.625 V			10	μA
IIL	Input low current	VDD = 2.625V, VIL = 0 V			-10	μA
ΔV/ΔT	Slew rate	20% to 80%	0.75			V/ns
C_{IN}	Input capacitance			2.5		pF

Electrical Characteristics(continued)

VDD =3.135 V to 3.6 V and TA = –40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
LVDS OUTPUT						
VOD	Differential output voltage magnitude	VIN, DIFF,RL = 100 Ω	250		450	mV
ΔVOD	Change in differential output voltage magnitude	VIN, DIFF,RL = 100 Ω	-15		15	mV
VOC(ss)	Steady-state common mode output voltage	VIN, DIFF,RL = 100 Ω	1.1		1.375	V
ΔVOC(ss)	Steady-state common mode output voltage	VIN, DIFF,RL = 100 Ω	-15		15	mV
Vring	Output overshoot and undershoot	Percentage of output amplitude VOD			10%	
VOS	Output AC common mode	VIN, DIFF, PP = 0.6 V, RL = 100 Ω		25	70	mVPP
IOS	Short-circuit output current	VOD = 0 V			±24	mA
t_{PD}	Propagation delay	VIN, DIFF, PP = 0.3 V		0.5	1.5	ns
$t_{SK,pp}$	Part-to-part skew				300	ps
$t_{SK,O}$	Output skew			10	50	ps
$t_{SK,P}$	Pulse skew	50% duty cycle input,crossingpoint-to-crossing-point distortion	-50		50	ps,RMS
t_{RJIT}	Random additive jitter	50% duty cycle input, edge speed = 0.75 V/ns, 10 kHz to 20 MHz		62	100	fs
t_R/t_F	Output rise and fall time	20% to 80%	50	150	300	ps

Phase Noise Plot



Low jitter SPXO(156.25MHz)(48fs) Output Phase Noise(78fs)

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

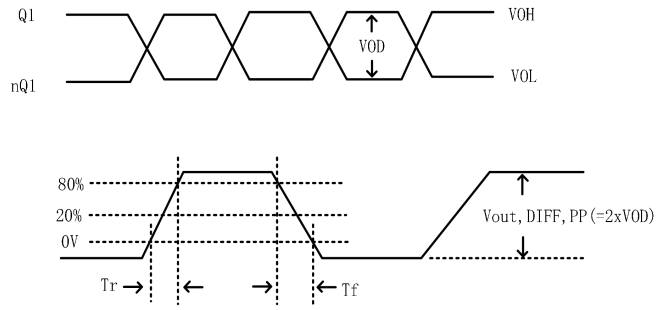
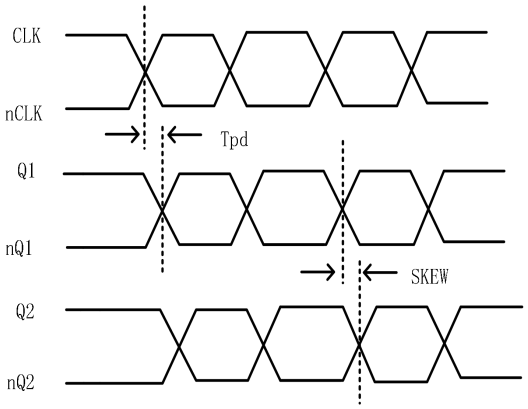


Figure 1.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 2.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

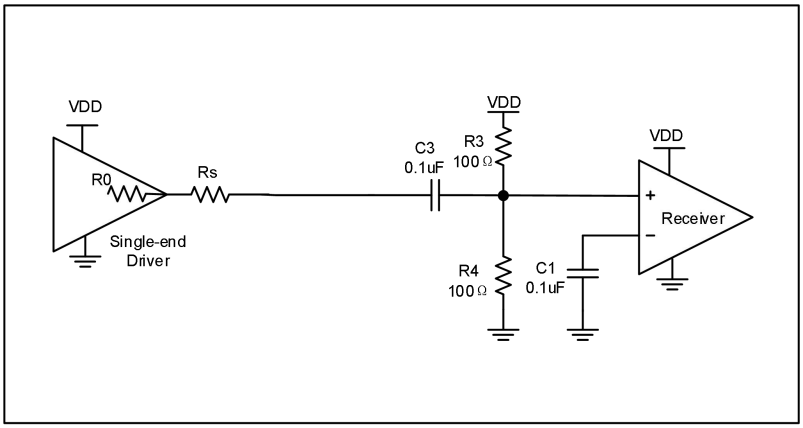
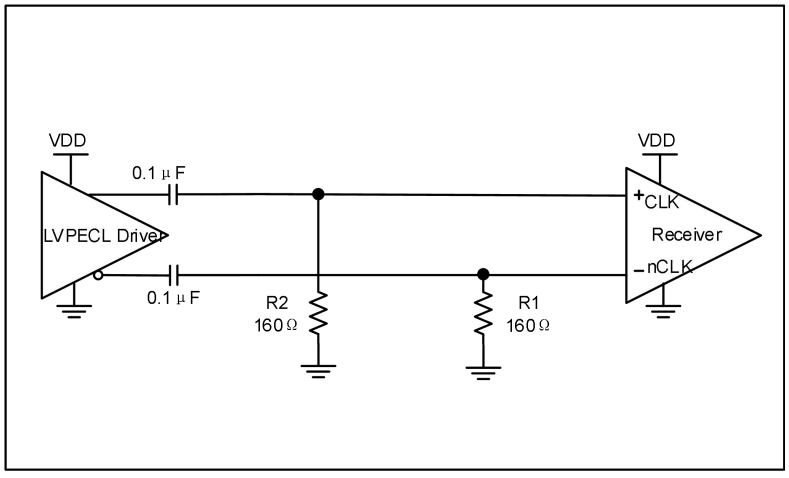
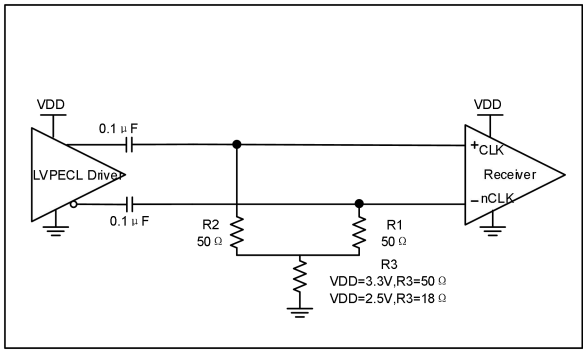


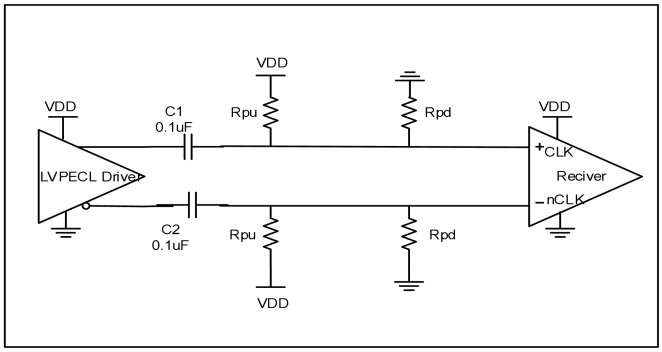
Figure3.Single-termination method of differential input

Input connection circuit

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure4 to Figure7 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

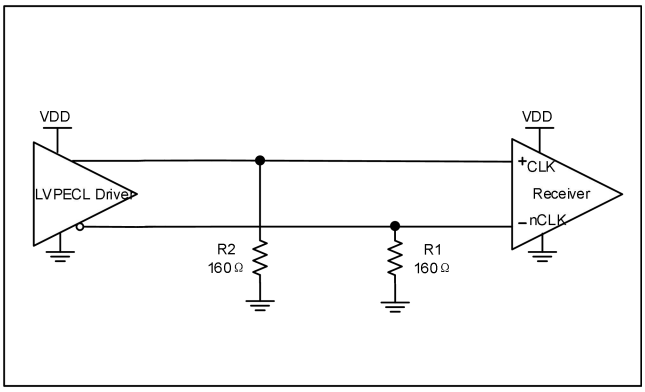


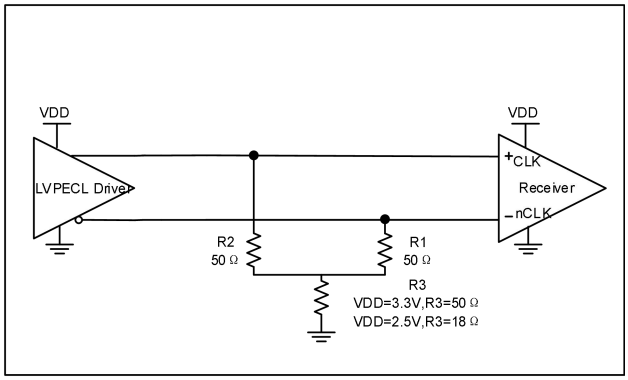


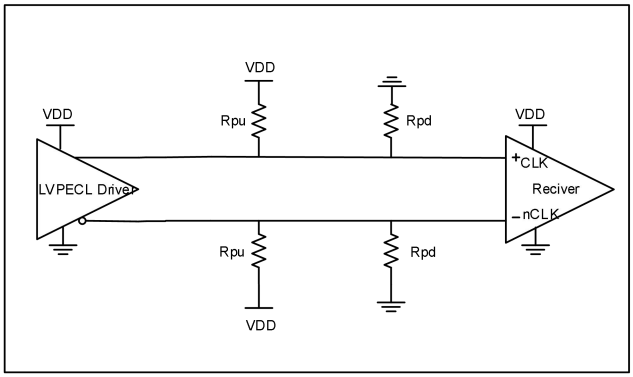


VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure4.LVPECL Driver(AC)

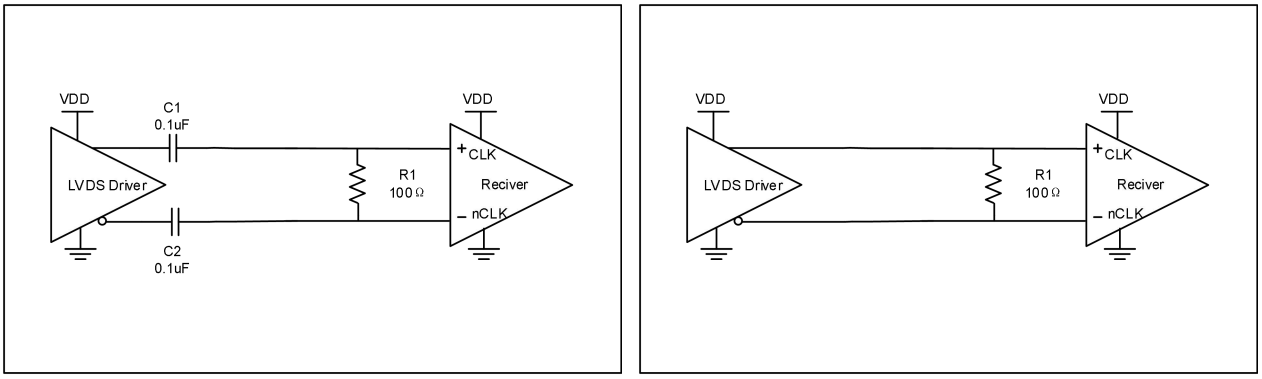






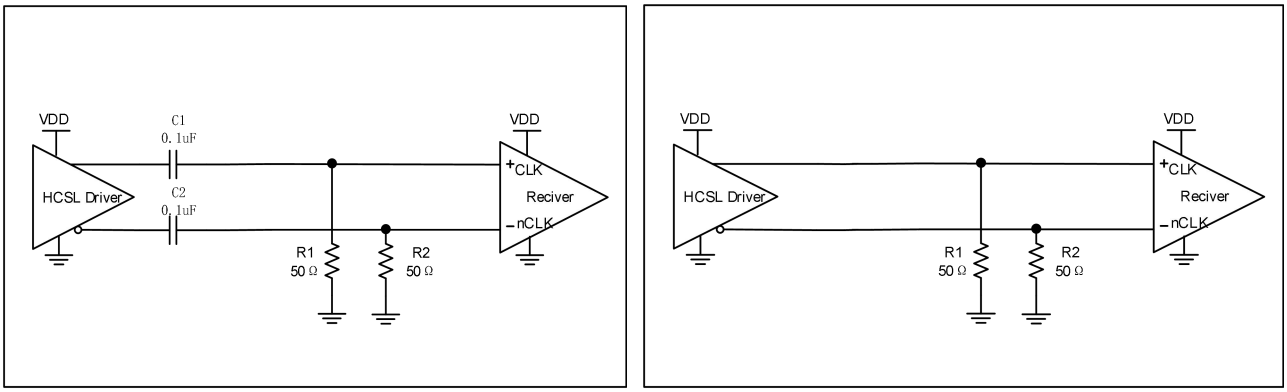
VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure5.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

Figure6.LVDS Driver



a)AC coupling **b)DC coupling**

Figure7.HCSL Driver

Output connection circuit

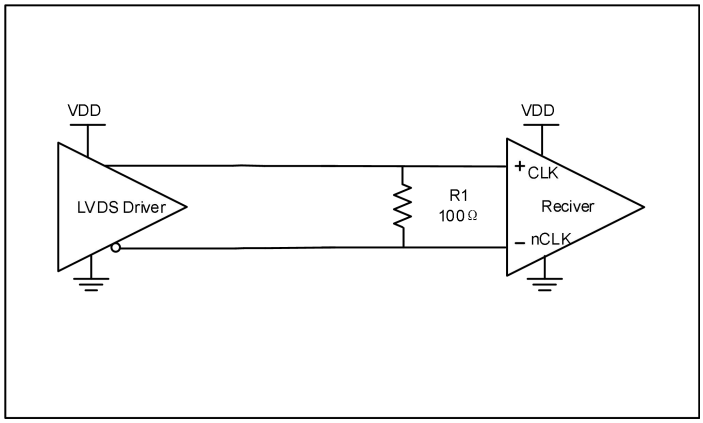
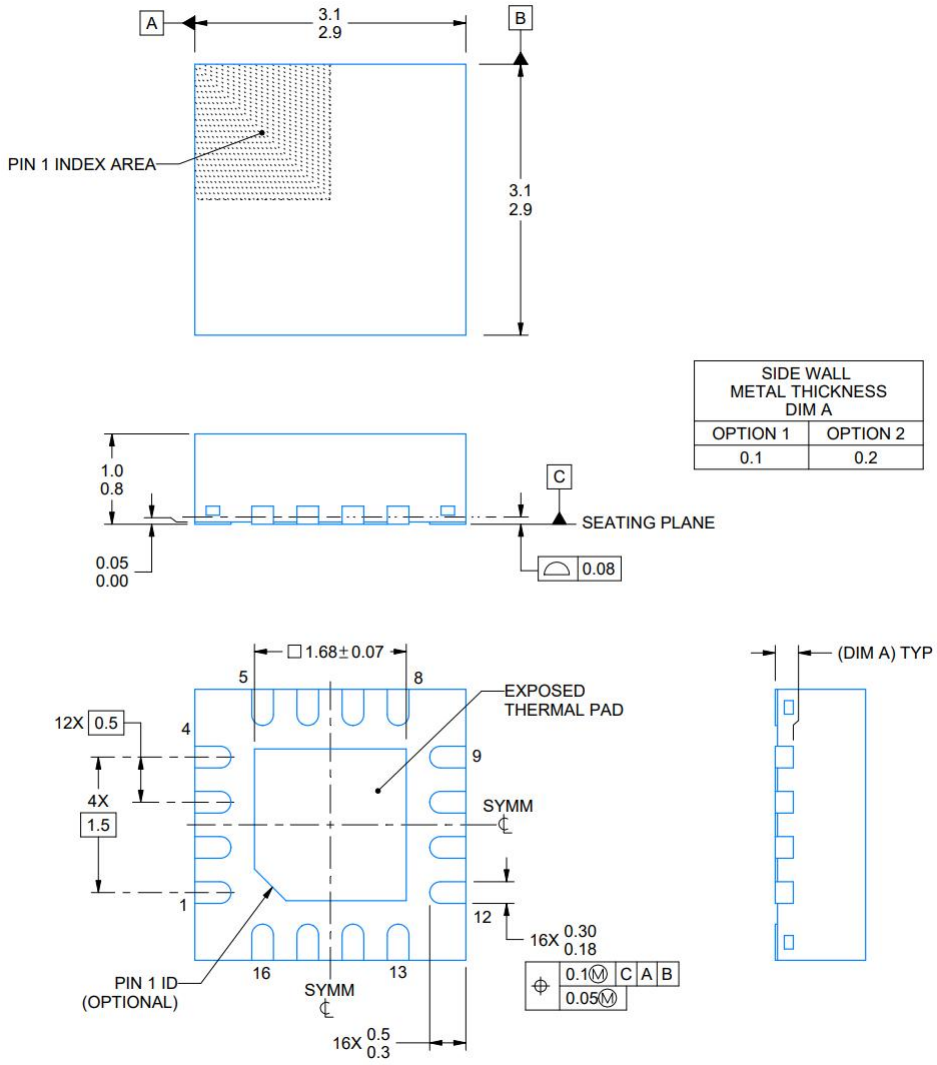


Figure8.LVDS Driver

PACKAGE DIMENSIONS(QFN-16)



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.80	0.90	1.00	K	0.20	-	-
A1	0.00	0.02	0.05	L	0.20	0.30	0.40
A3	-	0.20Ref	-	aaa	0.05		
b	0.20	0.25	0.30	bbb	0.10		
D	3.00BSC			ccc	0.10		
E	3.00BSC			ddd	0.05		
e	0.50BSC			eee	0.08		
D2	1.60	1.70	1.80				
E2	1.60	1.70	1.80				

Reflow profile

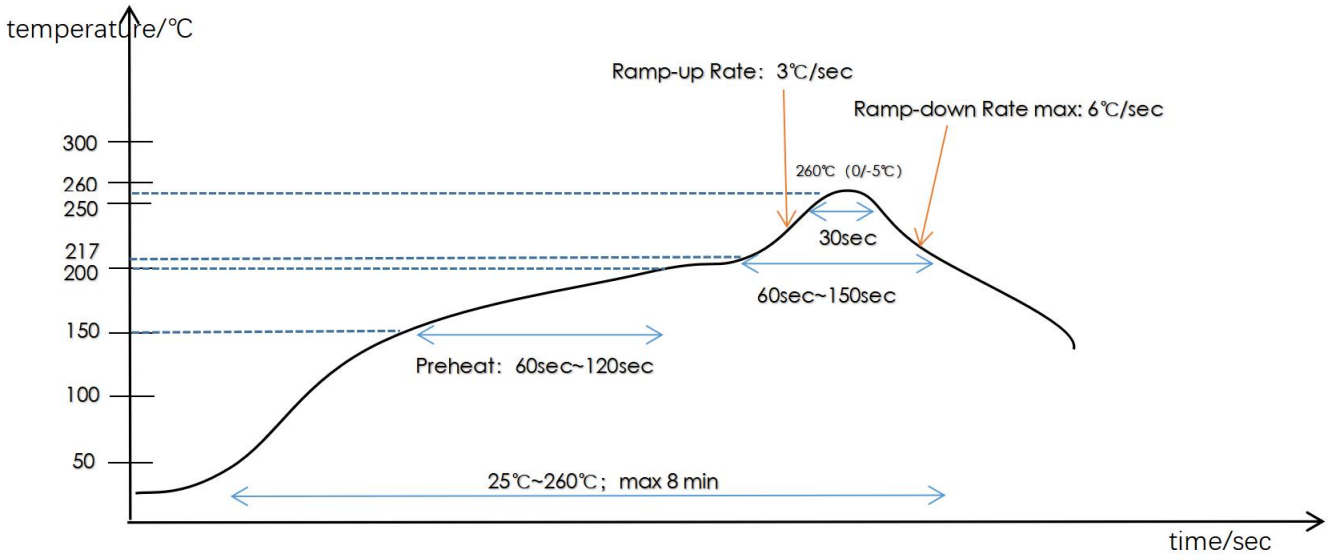


Figure9: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.12.26	First Draft.	1.0
2023.4.3	Update electrical performance parameters and Matching circuit diagram.	1.5
2023.5.11	Update Timing Diagrams and input selecton.	2.0
2023.8.8	Update the pin definition.	2.5