

## KIA12N60H-VB Datasheet

### N-Channel 650V (D-S) Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V) at $T_J$ max.		650
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.65
$Q_g$ max. (nC)		43
$Q_{gs}$ (nC)		5
$Q_{gd}$ (nC)		22
Configuration		Single

### FEATURES

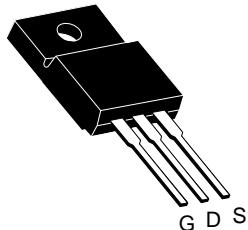
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)



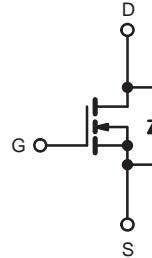
### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial

TO-220 FULLPAK



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	650	V	
		$V_{GS}$	$\pm 30$		
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$I_D$	12	A	
			9.4		
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	45		
Linear Derating Factor			3.6	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	290	mJ	
Maximum Power Dissipation		$P_D$	106 / 34	W	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	°C	
Drain-Source Voltage Slope	$T_J = 125$ °C	$dV/dt$	15	V/ns	
Reverse Diode $dV/dt$ <sup>d</sup>			4.1		
Soldering Recommendations (Peak Temperature) <sup>c</sup>			300	°C	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$  Ω,  $I_{AS} = 4.5$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/μs, starting  $T_J = 25$  °C.

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYP.	MAX.	UNIT			
Maximum Junction-to-Ambient	$R_{thJA}$	-	60	$^{\circ}\text{C}/\text{W}$			
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.8				
SPECIFICATIONS ( $T_J = 25^{\circ}\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		650	-	-	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^{\circ}\text{C}$ , $I_D = 1 \text{ mA}$		-	0.75	-	
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		3	-	5	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$ nA	
		$V_{GS} = \pm 30 \text{ V}$		-	-	$\pm 1$ $\mu\text{A}$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	1	
		$V_{DS} = 520 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^{\circ}\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 8 \text{ A}$	-	0.65	-	
Forward Transconductance	$g_{fs}$	$V_{DS} = 30 \text{ V}$ , $I_D = 8 \text{ A}$		-	16	-	
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$		-	1600	-	
Output Capacitance	$C_{oss}$			-	300	-	
Reverse Transfer Capacitance	$C_{rss}$			-	200	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to $520 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	63	-	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	213	-	
Total Gate Charge	$Q_g$			-	43	96	
Gate-Source Charge	$Q_{gs}$	$V_{GS} = 10 \text{ V}$	$I_D = 8 \text{ A}$ , $V_{DS} = 520 \text{ V}$	-	5	-	
Gate-Drain Charge	$Q_{gd}$			-	22	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520 \text{ V}$ , $I_D = 8 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_g = 9.1 \Omega$		-	13	25	
Rise Time	$t_r$			-	11	35	
Turn-Off Delay Time	$t_{d(off)}$			-	81	90	
Fall Time	$t_f$			-	25	40	
Gate Input Resistance	$R_g$	$f = 1 \text{ MHz}$ , open drain		-	3.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	15	
Pulsed Diode Forward Current	$I_{SM}$			-	-	40	
Diode Forward Voltage	$V_{SD}$	$T_J = 25^{\circ}\text{C}$ , $I_S = 8 \text{ A}$ , $V_{GS} = 0 \text{ V}$		-	-	1.5	
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}$ , $I_F = I_S = 8 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$ , $V_R = 400 \text{ V}$		-	345	-	
Reverse Recovery Charge	$Q_{rr}$			-	4.5	-	
Reverse Recovery Current	$I_{RRM}$			-	35	-	

**Notes**

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

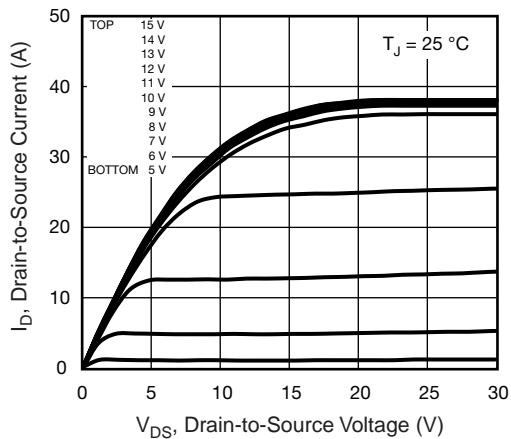
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


Fig. 1 - Typical Output Characteristics

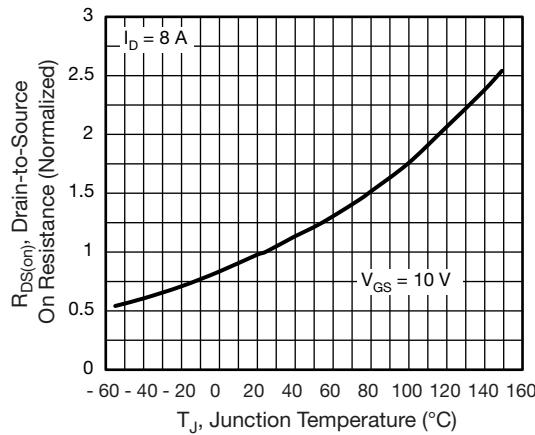


Fig. 4 - Normalized On-Resistance vs. Temperature

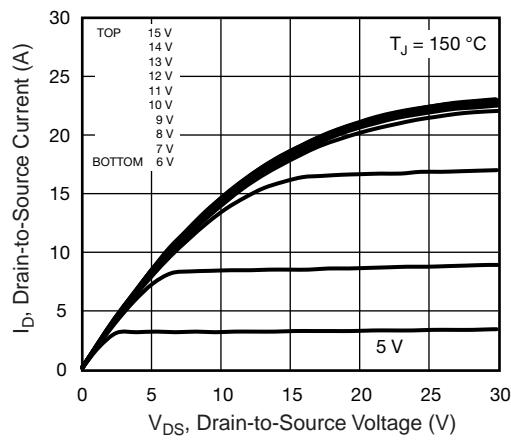


Fig. 2 - Typical Output Characteristics

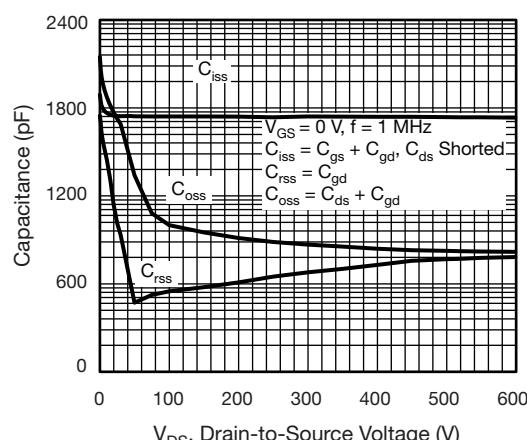


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

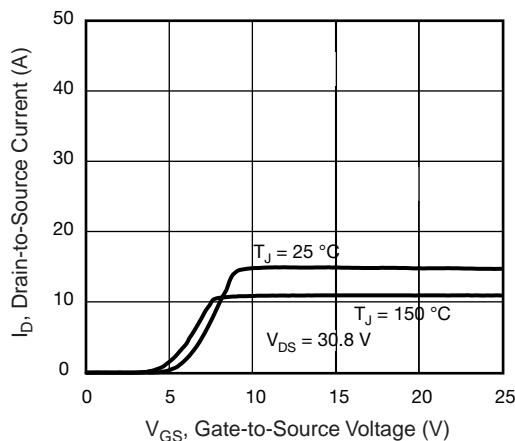


Fig. 3 - Typical Transfer Characteristics

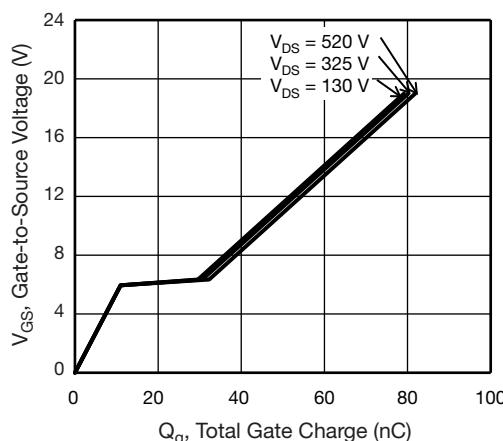


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

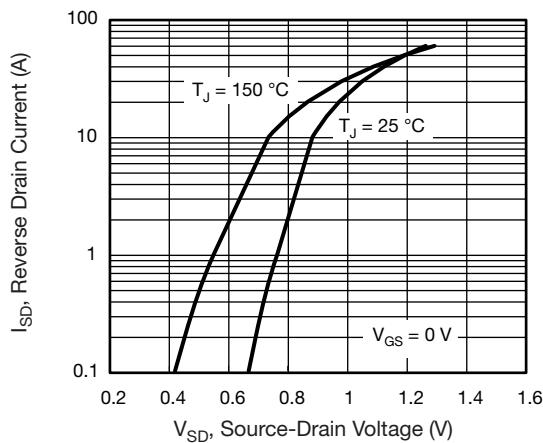


Fig. 7 - Typical Source-Drain Diode Forward Voltage

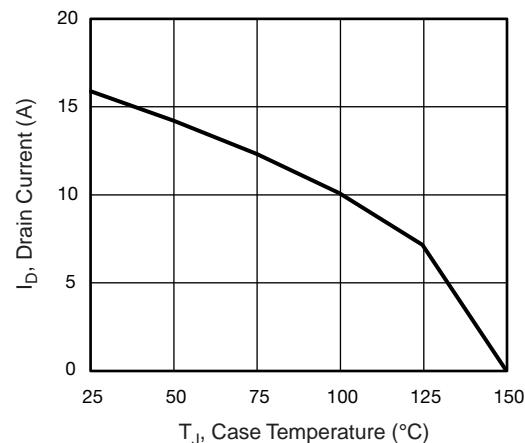


Fig. 9 - Maximum Drain Current vs. Case Temperature

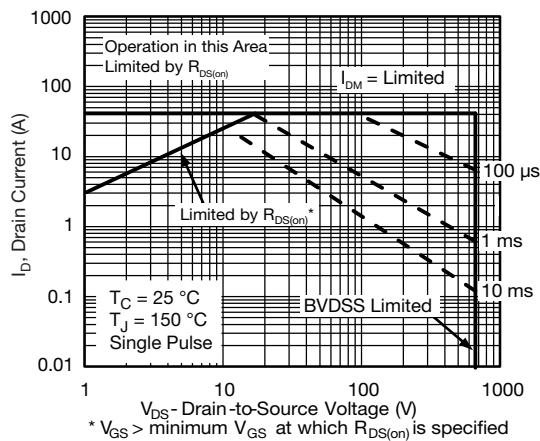


Fig. 8 - Maximum Safe Operating Area

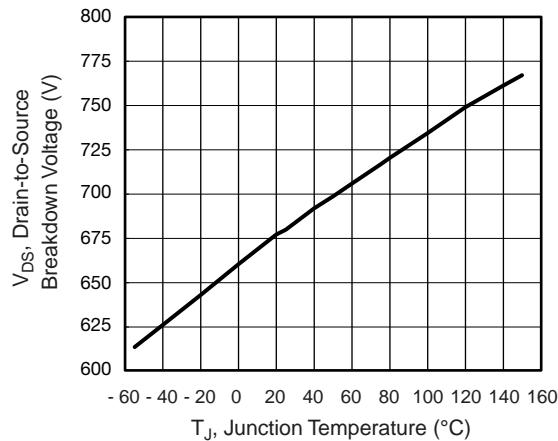


Fig. 10 - Temperature vs. Drain-to-Source Voltage

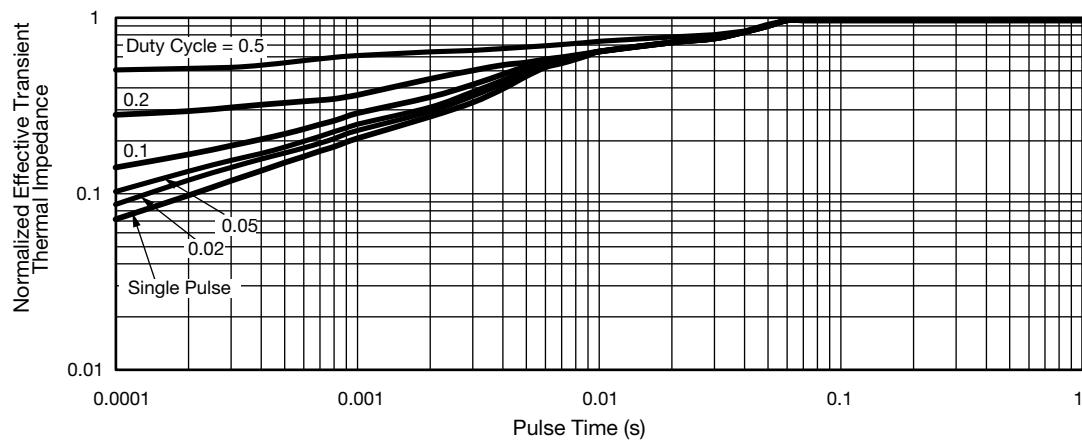


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

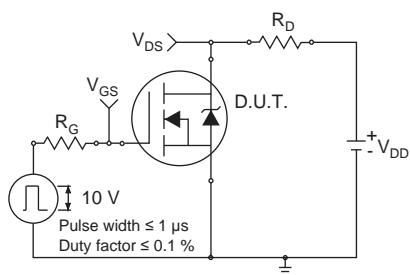


Fig. 12 - Switching Time Test Circuit

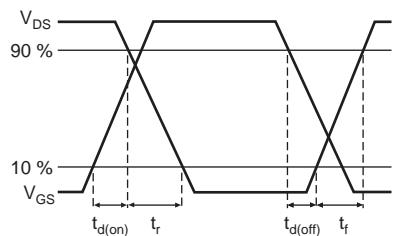


Fig. 13 - Switching Time Waveforms

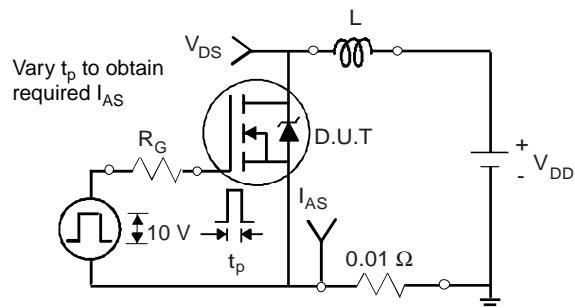


Fig. 14 - Unclamped Inductive Test Circuit

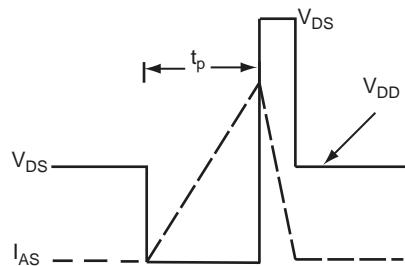


Fig. 15 - Unclamped Inductive Waveforms

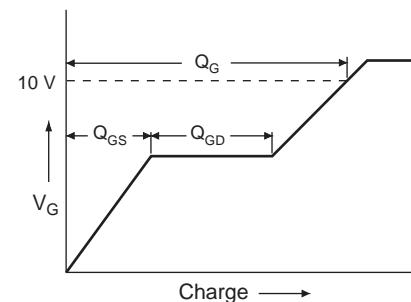


Fig. 16 - Basic Gate Charge Waveform

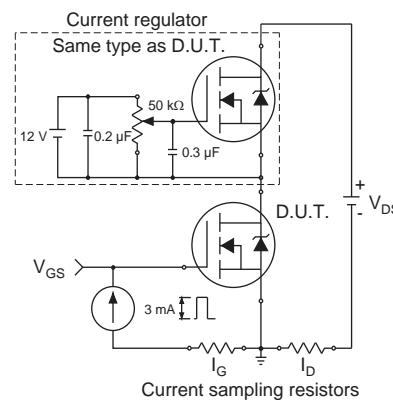
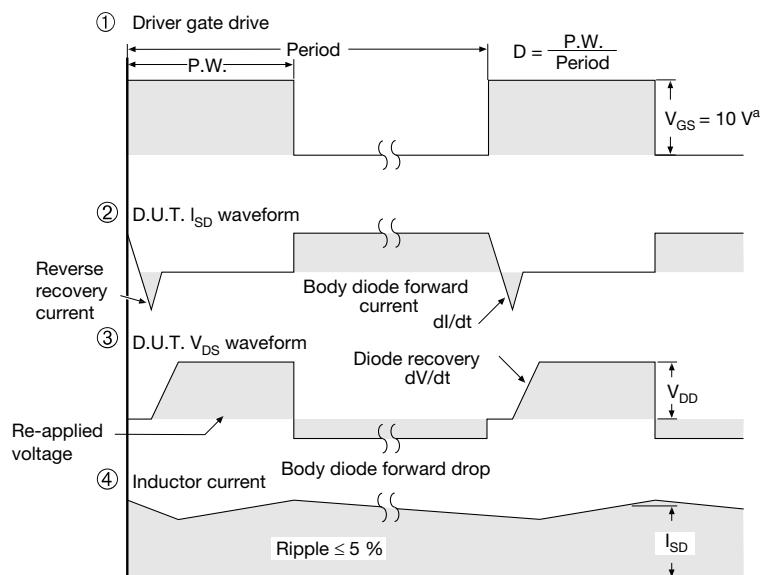
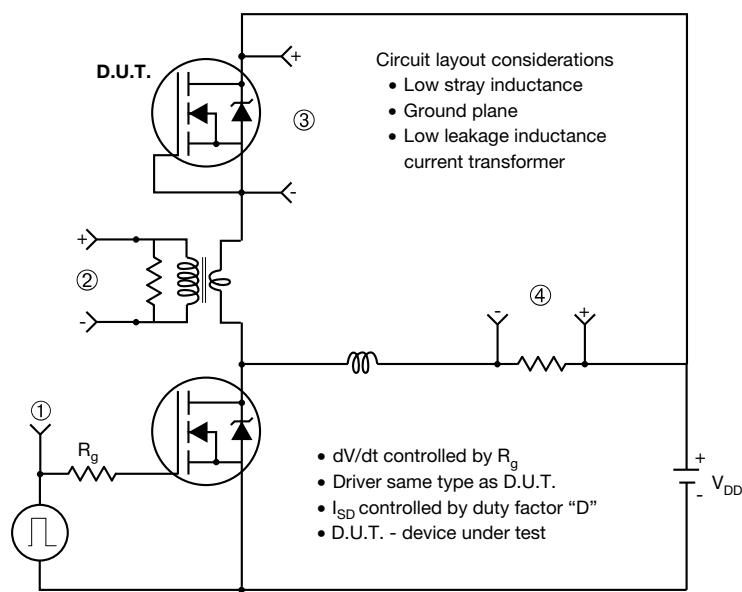
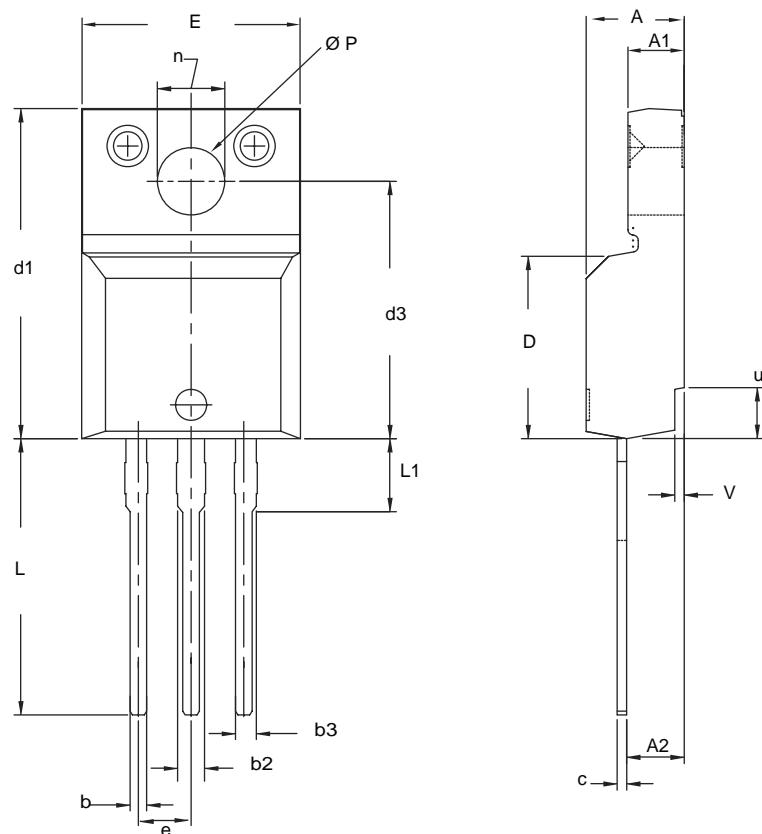


Fig. 17 - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

**Note**

a.  $V_{GS} = 5 \text{ V}$  for logic level devices

Fig. 18 - For N-Channel

**TO-220 FULLPAK (HIGH VOLTAGE)**


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØP	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

 ECN: X09-0126-Rev. B, 26-Oct-09  
 DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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