LP4076, LP4076E

36V/1A Standalone Single-Cell Linear Charger

Features

- Easy-to-use standalone single-cell charger
- High input voltage linear charger
  - Support up to 7V operating input voltage with 36V absolute maximum input rating
  - Maximum BAT withstand voltage up to 14V
  - Programmable up to 1A fast charge current
  - -0.5/+1% regulated output voltage accuracy
  - Trickle current 10% of fast charge current
  - Termination current 10% of fast charge current
- High integration
  - Integrated reverse blocking MOSFET
  - Built-in charge current sensing
  - Internal loop compensation
  - Integrated charge status indication
- Support full charge cycle of trickle current mode, constant current (CC) mode, constant voltage (CV) mode, charge termination and automatic recharge
- BAT leakage current 30nA typical
- Protection features
  - Input under-voltage lockout (UVLO)
  - Input over-voltage protection (OVP)
  - Battery reverse connection protection
  - Thermal regulation
  - Cold/hot battery temperature protection
- RoHS Compliant and 100% Lead (Pb)-Free
- Package: ESOP-8

Applications

- Wireless Speaker
- Cordless Power Tools
- Gaming Devices
- Portable Media Players
- Handheld Battery-Powered Devices
- Charging Docks and Cradles
- Power Banks
- E-Cigarettes

General Description

The LP4076/LP4076E is a highly advanced linear charger for single-cell Li-Ion and Li-Polymer batteries. The device is ideally suited for portable applications due to low number of external components required.

The device employs a full charge algorithm with trickle current, constant current (CC), constant voltage (CV) modes, charge termination and automatic recharge. The device supports charge current up to 1A, programmed by an external resistor. The device can withstand an input voltage up to 36V, which can protect the charger from any accidental insertion of a high-voltage supply or a hot insertion. The device can withstand a BAT voltage up to 14V, which is suited for power battery applications. Without an input supply, the battery leakage current is only 30nA typical.

The device provides various safety features for battery charging, including input under voltage lockout (UVLO), input over-voltage protection (OVP), battery reverse connection protection, cold/hot battery temperature protection, and thermal regulation protection that is implemented by reducing the charge current when the junction temperature reaches 140℃.

The LP4076/LP4076E is available in an ESOP-8 package.

Order Information

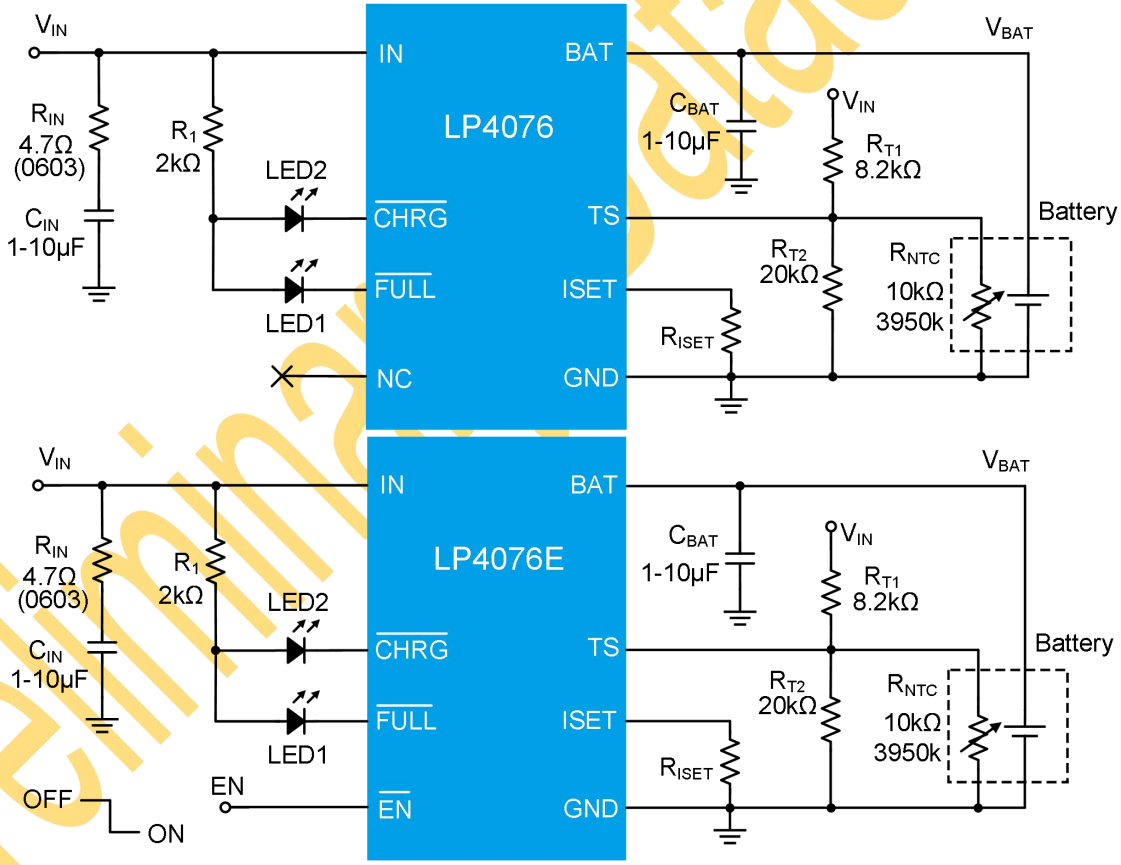
LP4076 □ □□ □-□□

- Battery Voltage
  Default:4.20V
  435:4.35V
- F: Pb - Free
- Package Type
  SP:ESOP-8
- Package Type
  E: With EN Function

Device Information

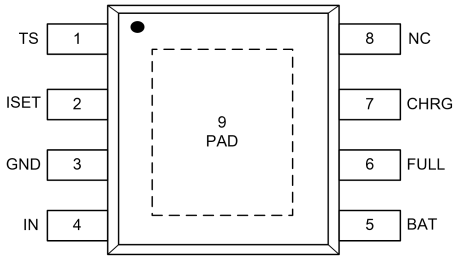
Part Number	Top Marking	Battery Voltage	Moisture Sensitivity Level	Package	Shipping
LP4076SPF	LPS LP4076 YWX	4.20V	MSL3	ESOP-8	4K/REEL
LP4076ESPF	LPS LP4076E YWX	4.20V	MSL3	ESOP-8	4K/REEL
LP4076ESPF-435	LPS LP4076E 435YWX	4.35V	MSL3	ESOP-8	4K/REEL
Marking indication: Y: Production year. W: Production week. X: Series number.					

Typical Application Circuit

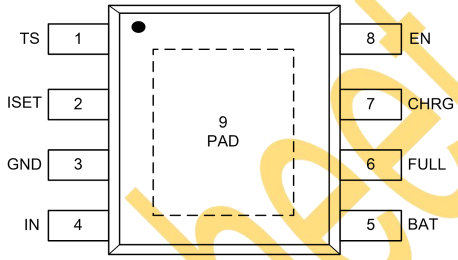


Pin Diagram

LP4076SPF
ESOP-8 (Top View)



LP4076ESPF
ESOP-8 (Top View



Pin Description

Pin	Name	Description
1	TS	Battery Temperature Sense Thermistor Input. This pin senses the temperature of the battery pack and charge is suspended if the battery temperature is out of range.
2	ISET	Fast Charge Current Program Pin. Connect this pin with an external resistor R_{ISET} to GND to program the fast charge current.
3	GND	GND. Connect to the system ground.
4	IN	Positive Supply Voltage Input. Place a 4.7Ω resistor and a 1-10μF ceramic capacitor in series from IN to GND, and place the components as close as possible to IC.
5	BAT	Battery Pin. Connect to the battery, A 1-10μF capacitor is needed typically.
6	FULL	Open-Drain Status Output. When the device is in charging state, the FULL pin is pulled high by an external pull-up resistor. When the charge cycle is completed, the pin is pulled low by an internal NMOS.
7	CHRG	Open-Drain Charge Status Output. When the device is in charging state, the CHRG pin is pulled low by an internal NMOS. When the charge cycle is completed, the internal NMOS turned-off, the pin could be pulled high by an external pull-up resistor.
8	EN	Charge Enable Input. Low active. (LP4076ESPF)
	NC	No Connection. (LP4076SPF)
9	PAD	Ground reference for the device that is also the thermal pad used to conduct heat from the device.

Absolute Maximum Ratings (1)

- IN to GND ---------- -0.3V to 36V
- CHRG, FULL to GND ---------- -0.3V to 28V
- BAT to GND---------- -5V to 14V
- EN, ISET, TS to GND---------- -0.3V to 6.5V
- Maximum Junction Temperature (T_J) ---------- 150℃
- Storage Temperature ---------- -55℃ to 150℃
- Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

- HBM (Human Body Model) ---------- 2kV
- MM (Machine Model) ---------- 200V

Thermal Information

- Junction-to-Ambient Thermal Resistance (R_{THJA}) ---------- 50℃/W
- Junction-to-Case Thermal Resistance (R_{THJC}) ---------- 36℃/W
- Maximum Power Dissipation (P_D, T_A=25°C) ---------- 2W

Recommended Operating Conditions

- Input Voltage ---------- 4.5V to 6V
- Maximum Charge Current ---------- 1A
- Operating Junction Temperature Range (T_J) ----------20℃ to 140℃
- Operating Ambient Temperature Range (T_A) ---------- -20℃ to 85℃

Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = 5V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range		4.5	5	6	V
$I_{Standby}$	Input Standby Current	Standby mode (Charge terminated) V_{EN}=0V		190		μA
$I_{Shutdown}$	Input Shutdown Current	V_{EN}=5V(LP4076ESPF)		27		μA
V_{UVLO}	Under Voltage Lockout of V_{IN}	V_{IN} Rising	3.3	3.5	3.7	V
V_{UVLO_HYS}	V_{UVLO} Hysteresis	V_{IN} Falling		200		mV
V_{OVP}	Over-Voltage Protection Threshold Voltage	V_{IN} Rising	6.7	7	7.3	V
V_{OVP_HYS}	OVP Hysteresis	V_{IN} Falling		300		mV
BATTTERY CHARGER						
V_{FLOAT}	Regulated Output Voltage		4.179	4.2	4.242	V
		LP4076ESPF-435	4.306	4.35	4.394	
I_{CC}	Fast Charge Current	R_{ISET}=3.4kΩ, Constant Current Mode	460	500	540	mA
		R_{ISET}=17kΩ, Constant Current Mode	90	100	110	mA
I_{TERM}	Termination Current Threshold	R_{ISET}=3.4kΩ, Constant Voltage Mode		10%		I_{CC}
I_{TRIKL}	Trickle Charge Current	V_{BAT}<V_{TRIKL}, R_{ISET}=3.4kΩ		10%		I_{CC}
V_{TRIKL}	Trickle Charge Threshold Voltage	V_{BAT} Rising	2.75	2.9	3.05	V
V_{TRHYS}	Trickle Charge Hysteresis Voltage	V_{BAT} Falling		200		mV
ΔV_{RECHRG}	Battery Recharge Voltage Difference Threshold (V_{FLOAT} -V_{RECHRG})	V_{BAT} Falling	100	150	200	mV
$V_{Headroom}$	V_{IN}-V_{BAT} threshold Voltage	V_{BAT}=3.7V, V_{IN} Rising	80	115	150	mV
$V_{Headroom\_HYS}$	V_{IN}-V_{BAT} threshold Voltage Hysteresis	V_{BAT}=3.7V, V_{IN} Falling		60		mV
T_{J_LIMIT}	Junction Temperature Limit	Thermal Foldback Protection State		140		℃
R_{DS}	IN-BAT MOSFET on-resistance	Charge Current=500mA		750		mΩ

BAT LEAKAGE CURRENT						
$I_{BAT\_Leakage}$	Battery Leakage Current	LP4076SPF V_{IN} floating, V_{BAT}=4.2V		0.03		μA
ISET/CHARG/FULL PINs						
V_{ISET_CC}	ISET Pin Voltage	Constant Current Mode		1		V
V_{ISET_TR}		Trickle Current Mode		0.1		V
V_{STAT}	STAT Pin Output Low Voltage	I_{STAT}=5mA			0.5	V
I_{STAT}	CHRG/FULL Pin Sink Current				5	mA
EN PIN (LP4076ESPF)						
V_{EN_ON}	EN Logic-Low Voltage Threshold	EN Falling			0.4	V
V_{EN_OFF}	EN Logic-High Voltage Threshold	EN Rising	1.4			V
I_{EN}	EN pin leakage current	V_{EN}=5V or V_{EN}=0V	-1		1	μA
TS PIN						
V_{NTC_H}	NTC threshold (Hot)	V_{NTC_H} falling, percentage to V_{IN}	28%	30%	32%	V_{IN}
$V_{NTC\_H\_HYS}$	V_{NTC_H} Hysteresis			2%		V_{IN}
V_{NTC_C}	NTC threshold (Cold)	V_{NTC_C} rising, percentage to V_{IN}	58%	60%	62%	V_{IN}
$V_{NTC\_C\_HYS}$	V_{NTC_C} Hysteresis			3%		V_{IN}

Typical Characteristics

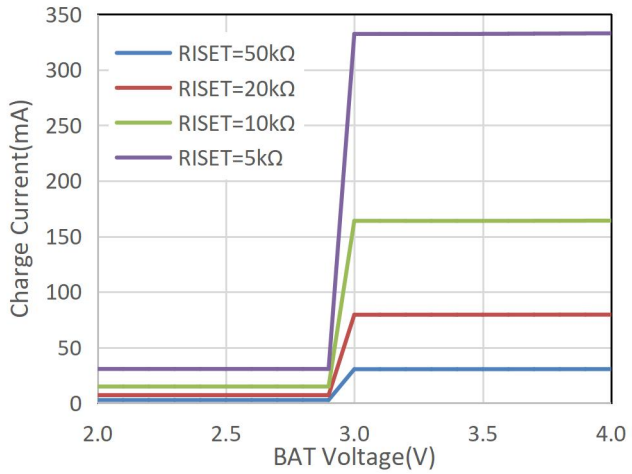


Figure 1. Charge Current vs BAT Voltage
V_{IN}=5V, 25℃

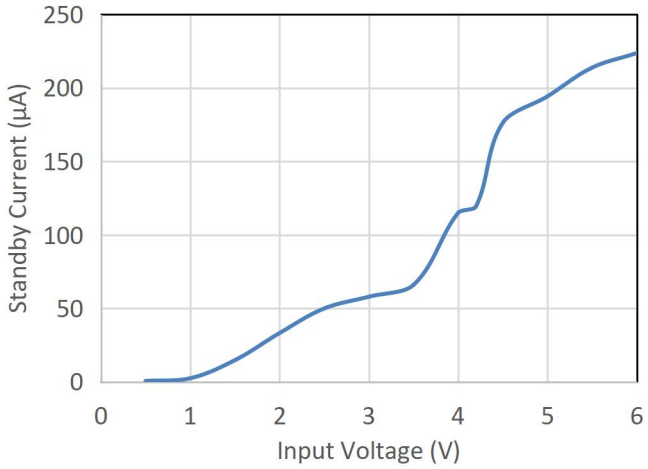


Figure 2. Input Standby current vs Input Voltage
Charge terminated, 25℃

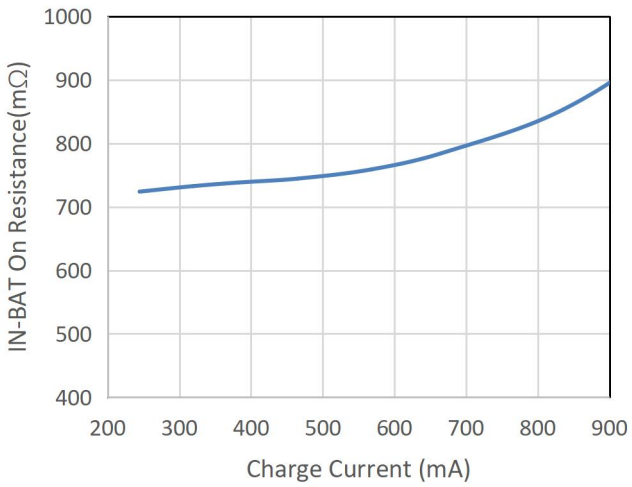


Figure 3. VIN-BAT ON-Resistance vs Charge Current
V_{BAT}=3.7V , 25℃

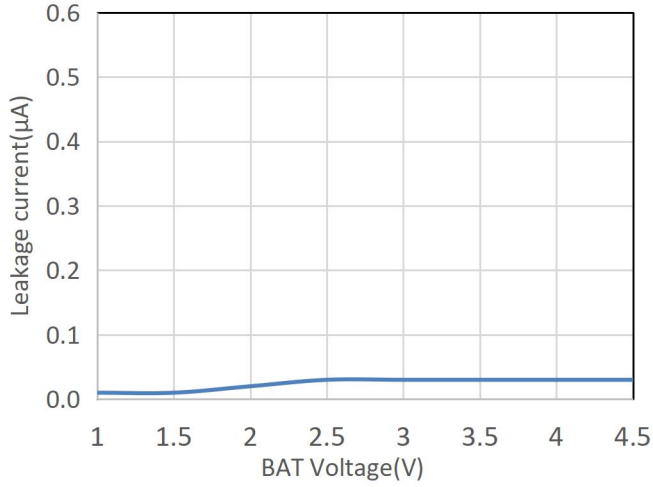


Figure 4. BAT Leakage Current vs V_{BAT}
V_{IN}=Floating, 25℃

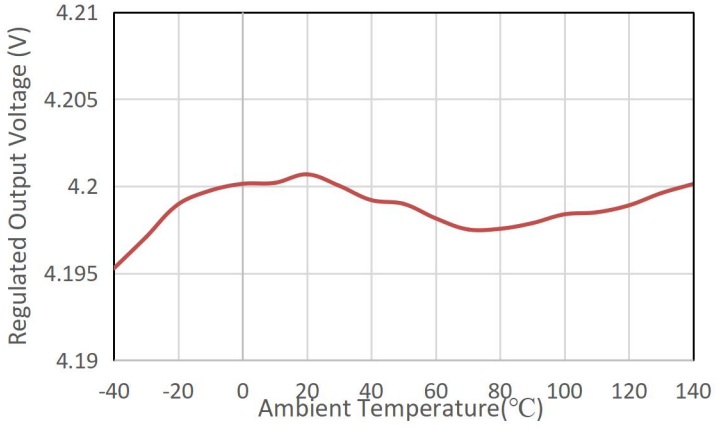
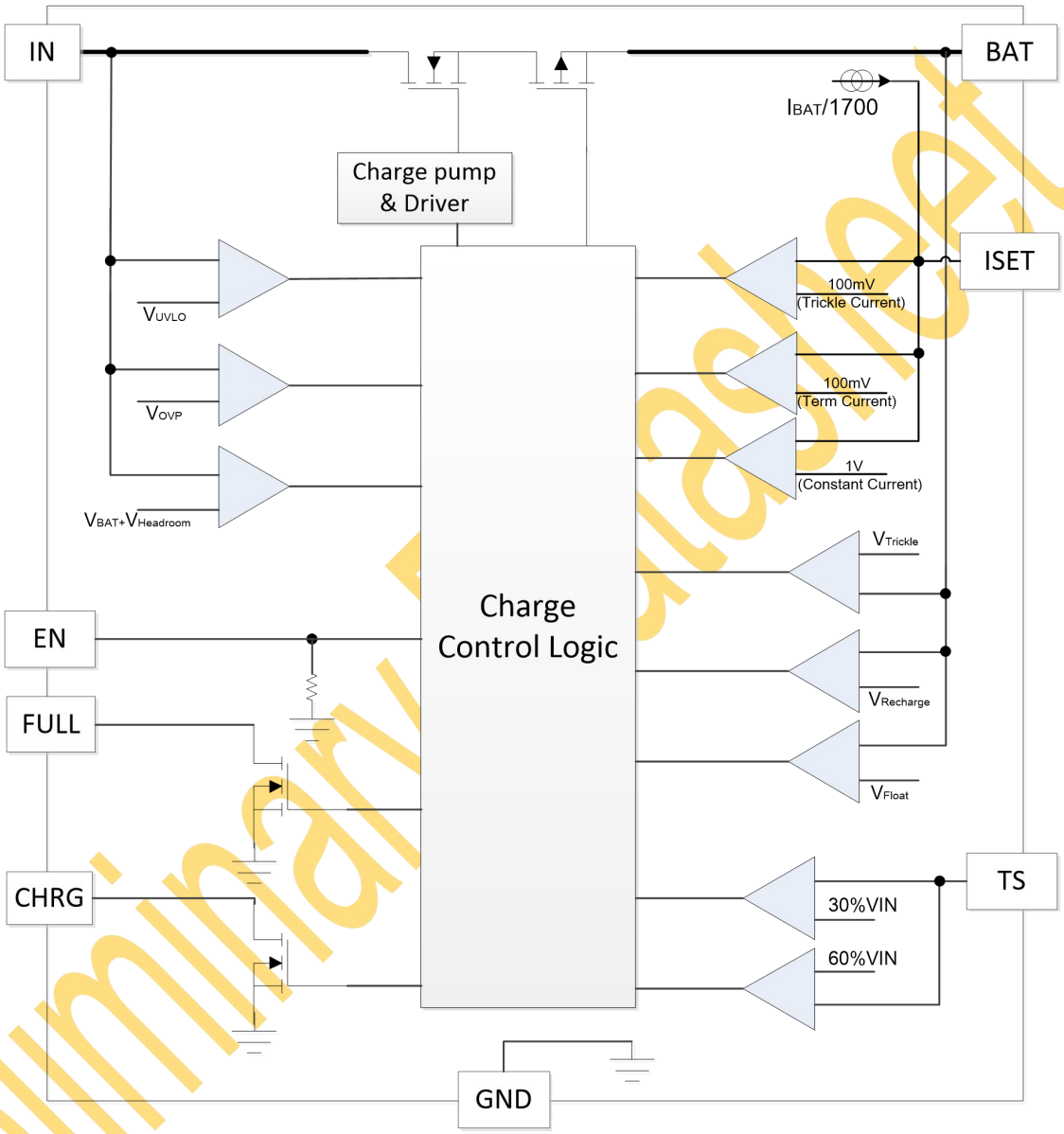


Figure 5. Regulated Output Voltage (V_{FLOAT}) vs Ambient Temperature

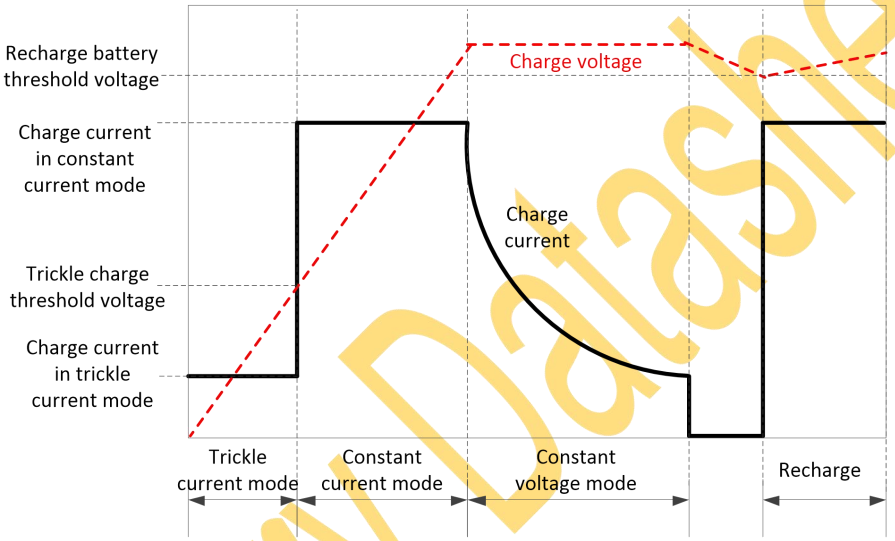
Functional Block Diagram



Detailed Description

Overview

The LP4076/LP4076E is a highly advanced linear charger with up to 1A maximum charge current for single cell Li-Ion and Li-Polymer batteries. The device charges the battery with full charge cycle: trickle current mode, constant current mode (CC), constant voltage mode (CV), charge termination and recharge. The typical charge profile can be showed as the figure below.



When the battery voltage is lower than Trickle Charge Threshold Voltage (V_{TRIKL}, 2.9V typical), the device charges in the trickle current mode, the charge current will be set to Trickle Charge Current (I_{TRIKL}), which is approximately 10% of the ISET programmed Fast Charge Current (I_{CC}) to bring the battery voltage up to a safe level for full current charging. When the battery voltage rises to V_{TRIKL}, the device enters the constant current mode, where the charge current is 100%I_{CC}. When the battery voltage approaches the Regulated Output Voltage (V_{FLOAT}), the device goes to constant voltage mode, the charge current starts to decrease. When the charge current is lower than the Termination Current threshold (I_{TERM}), which is 10%I_{CC}, the device will terminate the charging.

The device will automatically recharge the battery while the battery voltage drops ΔV_{RECHRG} (150mV, typical) from the Regulated Output Voltage (V_{FLOAT}).

ISET Programming Fast Charge Current

The Fast Charge Current (I_{CC}) is set by a resistor (R_{ISET}) connecting from the ISET pin to GND. The relationship between I_{CC} and the programming resistance is established by the following formula:

$$I_{CC} = \frac{V_{ISET} \times 1700}{R_{ISET}}$$

where V_{ISET}=1V typical.

Charge Termination and Automatic Recharge

A charge cycle will be terminated when the charge current falls to I_{TERM} (10%I_{CC}, typical), as the battery voltage reached V_{FLOAT}. The function is implemented by monitoring the ISET pin voltage and comparing to a 100mV threshold voltage. When the ISET pin voltage falls below 100mV for longer than 1ms typically, the charging will be terminated.

Once the charge cycle is terminated, the LP4076/LP4076E continuously monitors the voltage on the BAT pin by a comparator. A new charge cycle starts when the battery voltage drops by a voltage difference ΔV_{RECHRG} (150mV, typical) from V_{FLOAT}, which means the battery level drops to approximately 80% to 90% capacity. This ensures that the battery always keeps at or near a fully charged condition.

Undervoltage Lockout (UVLO) and Minimum Headroom Voltage

An internal UVLO circuit monitors the input voltage and keeps the device in Shutdown mode until the input supply rises above the UVLO threshold. The UVLO circuitry has a built-in hysteresis of 200 mV. The UVLO circuit is always active.

In addition, the input supply must be $V_{Headroom}$ (115mV, typical) higher than the battery voltage before the LP4076/LP4076E become operational. Whenever the input supply is below the UVLO threshold or lower than a voltage of $V_{Headroom}$ above the VBAT pin, the device is in Shutdown mode.

Enable Function (LP4076E only)

The LP4076E features an enable/disable function. An input “Low” signal or floating connection on EN pin will enable the device. To ensure the device to be active, the EN low voltage level must be lower than 0.4V. The device will enter the Shutdown mode when the voltage on the EN pin is higher than 1.4V. If the enable function is not needed in a specific application, the EN pin can be shorted to GND or left floating to keep the device continuously active.

Charge Status Indicator (CHRG & FULL)

When the input voltage is above the V_{UVLO} and above the voltage of V_{BAT}+$V_{Headroom}$, but lower than V_{OVP} (V_{IN}<V_{OVP}), CHRG pin and FULL pin have two different states: strong pull-down (~5mA) and high impedance. The strong pull-down state of CHRG implemented by an internal NMOS indicates that the device is in a charge cycle. After the charge current decreased to I_{TERM} in CV mode and then charging terminated, the CHRG pin will become high impedance, the FULL pin will become pull-down state.

Function	CHRG	FULL
Charging	Low	Hi-Z
Charge Terminated	Hi-Z	Low

Thermal Regulation Foldback

An internal thermal regulation foldback loop reduces charge current if the junction temperature reaches a preset value of approximately 140℃ to prevent further temperature rise. This function protects the device from excessive temperature and allows the user to get the limits of the power handling capability of a given circuit board without the risk of damaging the device. The charge current can be set according to typical ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.
Charge termination function will not be active when thermal foldback regulation protection is happening.

Battery Temperature Detection

The LP4076/LP4076E continuously monitors the battery temperature by measuring the voltage between the TS pin and GND pin. The devices compare V_{TS} to its internal thresholds V_{NTC_H} and V_{NTC_C} that is derived from internal resistor divider from V_{IN} to GND, and then determine whether charging is allowed. The temperature sensing circuit is immune to any fluctuation in V_{IN} because both the external voltage divider and the internal thresholds (V_{NTC_H} and V_{NTC_C}) are referenced to V_{IN}.

The resistor values of R_{T1} and R_{T2} are calculated by the following equations:

For NTC Thermistors:

$$R_{T1} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{(R_{TL} - R_{TH})K_1K_2}$$

$$R_{T2} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{R_{TL}(K_1 - K_1K_2) - R_{TH}(K_2 - K_1K_2)}$$

For PTC Thermistors:

$$R_{T1} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{(R_{TH} - R_{TL})K_1K_2}$$

$$R_{T2} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{R_{TH}(K_1 - K_1K_2) - R_{TL}(K_2 - K_1K_2)}$$

$K_{1(VTS\_H)}$=30%, $K_{2(VTS\_C)}$=60%.

where R_{TL} is the low temperature resistance and R_{TH} is the high temperature resistance of thermistor, as specified by the thermistor manufacturers. If the allowed charge temperature is 0 to 45 ℃, for a typical 10kΩ-3950K NTC thermistor, R_{TL} = 32.6kΩ, R_{TH}=4.4kΩ, then R_{T1}=8.2kΩ and R_{T2}=20kΩ.

Application Information

Thermal Consideration

Due to low efficiency of linear charging, the most important factor is the thermal design, which is a direct function of input voltage, output charge current and thermal impedance between the battery charger and the ambient cooling air.

The power dissipation can be calculated approximately:

$$P_D = (V_{IN} - V_{BAT}) \times I_{BAT}$$

where P_D is the power dissipation, V_{IN} is the input supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current.

The worst-case situation is when the device has transitioned from the trickle current mode to the constant current mode. In this situation, the battery charger has to dissipate the maximum power.

In this case, with a 5V input voltage source, 1A fast charge current, the max power dissipation could be:

$$P_{Dmax} = (5V - 2.9V) \times 1A = 2.1W$$

This power dissipation with the battery charger in the ESOP-8 package may cause thermal regulation foldback to reduce the charge current. Then a trade-off must be made between the charge current and thermal requirements of the charger.

External Capacitors

In order to maintain good stability in the whole charge cycle, a capacitance of 1-10μF is recommended to bypass the BAT pin to GND. In addition, the battery and interconnections appear inductive at high frequencies. These elements are in the control feedback loop during constant voltage mode. Therefore, the bypass capacitance may be necessary to compensate for the inductive nature of thew battery pack.

ISET Resistor

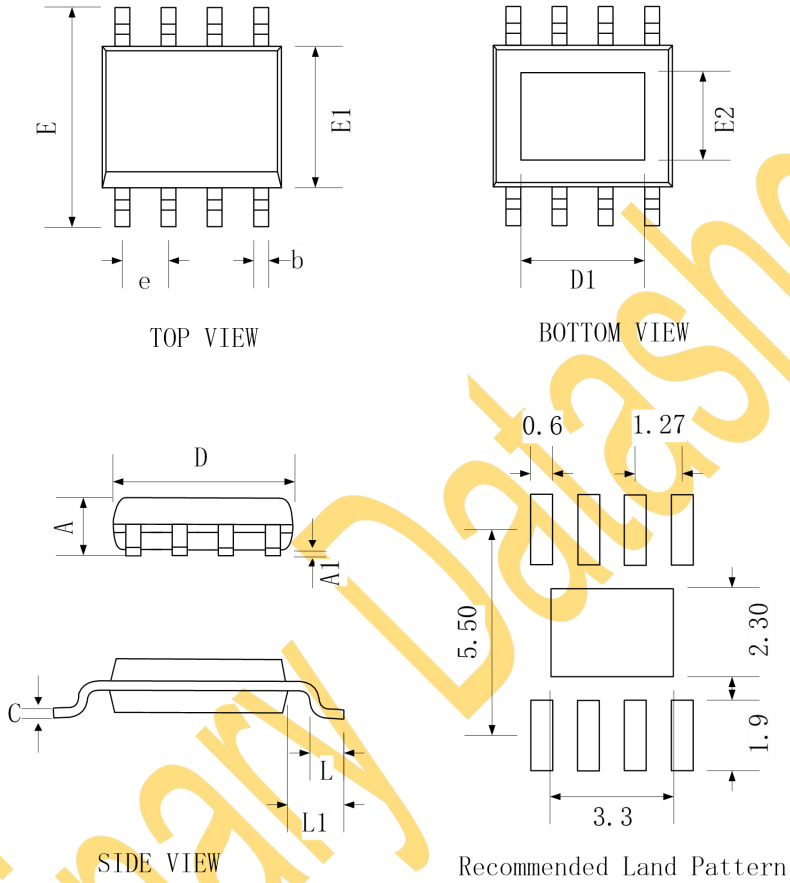
In order to assure the accuracy of the charge current, better than 1% precision resistance is recommended.

Layout Consideration

For optimum voltage regulation, place the battery pack as close as possible to the device's BAT and GND pins. This is recommended to minimize voltage drops along the high current-carrying PCB traces. If the PCB layout is used as a heat sink, adding many vias in the heat sink pad can help conduct more heat to the PCB backplane, thus reducing the maximum junction temperature. It is also recommended to place the capacitor C_{IN} and C_{OUT} as close as possible to the corresponding pins and the GND pin.

Packaging Information

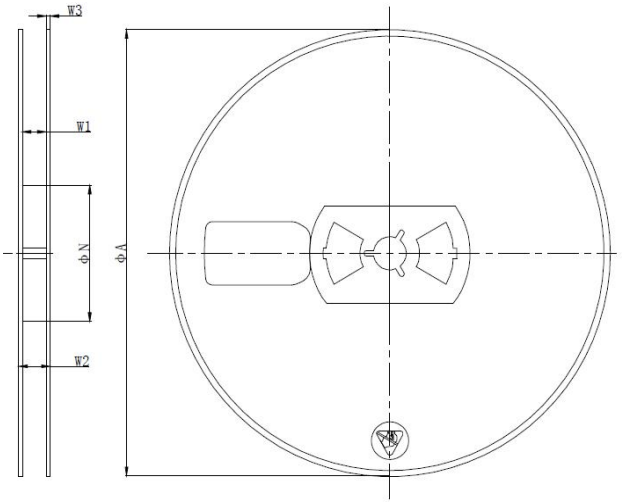
ESOP-8



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.00	-	0.15
b	0.30	0.40	0.50
c		0.20 REF	
D	4.70	4.90	5.10
D1		3.2 REF	
E	5.70	6.00	6.30
E1	3.70	3.90	4.10
E2		2.30 REF	
e		1.27 BSC	
L	0.40	0.60	0.80
L1		1.05 REF	

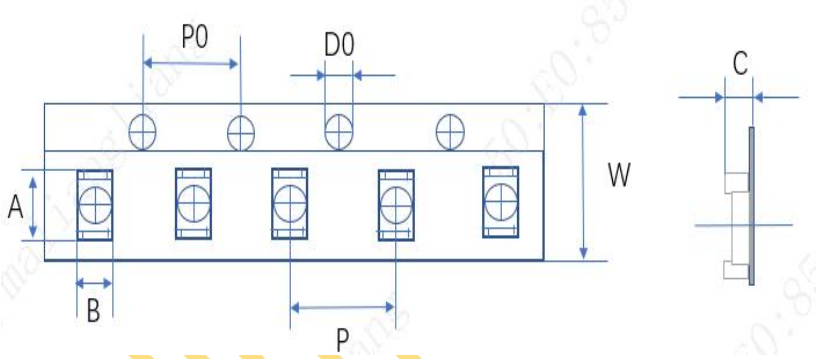
Tape and Reel Information

REEL DIMENSIONS



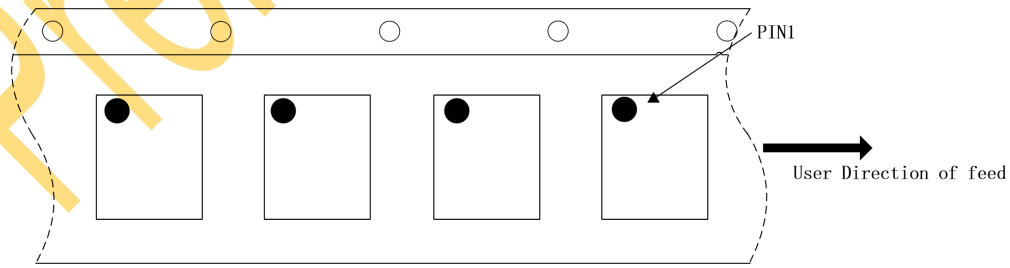
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	325.00	329.00	333.00
W2	15.00	17.00	19.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	6.20	6.60	7.00
B	5.10	5.50	5.90
P0	3.80	4.00	4.20
P	7.80	8.00	8.20
D0	1.30	1.50	1.70
W	11.90	12.00	12.30
C	1.90	2.10	2.30

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

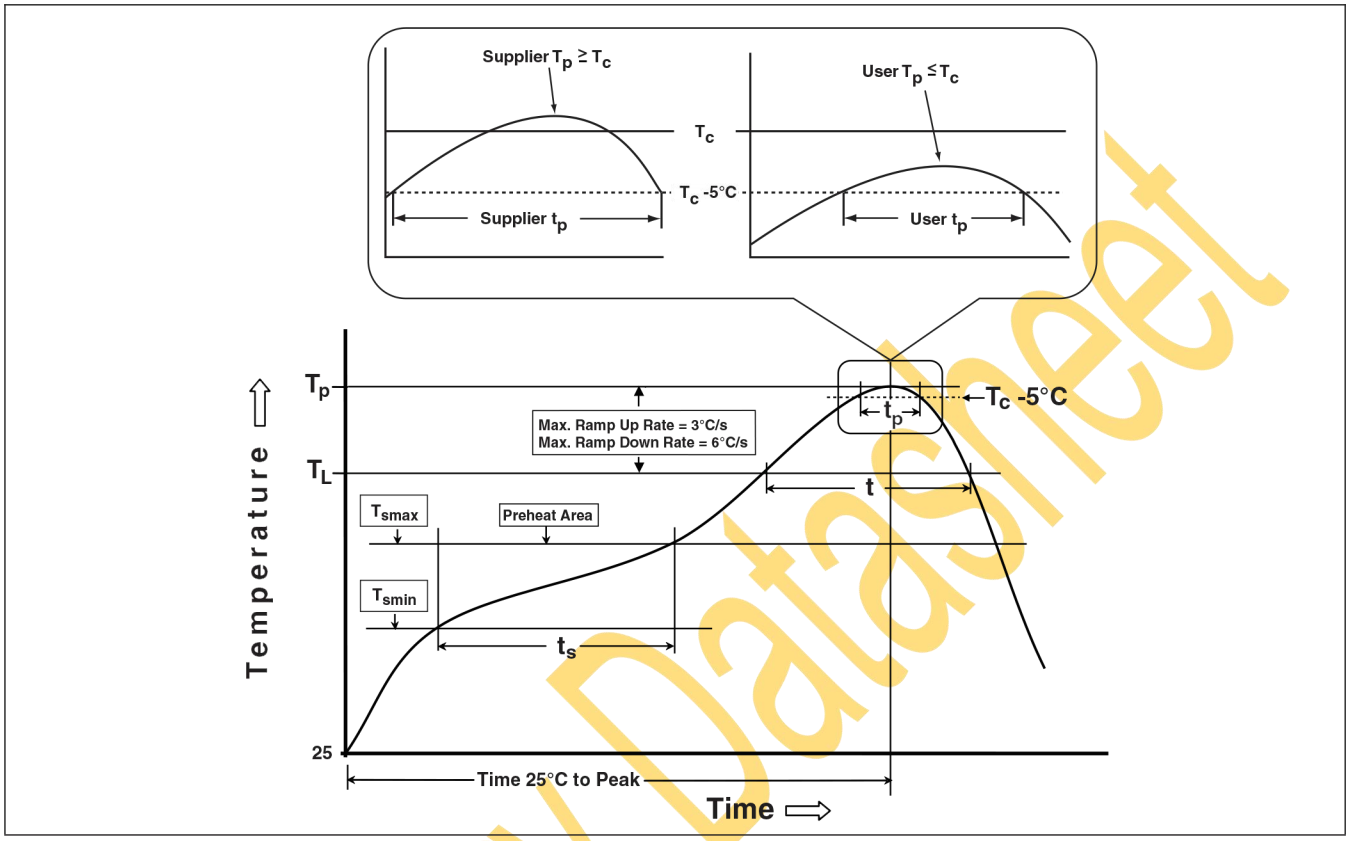


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;