

Parameters Subject to Change Without Notice

## DESCRIPTION

JW<sup>®</sup>7700A is a synchronous rectifier for Flyback converters. It integrates a 40V power MOSFET that can replace Schottky diode for high efficiency. It turns on the internal MOSFET if the  $V_{SW} < -500\text{mV}$  and turns it off before the current from GND to SW is lower than zero.

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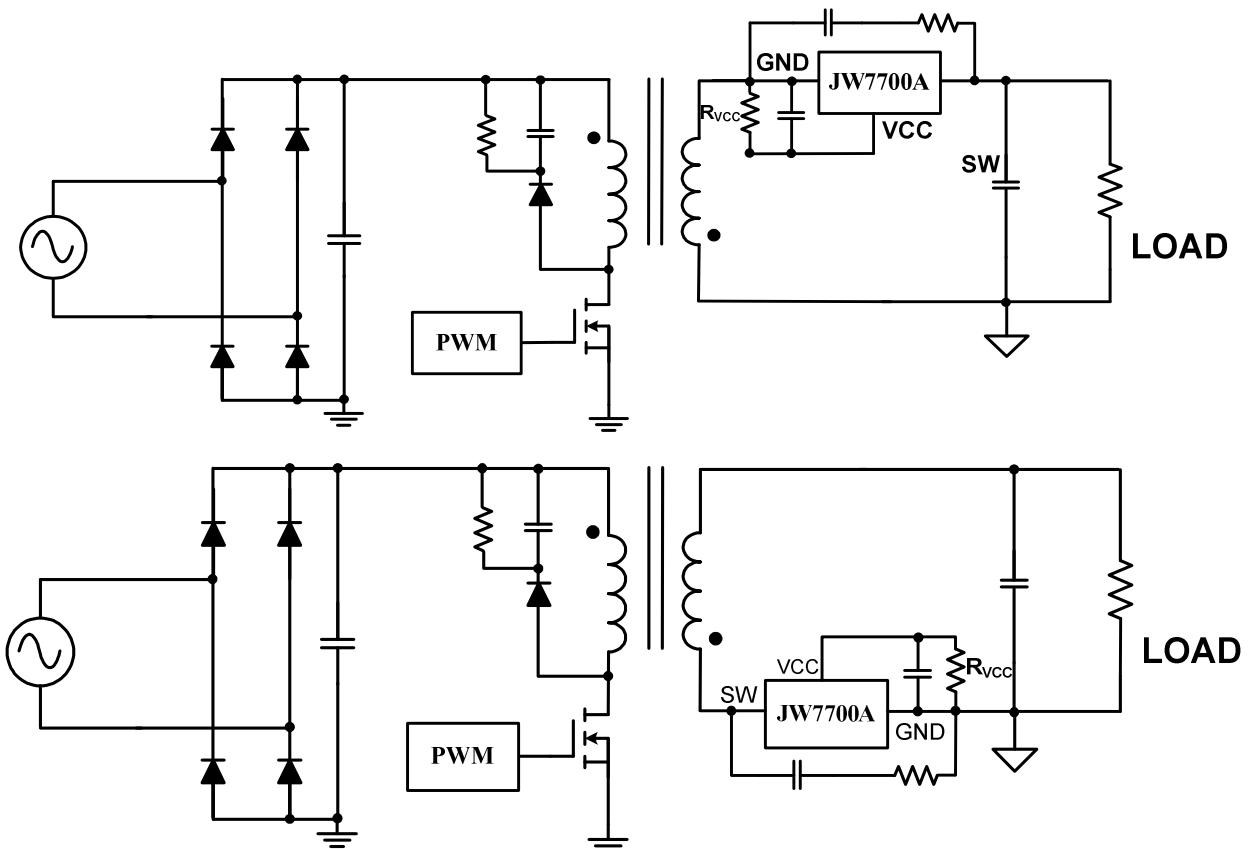
## FEATURES

- Supports DCM and Quasi-Resonant Flyback converter
- Integrated 15mΩ 40V Power MOSFET
- Supports High-side and Low-side Rectification
- No need external power supply

## APPLICATIONS

- Flyback converters
- Adaptors

## TYPICAL APPLICATION



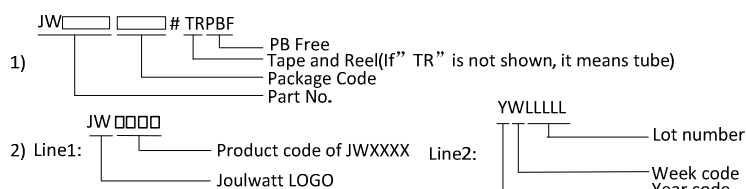
Note 1:  $R_{VCC}$  is recommended in case IC is damaged in CCM.

Note 2:  $D_{VCC}$  is recommended if VCC voltage is too low in light load.

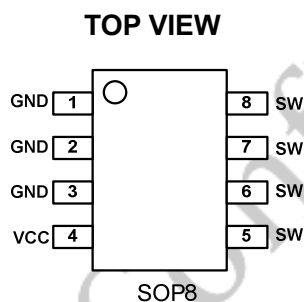
## ORDER INFORMATION

DEVICE <sup>1)</sup>	PACKAGE	TOP MARKING <sup>2)</sup>
JW7700ASOPB#TRPBF	SOP8	JW7700A YWLLLLL

## Notes:



## PIN CONFIGURATION

ABSOLUTE MAXIMUM RATING<sup>1)</sup>

SW PIN .....	40V
VCC PIN .....	24V
Maximum Power Dissipation <sup>2)</sup> .....	2.5W
Junction Temperature <sup>3)</sup> .....	150°C
Lead Temperature .....	260°C
Storage Temperature .....	-65°C to 150°C
ESD Susceptibility (Human Body Model) .....	2kV

## RECOMMENDED OPERATING CONDITIONS

SW Pin .....	20V to 35V
VCC PIN .....	7V to 9V
Operation Junction Temp. ....	-40°C to 125°C

THERMAL PERFORMANCE<sup>4)</sup>

	$\theta_{JA}$	$\theta_{JC}$
SOP8 .....	96	45°C/W

**Note:**

- 1) Exceeding these ratings may damage the device.
- 2)  $T_A=25^{\circ}\text{C}$ . The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J(\text{MAX})$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(\text{MAX})=(T_J(\text{MAX})-T_A)/\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Measured on JESD51-7, 4-layer PCB.

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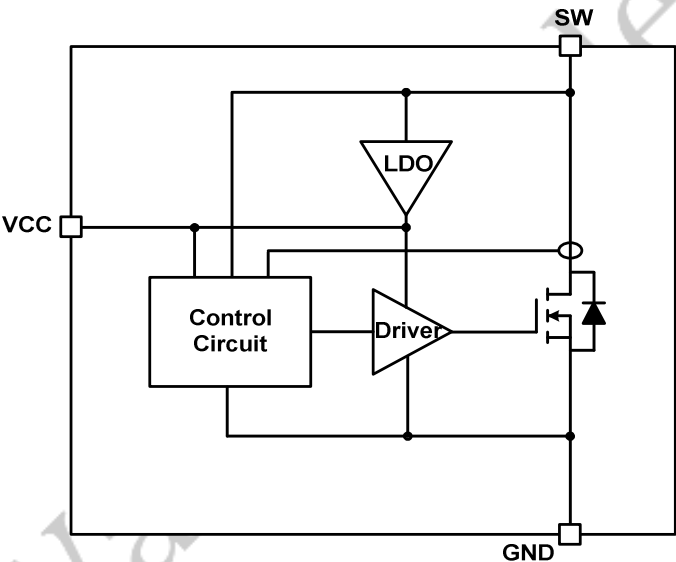
## ELECTRICAL CHARACTERISTICS

<i>TA = 25°C, unless otherwise stated.</i>						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
<b>VCC Section</b>						
VCC Operation Voltage	$V_{CC}$	SW=30V, VCC=0.1uF	7.4	7.75	8.1	V
VCC Start up Voltage	$V_{CC\_STAR\ UP}$		3.6	3.8	4	V
VCC UVLO	$V_{CC\_UVLO}$		3.5	3.65	3.8	V
Quiescent Current	$I_Q$	$V_{CC}=6.5V$ , $C_{VCC}=0.1uF$	70	85	100	uA
<b>Internal MOS Section</b>						
Internal MOS $R_{dson}$	$R_{dson}$	VCC=10V, Isw=10A		15		mΩ
Maximum Peak Current	$I_{peak}$	$T_J=25^\circ C$		30		A
Drain Current-continuous	$I_D$	$T_J=25^\circ C$		8		A
Internal MOS turn on delay	$T_{DON}$			24		nS
Internal MOS turn off delay	$T_{DOFF}$			10		nS
Internal MOS turn on minimum time	$T_{ON\_MIN}$			1		uS
Internal MOS turn off minimum time	$T_{OFF\_MIN}$		2.5	3.5		uS
<b>SW Section</b>						
Internal MOS turn on Threshold	$V_{MOS\_ON}$			-0.5		V
SW to GND Breakdown Voltage	$V_{(BR)DSS}$	VCC=9V, Isw=250uA	40			V

PIN DESCRIPTION

Pin No. SOP	Name	Description
1、2、3	GND	Ground
4	VCC	Power supply, Bypass a capacitor between VCC and GND.
5、6、7、8	SW	Internal Power MOSFET Drain.

BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### Operation

JW7700A is a synchronous rectifier, it can replace the Schottky to improve the efficiency in Flyback converters. It supports operation in DCM and Quasi-Resonant Flyback converters. It can power itself through the internal LDO during the turn-off period, a 0.1uF capacitor is needed between VCC and GND.

### Turn-on Blanking Time

The control circuitry contains a blanking function. When the internal MOSFET is turned on, it at least last for some time, the turn on blanking time is about 1uS. During the turn on blanking period, the turn off threshold is not totally blanked, but changes the threshold current. This assures that the internal MOSFET can always be turned off even during the blanking period.

### Under-Voltage Lockout (UVLO)

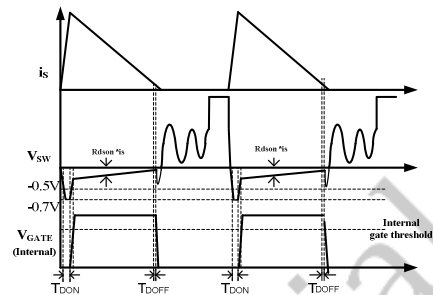
When the VCC is below UVLO threshold, the internal MOSFET is turned off and never turned on before the VCC exceeds the startup voltage.

### Turn On Phase

The switch current first flows through the body diode of integrate MOSFET, which generates a negative  $V_{SW}$ . When the  $V_{SW}$  is higher than 0.7V and then  $V_{SW}$  is lower than  $V_{MOS\_ON}$ , it turns on the integrate MOSFET after 24ns delay.

### Turn Off Phase

The JW7700A senses the current of the internal MOSFET  $I_{SW}$ , before  $I_{SW}$  is lower than Internal MOS turn off threshold, the driver voltage of the switch is pulled down to zero after 10ns delay.



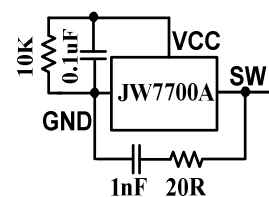
Turn on and turn off delay

### Startup

During the startup period, when the VCC is lower than startup voltage, the internal MOSFET is turned off. The current flows through body diode until the VCC exceeds the startup voltage.

### RC Snubber Circuit

In some applications (output short circuit protection), the inductor current may go into slight CCM condition. To avoid the voltage spike across the synchronous rectifier, we suggest RC snubber should be placed between SW and GND, and a resistor should be paralleled with VCC capacitor.



RC Snubber circuit

### PCB Layout Guidelines

1. The VCC pin must be locally bypassed with a capacitor.

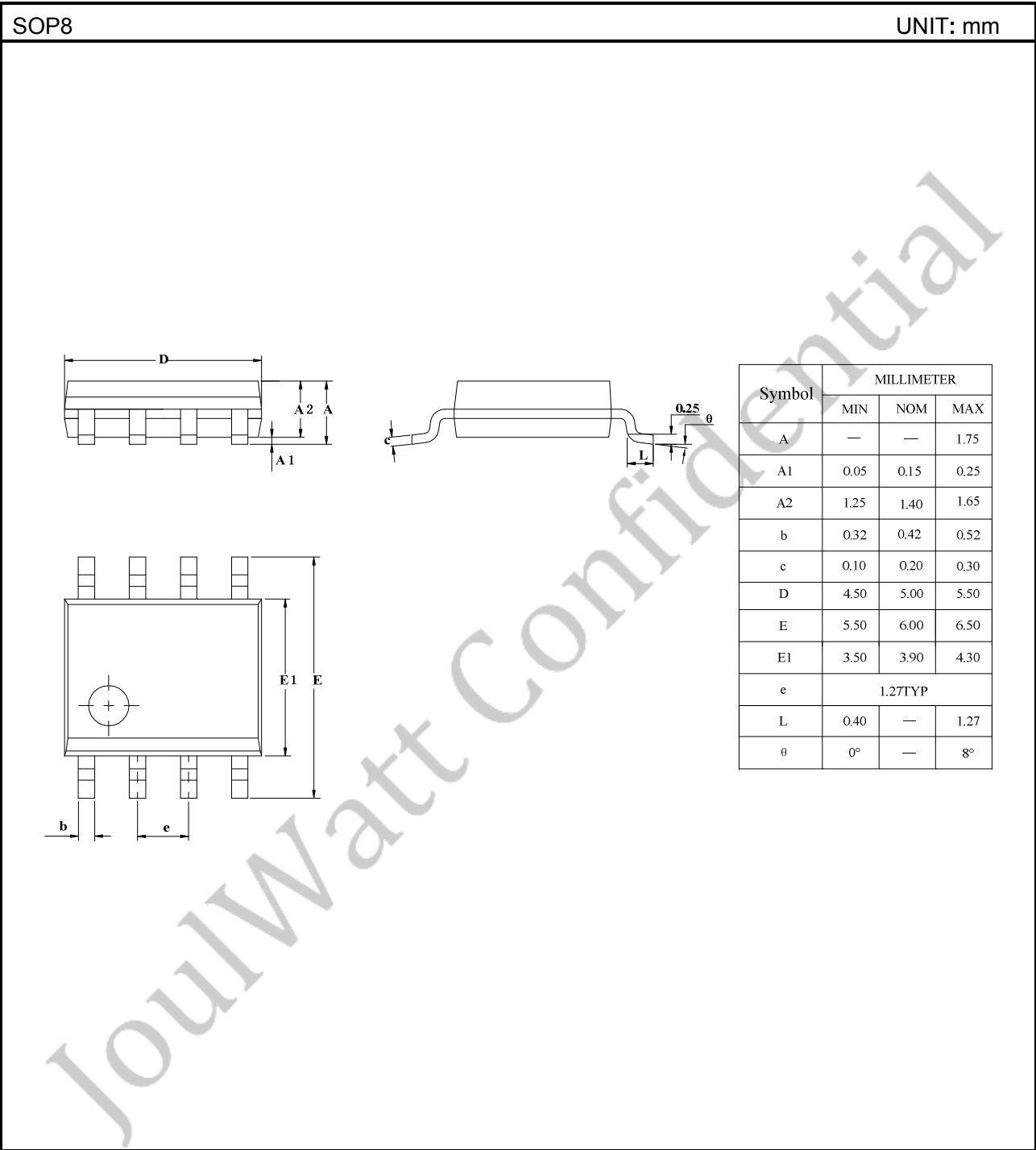
**Package and Bag Caution**

1. JW7700A is Moisture-Sensitive Devices and its MSL<sup>4)</sup> (Moisture-Sensitive Level) is level-3.
2. Calculated shelf life in sealed bag is 12 months at <40 °C and <90%RH(Relative Humidity).
3. Peak package body temperature<sup>4)</sup> is 260°C.
4. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
  - a) Mounted within 168 hours of factory at the condition  $\leq 30^{\circ}\text{C}/60\%\text{RH}$ .
  - b) Stored at <10%
5. Devices require bake before mounting if Humidity Indicator Car(HIC) is >10%RH when read at  $23 \pm 5^{\circ}\text{C}$ .
6. If baking is required, devices may be baked for 48 hours at  $125 \pm 5^{\circ}\text{C}$ . If device containers cannot be subjected to high temperature for shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure.

**Note:**

- 4) Level and body temperature defined by IPC/JEDEC J-STD-020.

PACKAGE OUTLINE





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