## Description

The HFDS4141uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.


SOP-8
(SOIC-8)

## General Features

$V_{DS}$ =-40V $I_D$ = -13A

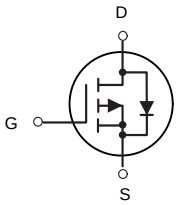
$R_{DS(ON)}$ < 19mΩ @ $V_{GS}$=10V

## Application

Battery protection

Load switch

Uninterruptible power supply




P-Channel MOSFET

## Package Marking and Ordering Information

| Product ID | Pack | Brand | Qty(PCS) |
|---|---|---|---|
| HFDS4141 | SOP-8(SOIC-8) | HXY MOSFET | 3000 |

## Absolute Maximum Ratings (Tc=25℃ unless otherwise noted )

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | - 40 | V |
| VGS | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_A$=25℃ | Drain Current[3], $V_{GS}$ @ 10V | -13 | A |
| IDM | Pulsed Drain Current[1] | -52 | A |
| $P_D$@$T_A$=25℃ | Total Power Dissipation | 3 | W |
| TSTG | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |
| Rthj-a | Maximum Thermal Resistance, Junction-ambient[3] | 41 | ℃/W |

## Electrical Characteristics ($T_J$ = 25°C, unless otherwise noted)

| Parameter | | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | | |
| Drain-Source Breakdown Voltage | | $V_{(BR)DSS}$ | $V_{GS}$ = 0V, $I_D$ = -250μA | -40 | - | - | V |
| Gate-body Leakage current | | $I_{GSS}$ | $V_{DS}$ = 0V, $V_{GS}$ = ±20V | - | - | ±100 | nA |
| Zero Gate Voltage Drain Current | $T_J$=25℃ | $I_{DSS}$ | $V_{DS}$ = -40V, $V_{GS}$ = 0V | - | - | -1 | μA |
| | $T_J$=100℃ | | | - | - | -100 | |
| Gate-Threshold Voltage | | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250μA | -1.0 | -1.5 | -2.2 | V |
| Drain-Source On-Resistance[4] | | $R_{DS(on)}$ | $V_{GS}$ = -10V, $I_D$ = -10A | - | 14.0 | 19 | mΩ |
| | | | $V_{GS}$ = -4.5V, $I_D$ = -5 A | - | 19.5 | 25 | |
| Forward Transconductance[4] | | $g_{fs}$ | $V_{DS}$ = -10V, $I_D$ = -10A | - | 44 | - | S |
| **Dynamic Characteristics**[5] | | | | | | | |
| Input Capacitance | | $C_{iss}$ | $V_{DS}$ = -20V, $V_{GS}$ =0V, f =1MHz | - | 2525 | - | pF |
| Output Capacitance | | $C_{oss}$ | | - | 190 | - | |
| Reverse Transfer Capacitance | | $C_{rss}$ | | - | 172 | - | |
| Gate Resistance | | $R_g$ | f =1MHz | - | 10 | - | Ω |
| **Switching Characteristics**[5] | | | | | | | |
| Total Gate Charge | | $Q_g$ | $V_{GS}$ = -10V,$V_{DS}$ = -20V, $I_D$= -10A | - | 35 | - | nC |
| Gate-Source Charge | | $Q_{gs}$ | | - | 5.5 | - | |
| Gate-Drain Charge | | $Q_{gd}$ | | - | 8 | - | |
| Turn-On Delay Time | | $t_{d(on)}$ | $V_{GS}$ = -10V, $V_{DD}$ = -20V, $R_G$ = 3Ω, $I_D$= -10A | - | 14.5 | - | ns |
| Rise Time | | $t_r$ | | - | 20.2 | - | |
| Turn-Off Delay Time | | $t_{d(off)}$ | | - | 32 | - | |
| Fall Time | | $t_f$ | | - | 10 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Diode Forward Voltage[4] | | $V_{SD}$ | $I_S$ = -10A, $V_{GS}$ = 0V | - | - | -1.2 | V |
| Continuous Source Current | $T_C$=25°C | $I_S$ | - | - | - | -13 | A |

Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is $V_{DD}$= -25V, $V_{GS}$= -10V, L= 0.1mH, $I_{AS}$= -34A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

## Typical Characteristics

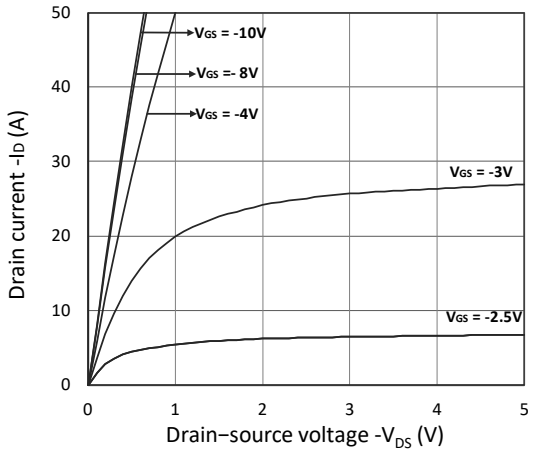



Figure 1. Output Characteristics

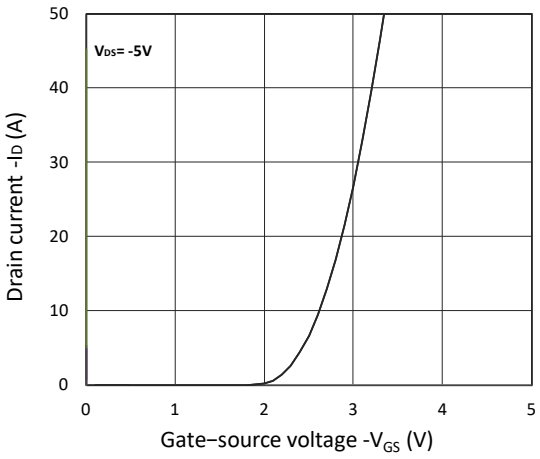



Figure 2. Transfer Characteristics

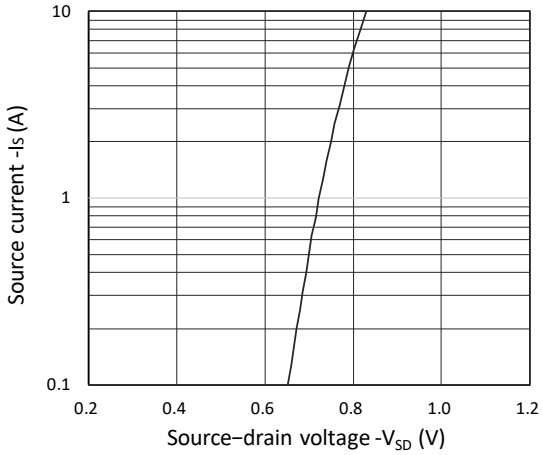



Figure 3. Forward Characteristics of Reverse

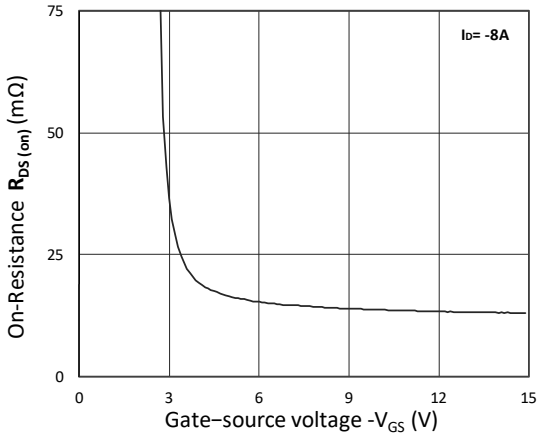



Figure 4. $R_{DS(ON)}$ vs. $V_{GS}$

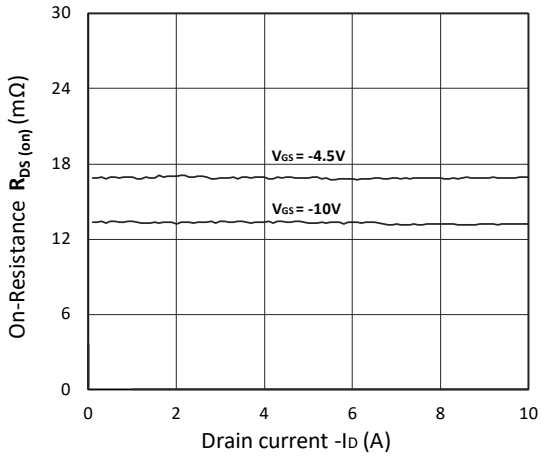



Figure 5. $R_{DS(ON)}$ vs. $I_D$

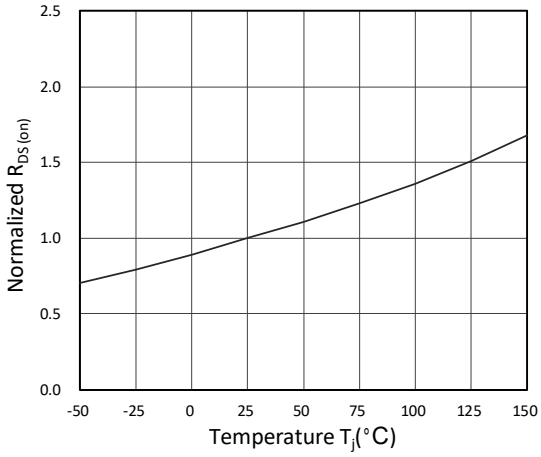



Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

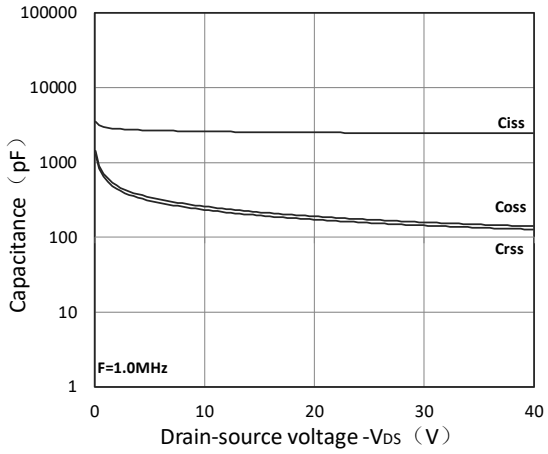



Figure 7. Capacitance Characteristics

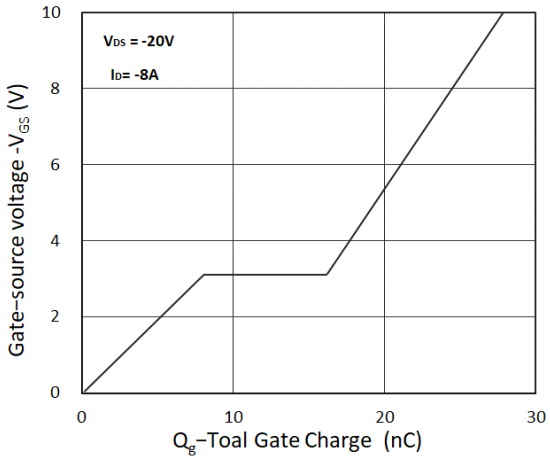



Figure 8. Gate Charge Characteristics

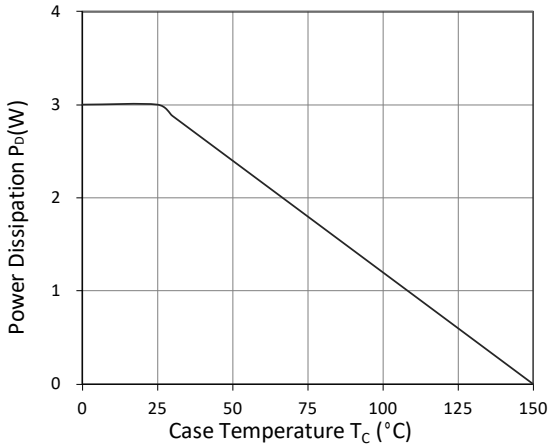



Figure 9. Power Dissipation

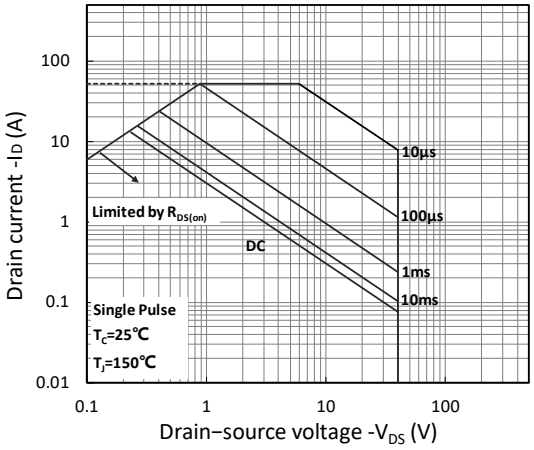



Figure10. Safe Operating Area

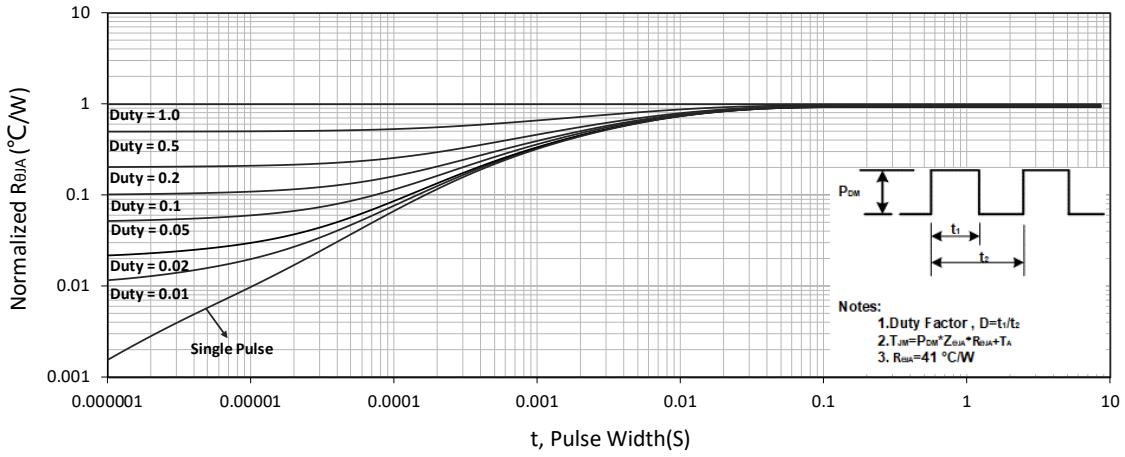



Figure 11. Normalized Maximum Transient Thermal Impedance

## Test Circuit

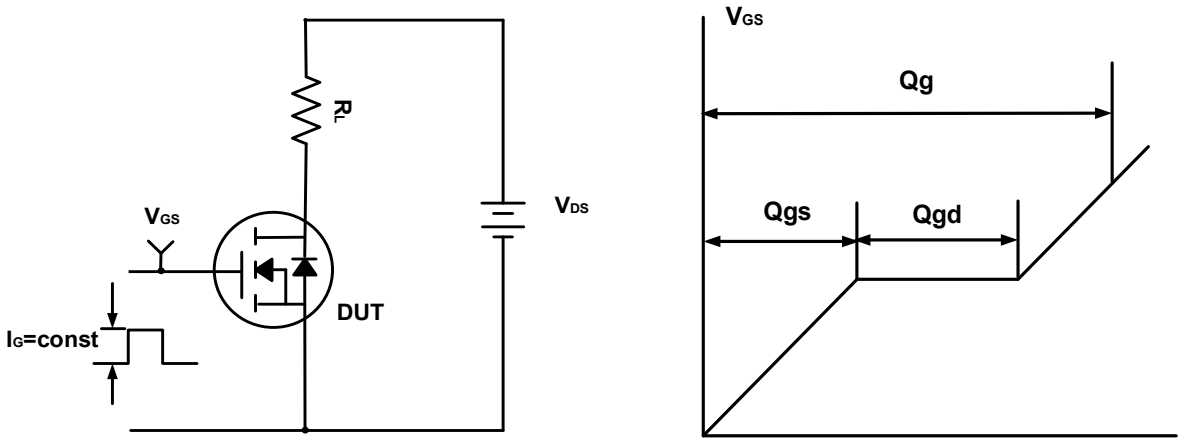



**Figure A. Gate Charge Test Circuit & Waveforms**

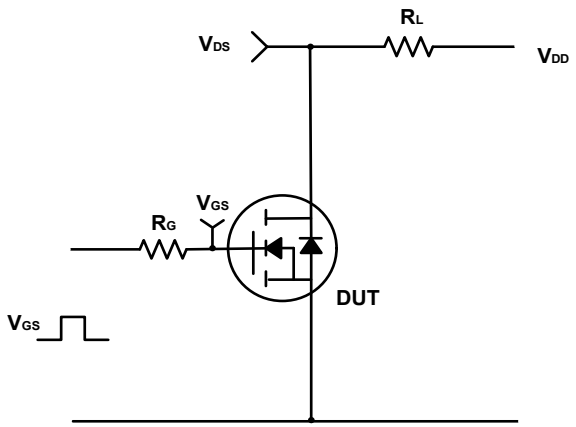



**Figure B. Switching Test Circuit & Waveforms**

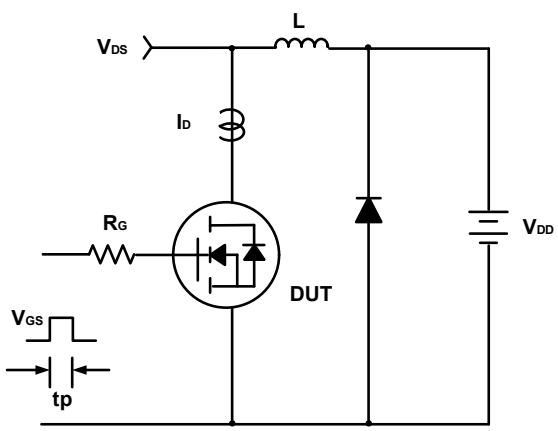
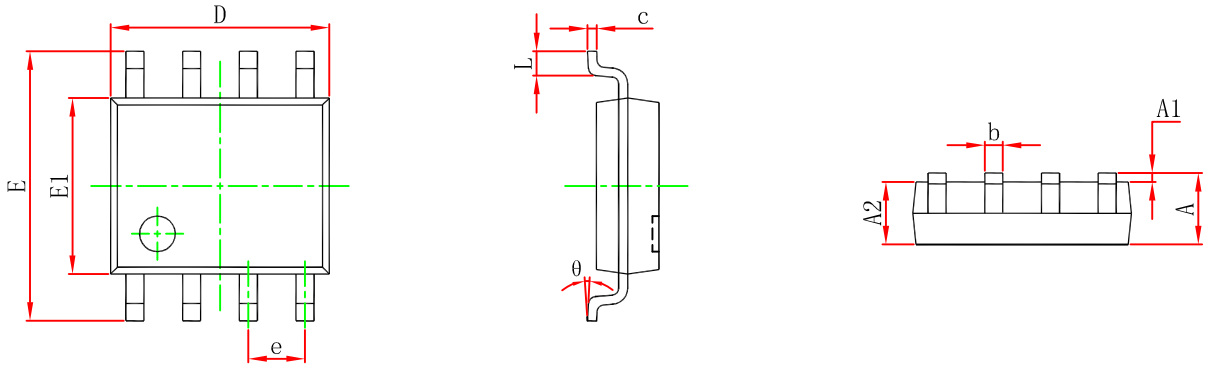
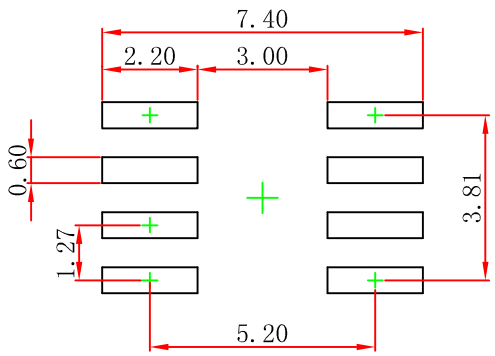



**Figure C. Unclamped Inductive Switching Circuit & Waveforms**

## SOP-8(SOIC-8) Package Outline Dimensions




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.800 | 5.000 | 0.189 | 0.197 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| E | 5.800 | 6.200 | 0.228 | 0.244 |
| E1 | 3.800 | 4.000 | 0.150 | 0.157 |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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