CHIPLINK P-Channel Enhancement Mode MOSFET

Description

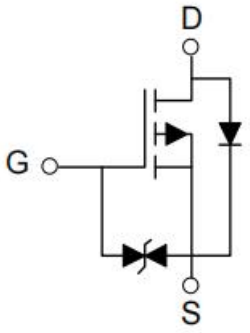
The LX3415KS uses advanced trench technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch applications.

Features

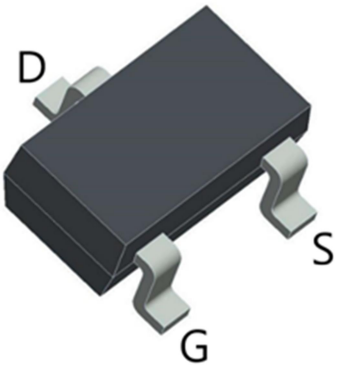
- V_{DS} = -20V, I_D = -4.1A
  $R_{DS(ON)typ}$ = 21mΩ@V_{GS} = -4.5V
  $R_{DS(ON)typ}$ = 27mΩ@V_{GS} = -2.5V
  ESD protected 2KV
- Low Gate Charge
- ESD Protection
- Termination is Lead-free and RoHS Compliant

Applications

- Battery Isolation
- Load Switch
- Electronic Cigarette



Schematic Diagram



SOT23 Package

Maximum Ratings

(T_A = 25℃, unless otherwise noted)

PARAMETER	SYMBOL	MAX	UNIT
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	-4.1	A
Pulsed Drain Current[C]	I_{DM}	-20	A
Maximum Power Dissipation[B]	P_D	0.88	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃

Thermal Characteristic

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance, Junction-to-Ambient[A]	$R_{\theta JA}$	280	℃/W

Electrical Characteristics

(T_A = 25℃, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D =-250μA	-20			V
Gate-Threshold Voltage	$V_{th(GS)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.4	-0.7	-1	V
Gate-body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±10V			±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	μA
Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -4.1A		21	32	mΩ
		V_{GS} = -2.5V, I_D = -3A		27	41	mΩ
Forward Transconductance	g_{FS}	V_{DS} = -5V, I_D = -2A		20		s
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS} = -10V, V_{GS} = 0V, F = 1MHz		922		pF
Output Capacitance	C_{oss}			88		
Reverse Transfer Capacitance	C_{rss}			76		
Switching Capacitance						
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -10V, V_{GS} =- 4.5V, R_L = 2.22Ω, R_G = 3Ω		13		ns
Turn-On Rise Time	t_r			10		ns
Turn-Off Delay Time	$t_{d(off)}$			78		ns
Turn-Off Fall Time	t_f			32		ns
Total Gate Charge	Q_g	V_{DS} = -10V, I_D = -4A, V_{GS} = -4.5V		11.5		nC
Gate-Source Charge	Q_{gs}			1.3		nC
Gate-Drain Charge	Q_{gd}			2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = -1A			-1	V

Notes:

A. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25℃. The value in any given application depends on the user's specific board design.

B. The power dissipation PD is based on $T_{J(MAX)}$ = 150℃, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 150℃. Ratings are based on low frequency and duty cycles to keep initial TJ = 25℃.

D. The static characteristics in Figures 1 to 6 are obtained using < 300μs pulses, duty cycle 0.5% max.

E. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$ = 150℃. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

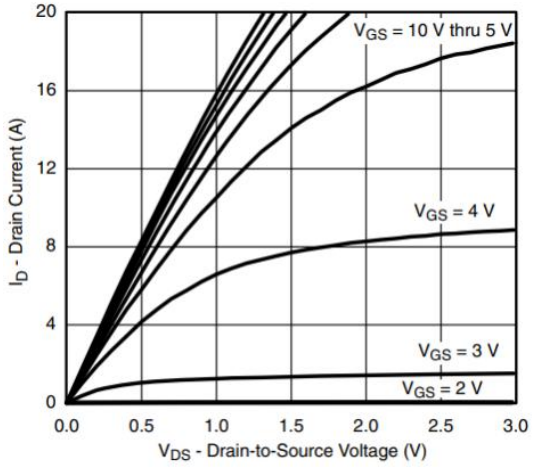


Figure 1. On-Region Characteristics

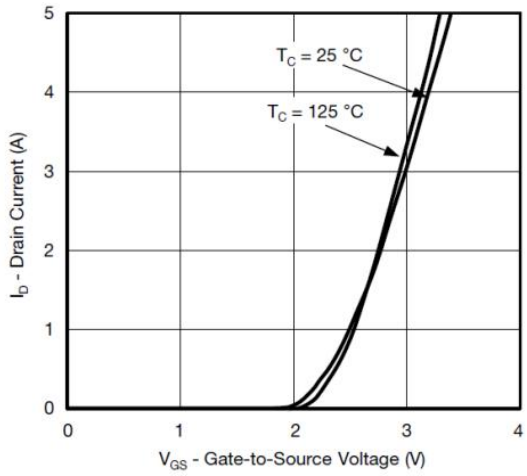


Figure 2. Transfer Characteristics

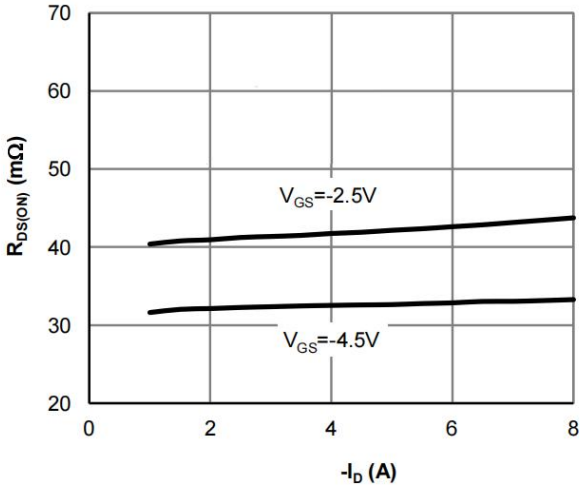


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

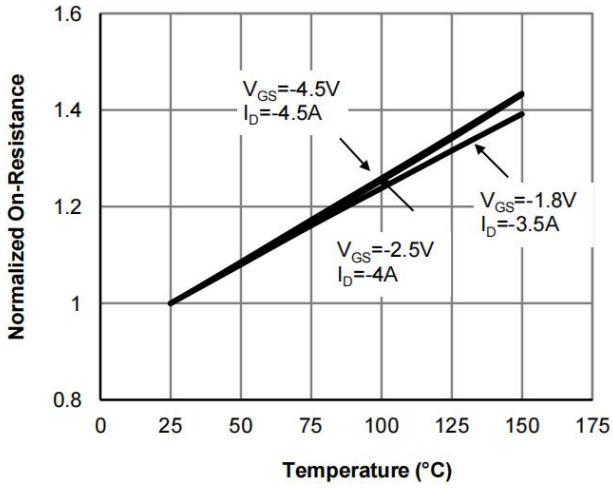


Figure 4. On-Resistance vs. Junction Temperature

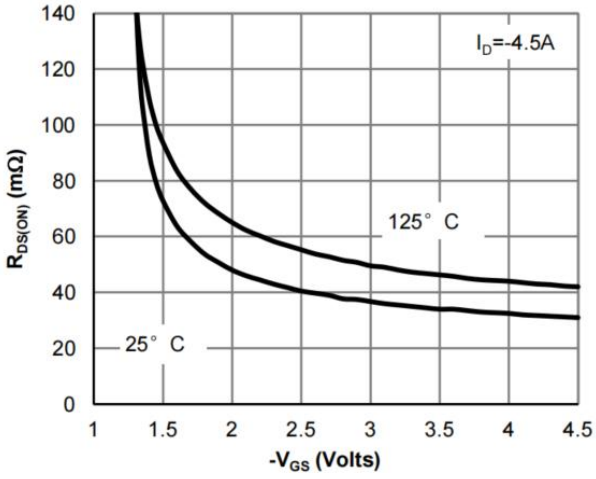


Figure 5. On-Resistance vs. Gate-Source Voltage

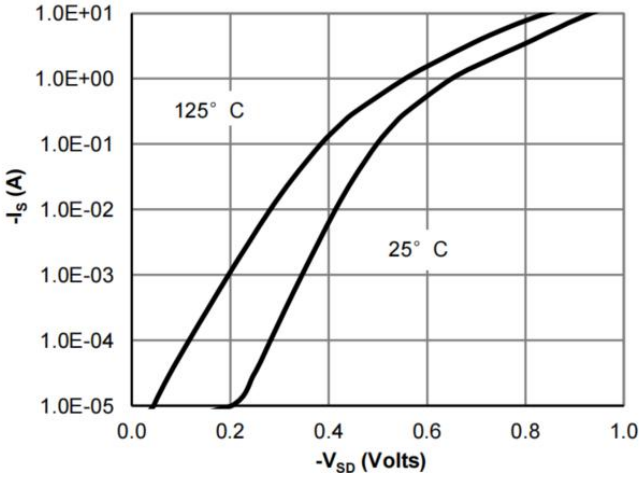


Figure 6. Body-Diode Characteristics

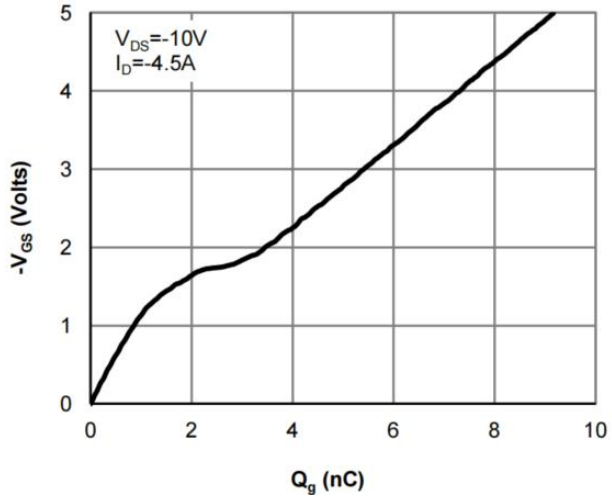


Figure 7. Gate-Charge Characteristics

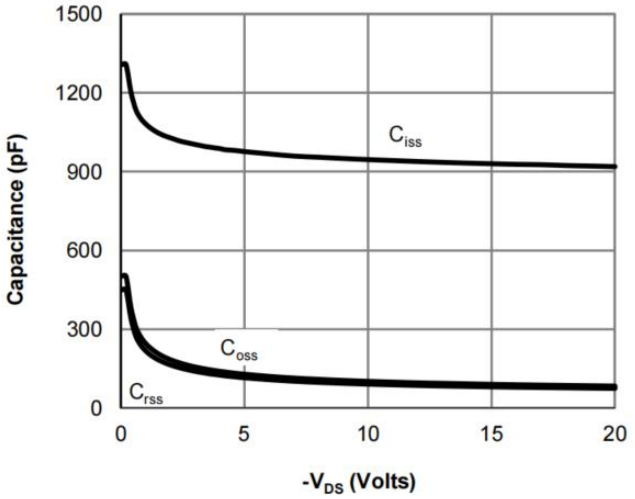


Figure 8. Capacitance Characteristics

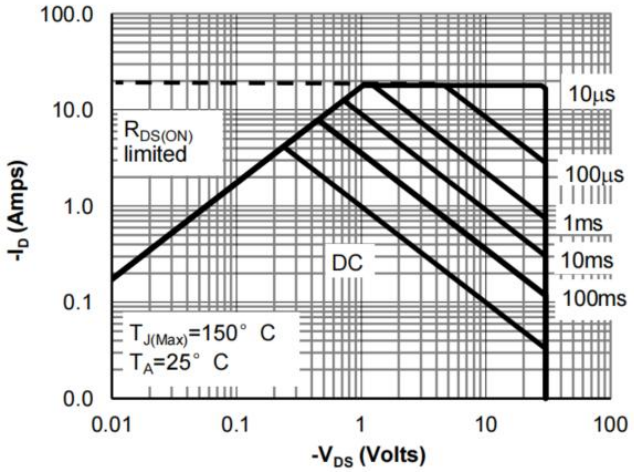


Figure 9. Maximum Forward Biased Safe Operating Area

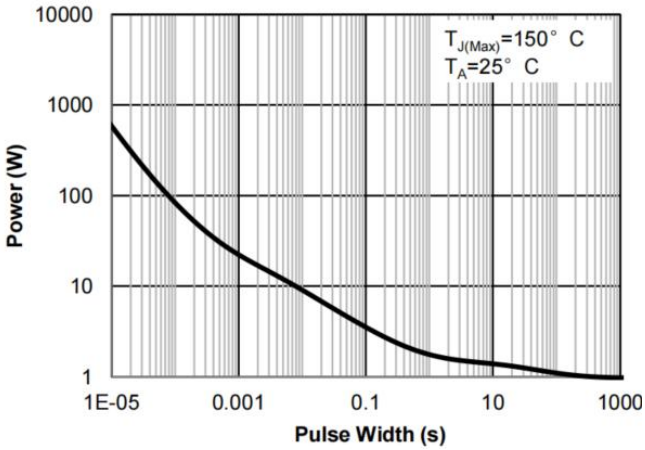


Figure 10. Single Pulse Power Rating Junction-to-Ambient

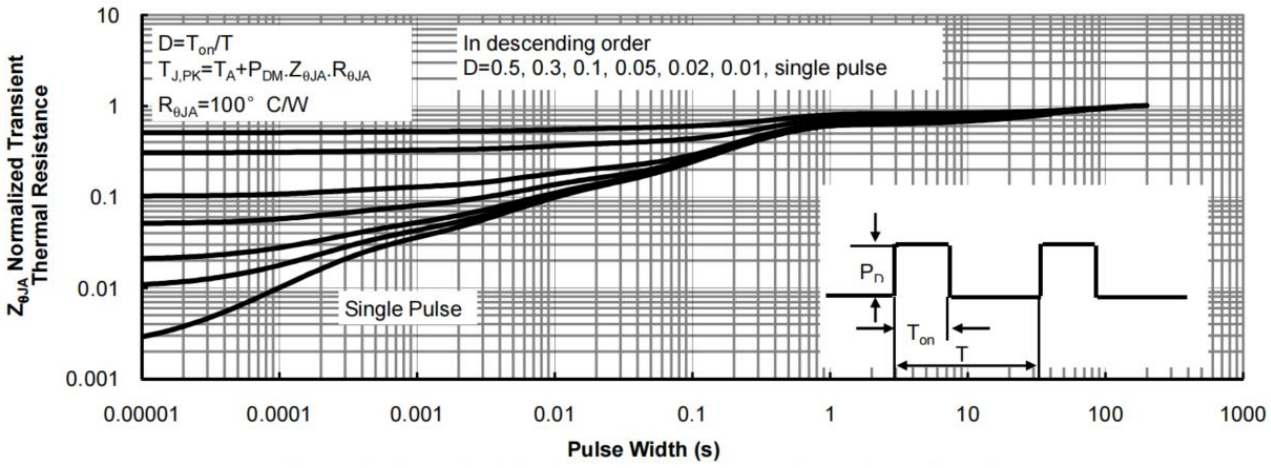


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit and Waveform

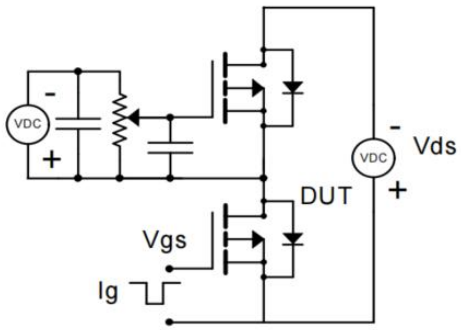


Figure 12. Gate Charge Test Circuit

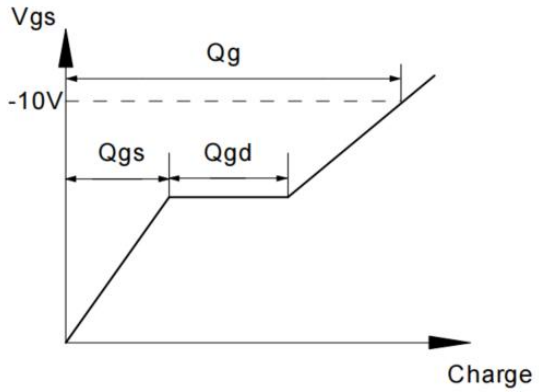


Figure 13. Gate Charge Waveform

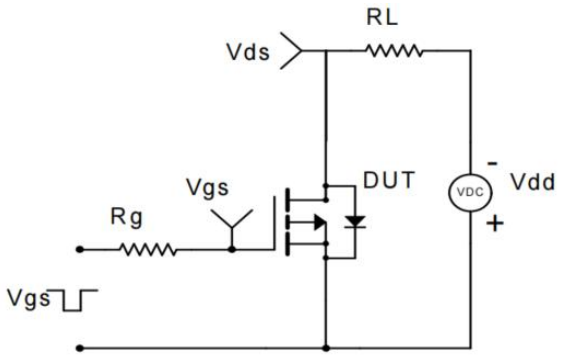


Figure 14. Resistive Switching Test Circuit

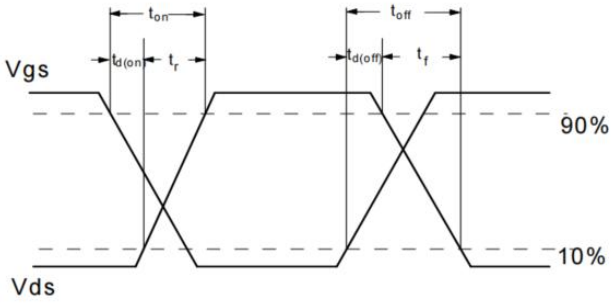


Figure 15. Resistive Switching Waveforms

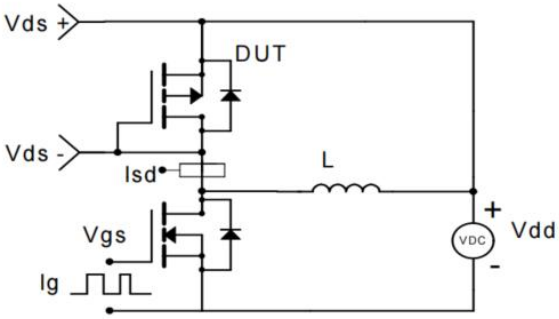


Figure 16. Diode Recovery Test Circuit

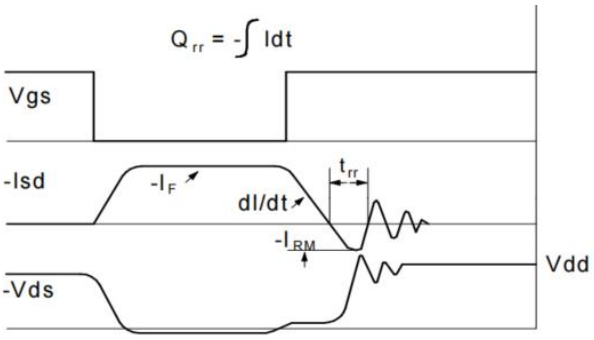
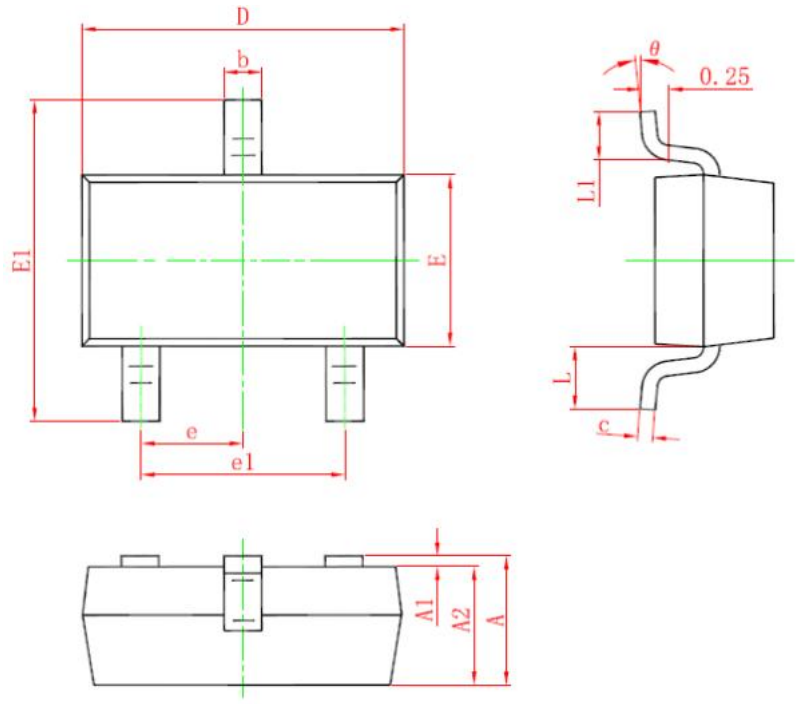


Figure 17. Diode Recovery Waveforms

SOT-23 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITIAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED.

CHIPLINK DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS.

THIS DOCUMENT SUPERSEDES AND REPLACES ALL INFORMATION PREVIOUSLY SUPPLIED.

CHIPLINK RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.