OB5686A

HV Start Up, High PF, Low THD CV Controller

GENERAL DESCRIPTION

OB5686A is a flyback and buck controller with high power factor, low THD and high constant voltage (CV) precision. It can achieve low system cost for isolated and non-isolated applications.

The proprietary CV control scheme is used and the system can achieve high power factor with constant on-time control scheme. Quasi-resonant (QR) operation and clamping frequency greatly improves the system efficiency. The advanced high voltage start-up technology is used to meet the fast start-up time and low standby power requirements.

OB5686A offers comprehensive protection including line over voltage and line brownout protection, open circuit protection, short circuit protection, over load protection, cycle-by-cycle current limiting, built-in leading edge blanking, VDD under voltage lockout (UVLO), etc.

OB5686A is offered in SOP8 package.

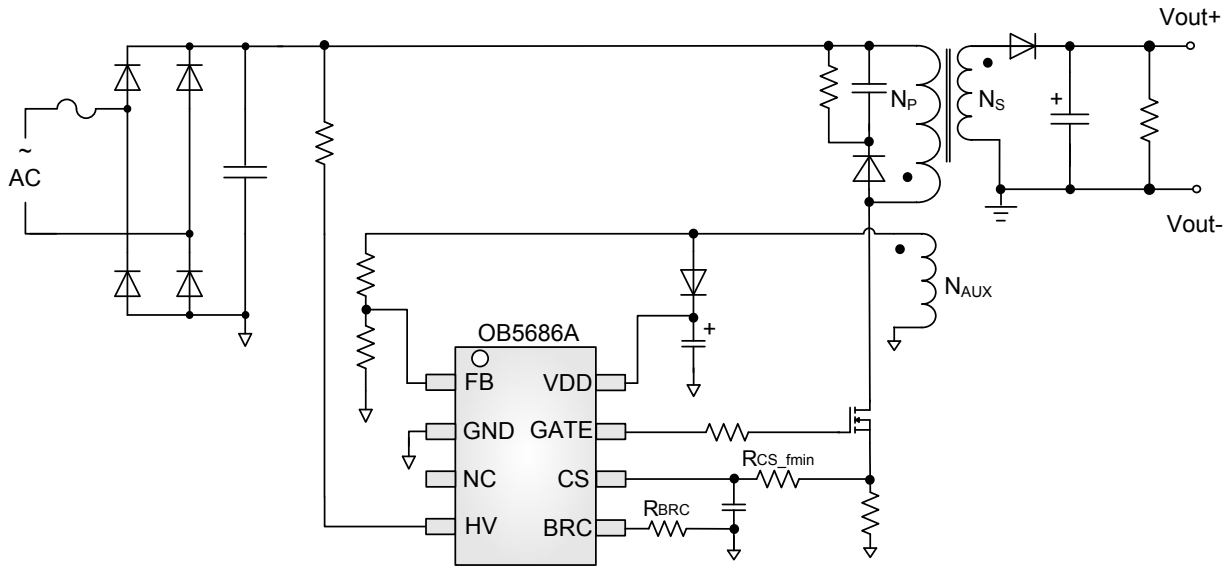
FEATURES

- High precision constant voltage regulation
- High PF and low THD
- HV start-up
- Low Standby Power
- ±5%/±15% fast dynamic response adaptively
- Externally configurable minimum frequency
- Low system cost and high efficiency
- Quasi-resonant operation
- Externally configurable line brownout protection
- Externally configurable line over voltage protection
- Output short circuit protection
- Output open circuit protection
- Cycle-by-cycle current limiting
- Built-in leading edge blanking (LEB)
- VDD under voltage lockout with hysteresis (UVLO)
- VDD over voltage protection
- Over temperature protection (OTP)
- Over load protection (OLP)
- Audio Noise Free
- Low Standby Power

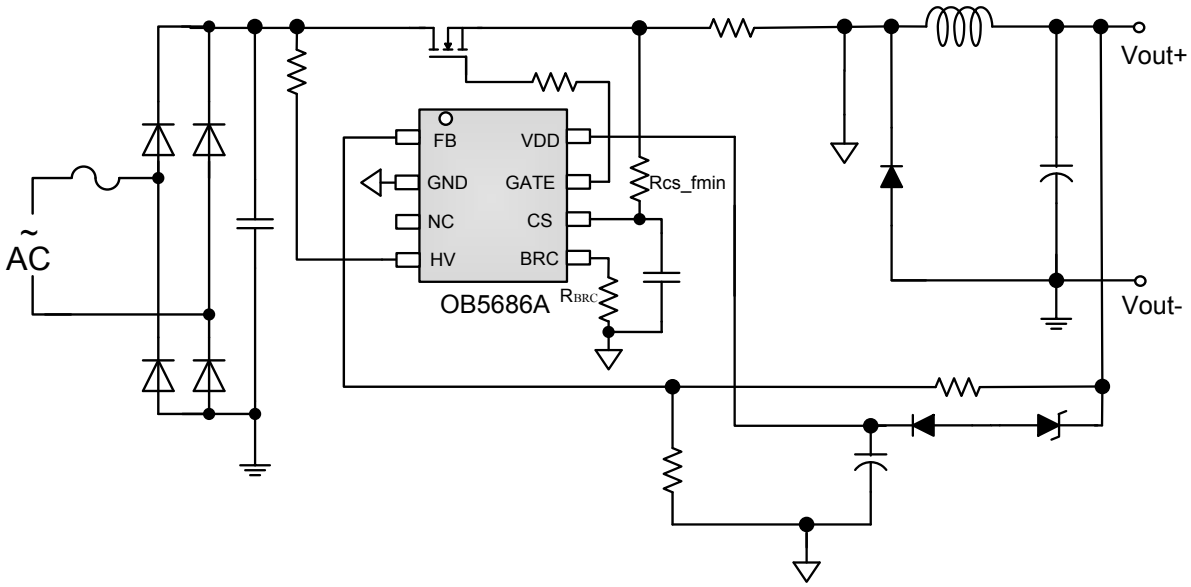
APPLICATIONS

- Smart LED lighting
- Motor drive power supply

FLYBACK TYPICAL APPLICATION



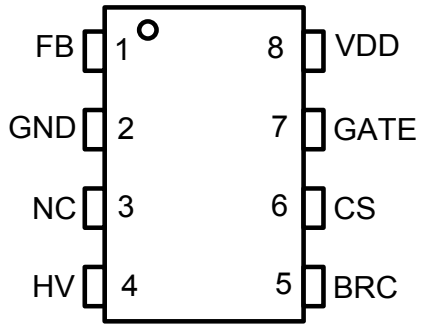
BUCK TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map is shown as below for SOP8.



Ordering Information

Part Number	Description
OB5686ACP	SOP8,Halogen-free in Tube
OB5686ACPA	SOP8,Halogen-free in T&R

Note: All Devices are offered in Halogen-free Package if not otherwise noted.

Package Dissipation Rating

Package	RθJA (℃/W)
SOP8	90

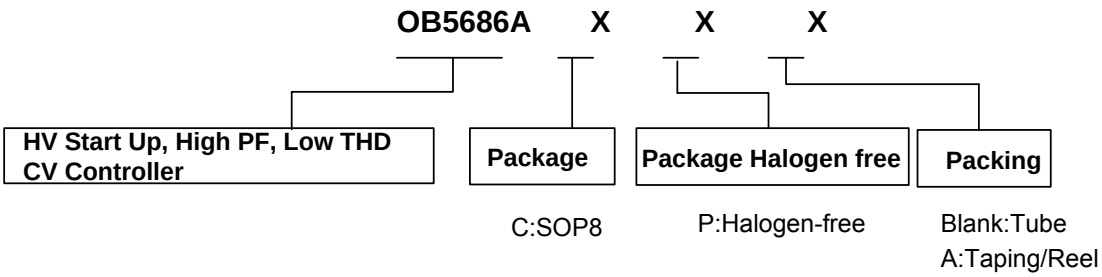
Absolute Maximum Ratings

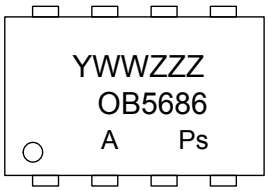
Parameter	Value
HV Voltage	-0.3 to 700 V
VDD Voltage	-0.3 to 40V
GATE Voltage	-0.3 to 40V
CS Input Voltage	-0.3 to 7V
BRC Input Voltage	-0.3 to 7V
FB Input Voltage[2]	-1 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Operating Ambient Temperature T_A	-20 to 85 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Note2: The negative voltage amplitude is relaxed to -1V under the condition that its max negative current is in less than 10mA.

Marking Information



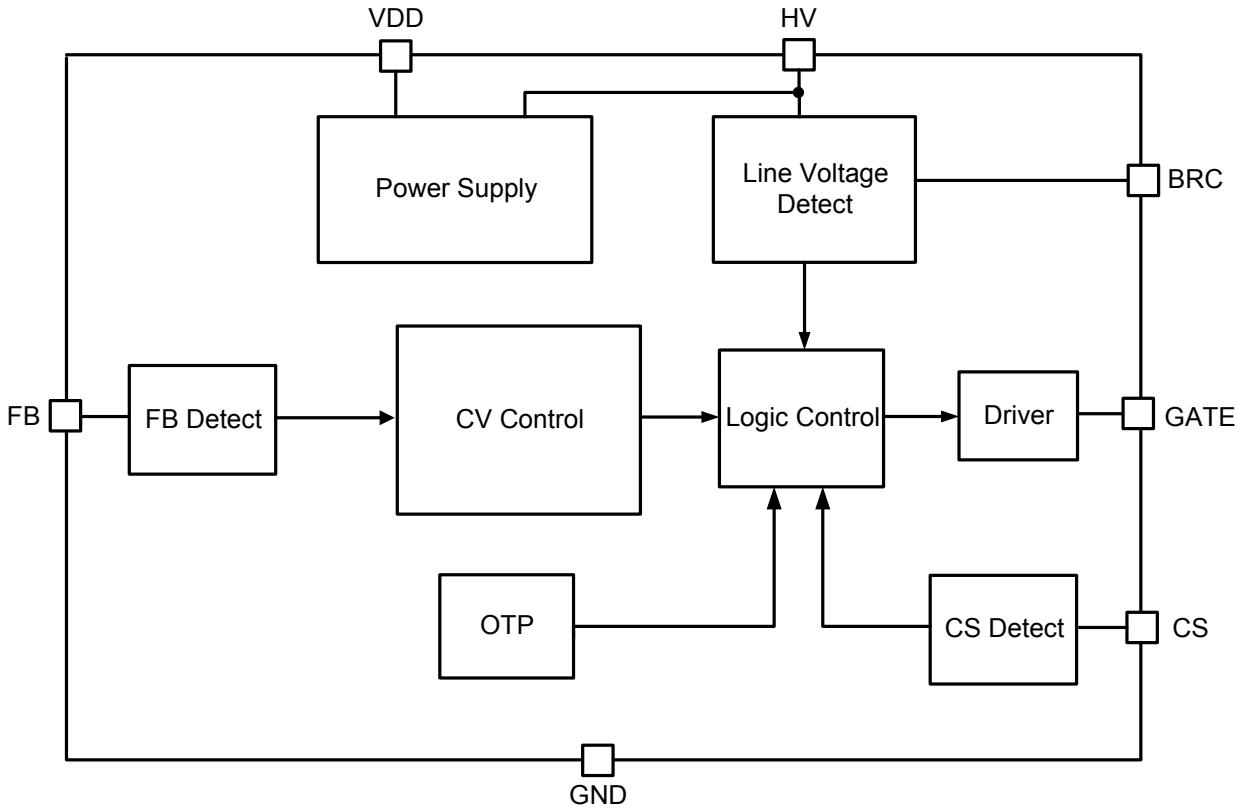


Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
P:Halogen-free Package
S:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	FB	I	Output voltage feedback.
2	GND	P	Power ground.
3	NC		No connection
4	HV	P	High voltage power supply
5	BRC	I/O	Line brownout setting
6	CS	I	Current sense input pin.
7	GATE	O	Gate driver output for power MOSFET.
8	VDD	P	Power supply.

BLOCK DIAGRAM

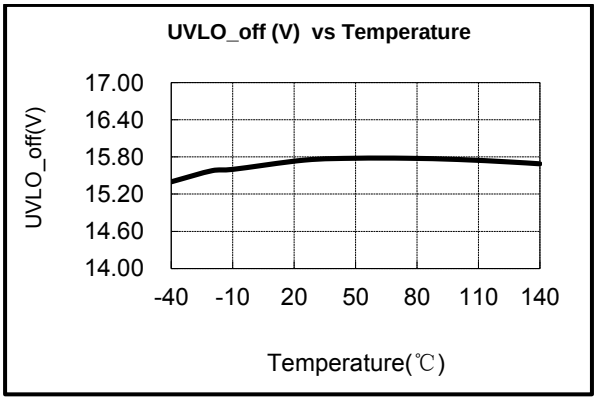


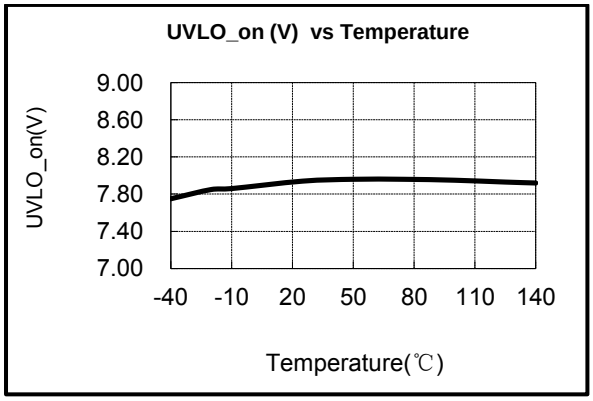
ELECTRICAL CHARACTERISTICS

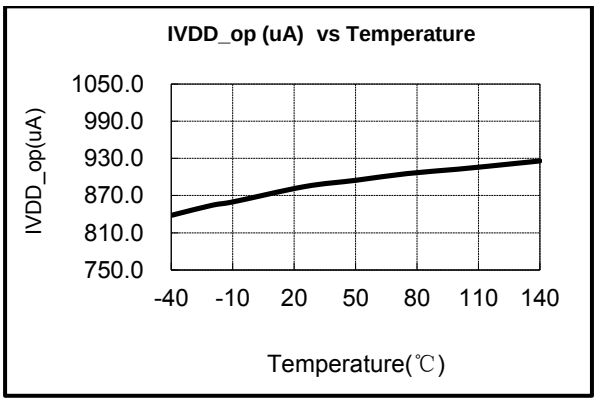
(TA = 25℃, VDD=20V, if not otherwise noted)

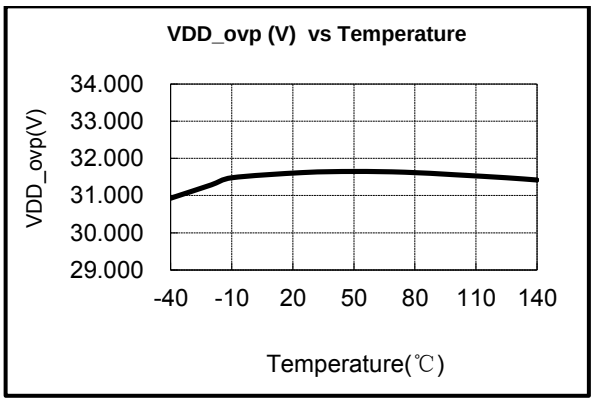
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section						
IVDD_op	Static current	VDD=20V		850		uA
UVLO_off	VDD under voltage Lockout Exit	VDD rising		16.2		V
UVLO_on	VDD under voltage Lockout Enter	VDD falling		8		V
VDD_ovp	VDD overvoltage protection			32		V
FB Detect Section						
Vth_ovp	Output overvoltage protection			3.2		V
Vth _scp	Output short protection			0.4		V
CS Detect Section						
TLEB	Leading Edge Blanking time			420		ns
Vth_ocp	Over current threshold voltage	Ton=0us		0.6		V
CV Control Section						
Vref	Error Amplifier Reference Voltage		2.45	2.5	2.55	V
Fmax	Maximum Frequency			120		KHz
Toff_min	Minimum off time			2		us
Toff_max	Maximum off time			110		us
Ton_max	Maximum on time			20		us
Fmin	Minimum frequency	Rcs_fmin＞2.5kohm		500		Hz
		Rcs_fmin＜1kohm		500		Hz
		Rcs_fmin 1k~2.5kohm		1k		Hz
Line Detect Section						
Line_ovp_startup	Line over voltage protection @ startup			311		Vac
Line_ovp_normal	Line over voltage protection @ normal operation			323		Vac
Line _brownout	Brown-out	R_{BRC}=GND		140		Vac
	Brown-in			154		Vac
	Brown-out	R_{BRC} Floating		71		Vac
	Brown-in			83		Vac
OTP section						
OTP	Over temperature protection			150		℃
Gate Drive Section						
Vclamp	Gate output clamping voltage			12		V
Tr	Rising edge time	CL=1nF		80		ns
Tf	Falling edge time	CL=1nF		30		ns

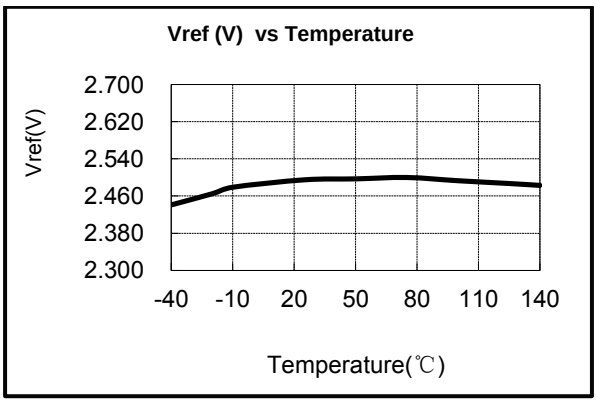
CHARACTERIZATION PLOTS

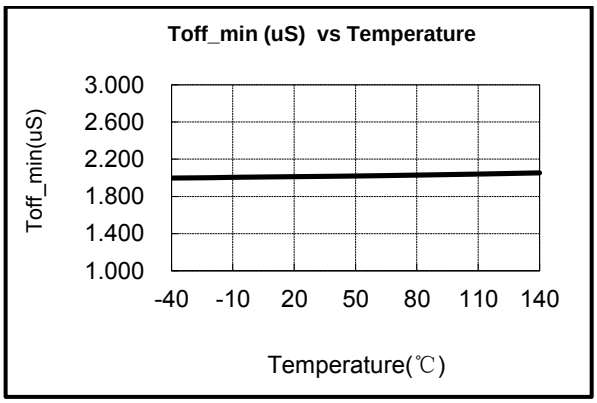


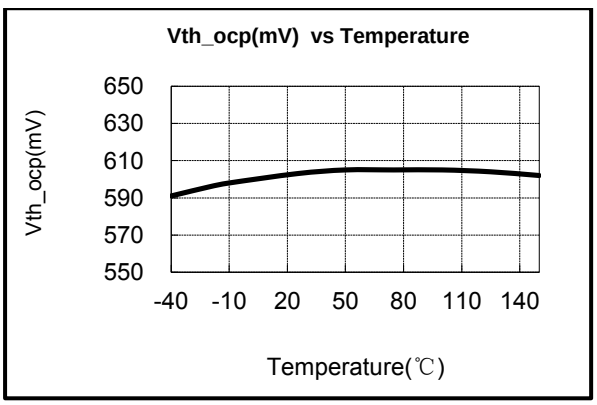












OPERATION DESCRIPTION

OB5686A is a flyback and buck controller with HV startup high power factor, low THD and high constant voltage (CV) precision. It can achieve low system cost for isolated and non-isolated applications.

Startup

OB5686A integrates HV startup circuit. During power on state, it provides about 1mA current to charge the capacitor connecting between VDD and ground from HV pin. When the VDD voltage is higher than UVLO_off, the charge current is switched off. At this moment, the VDD capacitor provides current to OB5686A until the auxiliary winding of the main transformer starts to supply the operation current.
In general application, a 20KΩ(typical) resistor is recommended to be placed in the high voltage path to limit the current.

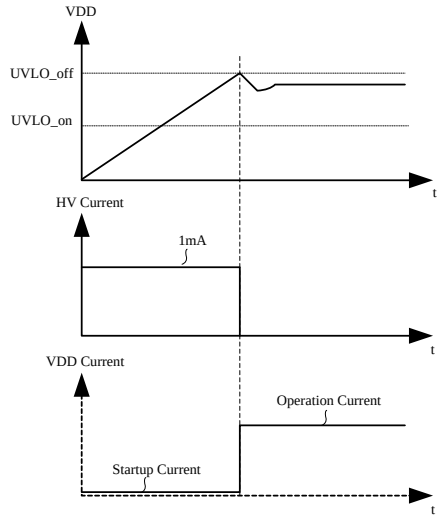


Figure.1 Startup Current Timing

During startup, OB5686A detects the line voltage. If the line voltage is lower than preset brownout voltage for 20mS or is higher than 311Vac, the power MOSFET will not be allowed to turn on. If BRC pin floating, line brownout and line OVP will be disabled. If the line voltage is detected in normal range, OB5686A will operate at open loop and over-current protection is set cycle-by-cycle until it senses the output voltage by FB pin up to about 0.4V.

Output voltage regulation

In flyback application, in order to achieve primary side constant voltage control, the output voltage is detected through the auxiliary winding voltage. During OFF time, the voltage across the auxiliary winding is:

$$V_A = (V_{OUT} + V_{DF})\frac{N_A}{N_S}$$

N_S is the turns of secondary winding
V_{DF} is the forward voltage of the power diode
N_A is the turns of auxiliary winding
At the current zero-crossing point, V_{DF} is nearly zero, so V_{OUT} is proportional with V_A exactly. The FB voltage of this point is sampled as the feedback of output voltage. The resistor of voltage divider is designed by:

$$V_{OUT} = \frac{V_{ref}}{\frac{N_A}{N_S}\frac{R_2}{R_1 + R_2}}$$

V_{ref} is the internal voltage reference
R_1 is high side resistance of voltage divider
R_2 is low side resistance of voltage divider

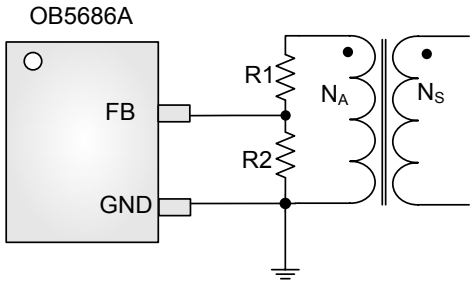


Figure.2 Flyback FB Section Circuit

In buck application, in order to achieve constant voltage control, the output voltage is detected by the buck inductor voltage.
The resistor divider is designed by:

$$V_{OUT} = \frac{V_{ref}}{\frac{R_4}{R_3 + R_4}}$$

V_{ref} is the internal voltage reference
R_3 is high side resistance of voltage divider
R_4 is low side resistance of voltage divider

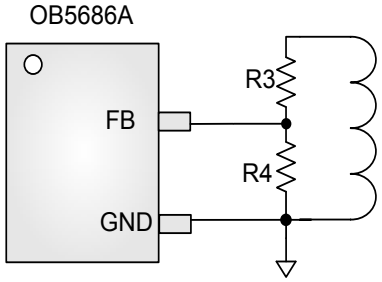


Figure.3 Buck FB Section Circuit

Adaptively adjust dynamic response

When the output load changes from heavy load to light load, the FB voltage will be detected higher than VFB_H, OB5686A is forced into Fmin mode

operation for fast response to reduce the output energy. When the FB voltage returns to VFB_R, OB5686A works in normal operation. When the output load changes from light load to heavy load, the FB voltage will be detected lower than VFB_L, OB5686A works in OCP mode for fast response to ensure sufficient energy supply to the output. When the FB voltage returns to VFB_R, OB5686A works in normal operation .

OB5686A is offered fast dynamic response, the dynamic thresholds VFB_H and VFB_L is adjusted adaptively according to the ripple of the output voltage. So OB5686A can internally select different dynamic thresholds for different output capacitors. Also the dynamic threshold can be forced to ±5% by placing a 2.5kohm Rcs_fmin resistance.

The threshold of VFB as shown in table:

Dynamic	VFB_H	VFB_R
+5%	2.625V	2.55V
+15%	2.875V	2.55V
	VFB_L	**VFB_R**
-5%	2.375V	2.44V
-15%	2.125V	2.44V

PF and THD

The duration of the turn on period ton is generated and keeps constant by a patented control method. Constant on time and quasi-resonant operation provide high power factor (PF) and low total harmonic distortion (THD).

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting (OCP) is offered in OB5686A. The switching current is detected through the sense resistor between the CS pin and GND. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery. The current limit comparator is disabled during this blanking time and thus the external MOSFET is not closed during this period.

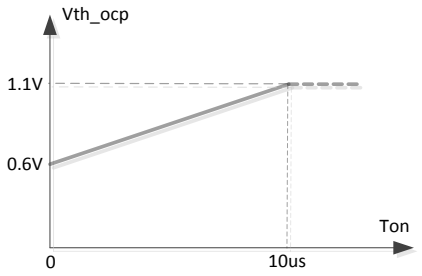


Figure.4 OCP and Ton Curve

Quasi-Resonant Operation

OB5686A performs quasi-resonant detection through FB pin by monitoring the output voltage. FB voltage drops when the energy stored in transformer or inductance is released to the output. When FB pin voltage falls below 0V (typical), an internal FB comparator is triggered and a new PWM switching cycle is initiated after the FB trigger.

Gate Drive Output

The output stage is designed to ensure zero cross-conduction current, which minimizes heat dissipation, improves efficiency, and enhances reliability. The built-in 12V clamp at the gate output protects the MOSFET gate from high voltage stress.

Protection Controls

OB5686A ensures good reliability design through its good protection coverage. Output over voltage protection (OVP), Over Load Protection (OLP), VDD under voltage lockout (UVLO), VDD over voltage protection (VDD OVP), brown-out protection, cycle-by-cycle current limiting, output short circuit protection, output open circuit protection, over temperature protection, line over voltage protection, diode short protection and output gate clamp are standard features provided by OB5686A.

Short Circuit Protection

When output is shorted, the FB voltage is low. If the voltage at FB pin falls below a threshold of approximately 0.4 V (typical), the OCP threshold voltage is reduced to 0.4 V (typical). In this way, the power dissipation is greatly reduced. OB5686A shuts down during SCP protection, after 0.5S (typical) VDD drops below UVLO_on and the OB5686A will be reset.

Open Circuit Protection

When an open circuit happens, the FB pin voltage is high. If the FB pin voltage is higher than a threshold of approximately 3.2V (typical), the IC will shut down and enter power on startup sequence thereafter. The OB5686A shuts down during OCP protection, after 0.5S (typical) VDD drops below UVLO_on and the OB5686A will be reset.

Over Load Protection

OB5686A detects output power and offers over load protection (OLP). If output power exceeds the power limit threshold (about 1.3 times of full load), the control circuit reacts by turning off the power MOSFET. The OB5686A shuts down during OLP protection, after 0.5S (typical) VDD drops below UVLO_on and the OB5686A will be reset.

Over Temperature Protection

Over temperature protection is offered in OB5686A. When temperature of the device rises above 150℃ (typical), the IC will shut down. And the state will remain until the device is restarted.

Line Brownout

Line brownout voltage is set by the BRC pin. When the detected voltage from the BRC reaches the threshold, the line brownout voltage is set before startup. The OB5686A shuts down during line brownout, after 0.5S (typical) VDD drops below UVLO_on and the OB5686A will be reset. If the BRC pin connecting to GND with 10Kohm resistor, line brownout function will be disabled.

The connecting of the BRC pin as shown in table:

BRC pin	Line Brownout Voltage
Connecting to GND	140Vac
Connecting to GND with 10Kohm resistor	No Brownout
Floating	71Vac

Line Over Voltage Protection

OB5686A provides line over voltage protection to prevent IC from working in high voltage stress. OB5686A detects line voltage and compares with inner threshold voltage. When line voltage reaches 323Vac, the over voltage protection function is activated and the switching is turned off, after 0.5S (typical) VDD drops below UVLO_on and the OB5686A will be reset.

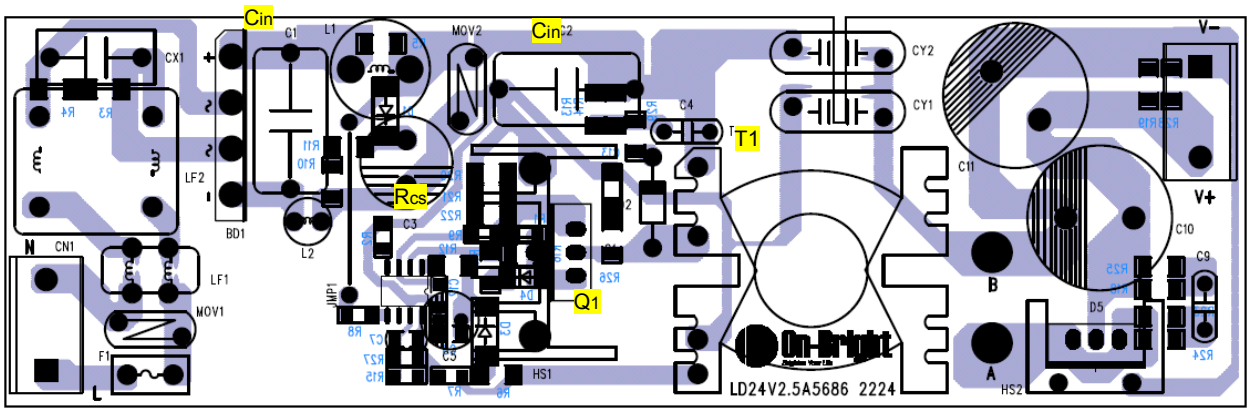
If the BRC pin connecting to GND with 10Kohm resistor, line over voltage protecting function will be disable.

BRC pin	Line OVP Voltage
Connecting to GND	323Vac
Connecting to GND with 10Kohm resistor	No Line OVP
Floating	323Vac

Layout Consideration

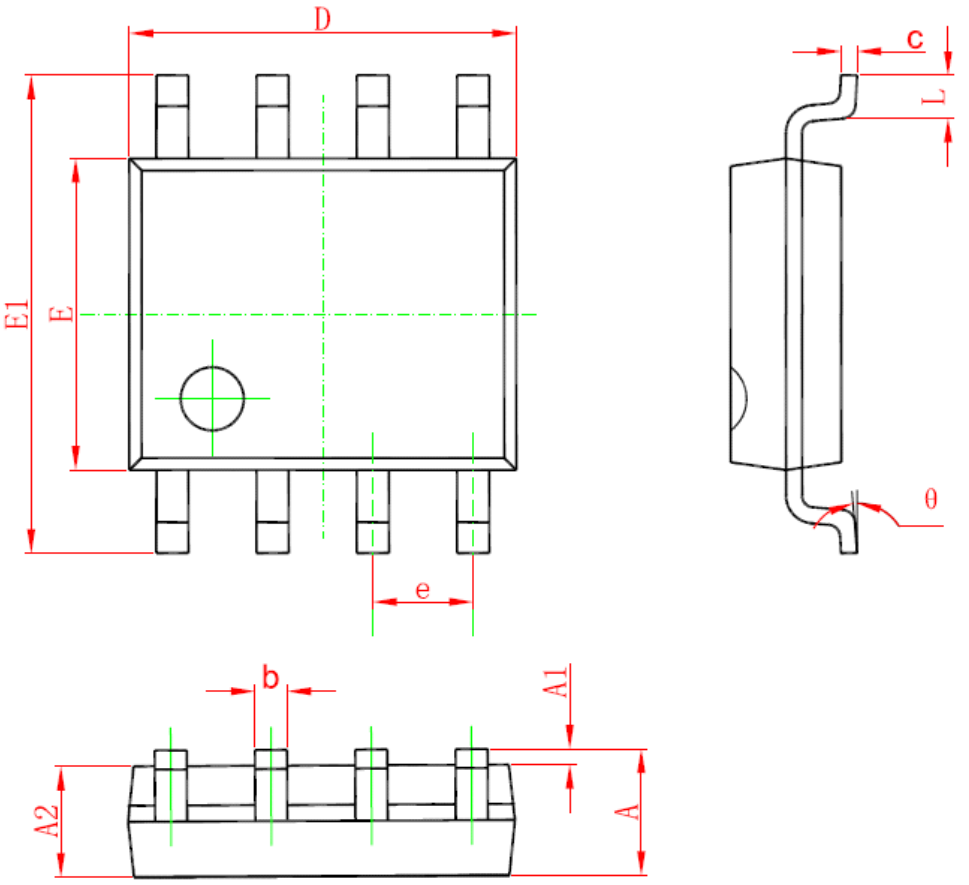
Careful attention must be paid to the PCB board layout and components placement. Proper layout of the high frequency switching path is critical to prevent noise and electromagnetic interference problems. Using the following guidelines for good PCB layout:

1) The loop of Cin→T1→Q1→ Rcs→GND and Gate→Q1→Rcs→GND is flowing with high frequency pulse current. They must be as short as possible to decrease noise coupling and kept a space to other low coltage traces,such as IC control circuit paths ,especially；Besides, the path between CS resistor ground and IC ground is recommended to be as short as possible, too.
2) The loop from the input capacitor to VDD pin is a high voltage loop. Keep a space from the loop to other low voltage traces.
3) It is good for reducing noise, output ripple and EMI issue to separate ground traces of the input capacitor, auxiliary winding and IC control circuit. Finally, connect them together at the input capacitor ground. The areas of these ground traces should be kept large.
4) Ground of IC peripheral devices should be connected to the IC ground. The ground of CS resistor should be connected with the IC ground first, then tied together at negative pole of the input capacitor .
   The ground of CS capacitor should be connected the IC ground or input capacitor with a single-point junction .
5) To reduce the parasitic trace inductance and EMI, the area of the loop connecting to the secondary winding, the output diode, and the output filter capacitor must be minimized. In addition, the sufficient copper area at the anode and cathode terminal of the output diode can help for heat-sinking. It is recommended to apply the larger area at the quiescent cathode terminal. The large anode area will induce high-frequency radiated EMI.



PACKAGE MECHANICAL DATA

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.700	4.100	0.146	0.161
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

IMPORTANT NOTICE

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