LP4030H

Standalone 1-4 Cell 3A Battery Charger

Features

- Easy-to-use standalone 1-to-4 cell charger
- High input voltage switching charger
  - Support 4.5V to 20V input voltage with 28V absolute maximum input rating
  - 3.0A maximum fast charge current
  - Trickle charge current: 10% of fast charge current
  - Termination current: 10% of fast charge current
  - Up to 92% efficiency
  - Input dynamic power management for various input source capacity
- High integration
  - Integrated reverse blocking and synchronous switching MOSFET
  - Charge current sensing
  - Internal loop compensation
  - Internal bootstrap diode
  - Charge operation indication driver
- Support full charge cycle of trickle charge, constant current charge and constant voltage charge, charge termination and recharge
- Protections
  - Input under-voltage lockout (UVLO)
  - Over-voltage protection (OVP)
  - Cold/hot battery temperature protection
  - Thermal shutdown protection
  - Cycle-by-cycle current-limit protection

General Description

The LP4030H family is highly integrated switching charger for 1-4 cells of Li-Ion and Li-Polymer batteries. The devices support 4.5V to 20V operation input voltage and charge current is up to 3A. The BAT pin withstands a voltage up to 28V, which is designed for protecting the devices from an over-shoot voltage in battery application systems.

The devices provide various safety features for battery charging, including battery under/over temperature protection, device junction over temperature and cycle-by-cycle inductor current limit protection. The input voltage regulation loop reduces charge current when the input source capacity is not enough to provide the programmed charge current. The STAT output indicates the charging status.

The LP4030H family is available in a DFN-10(3x3mm) package.

Applications

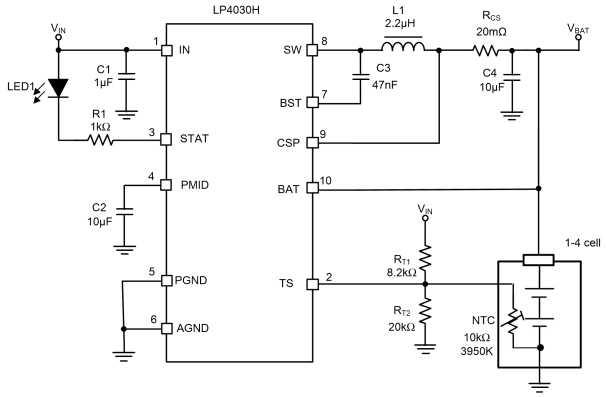
- Wireless Speaker
- Cordless Power Tools
- Gaming Devices
- Portable Media Players
- Handheld Battery-Powered Devices
- Charging Docks and Cradles
- Toys
- E-Cigarettes

Order Information

LP4030H □ □□ □ □□□

- Battery Voltage
  - Default: 4.20V
  - 435: 4.35V
  - 44: 4.40V
- F: Pb-Free
- Package Type
  - QV: DFN-10
- Battery cells
  - A: 1 cell
  - B: 2 cell
  - C: 3 cell
  - D: 4 cell

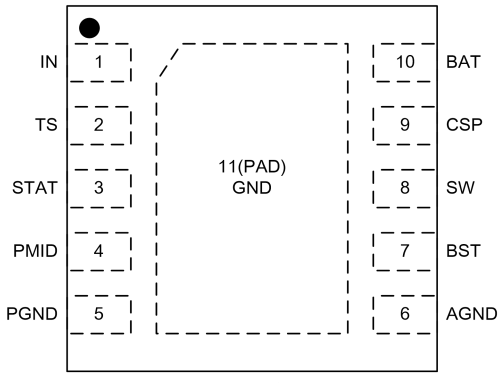
Typical Application Circuit



Device Information

Part Number	Top Marking	Battery Cells / Voltage	Package	Shipping
LP4030HAQVF	LPS LP4030HA YWX	1 Cell 4.2V / cell	DFN-10	5K/REEL
LP4030HAQVF-435	LPS LP4030HA 435YWX	1 Cell 4.35V / cell	DFN-10	5K/REEL
LP4030HAQVF-44	LPS LP4030HA 44YWX	1 Cell 4.4V / cell	DFN-10	5K/REEL
LP4030HBQVF	LPS LP4030HB YWX	2 Cell 4.2V / cell	DFN-10	5K/REEL
LP4030HCQVF	LPS LP4030HC YWX	3 Cell 4.2V / cell	DFN-10	5K/REEL
LP4030HDQVF	LPS LP4030HD YWX	4 Cell 4.2V / cell	DFN-10	5K/REEL
LP4030HBQVF-87	LPS LP4030HB 87YWX	2 Cell 4.35V / cell	DFN-10	5K/REEL
LP4030HCQVF-435	LPS LP4030HC 435YWX	3 Cell 4.35V / cell	DFN-10	5K/REEL
LP4030HDQVF-435	LPS LP4030HD 435YWX	4 Cell 4.35V / cell	DFN-10	5K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



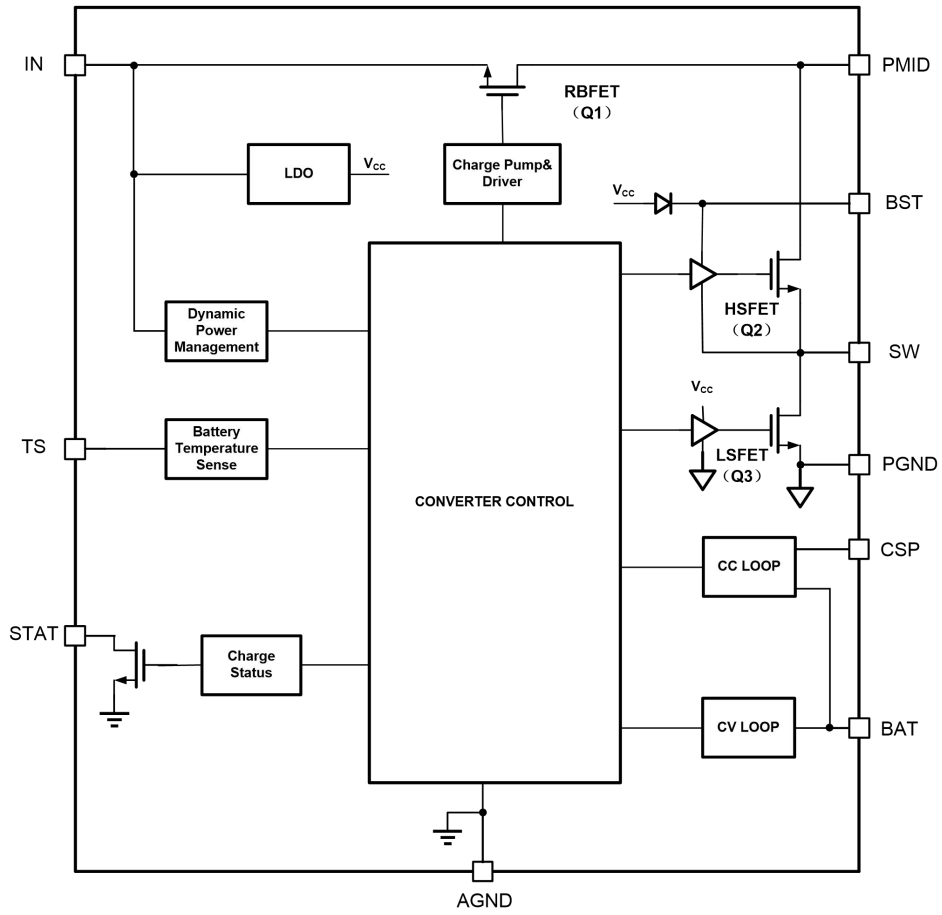
DFN-10
(Top View)

DFN-10 (Top View)

Pin Description

Pin	Name	Description
1	IN	Positive Supply Voltage Input. Place a 1μF ceramic capacitor from IN to PGND and place the capacitor as close as possible to IC.
2	TS	Battery Temperature Sense Thermistor Input. This pin senses the temperature of the battery pack and charge is suspended if the battery temperature is out of range.
3	STAT	Open-Drain Charge Status Output. When the battery is charging, this pin is pulled down to GND by an internal N-channel MOSFET. While the charge is complete, STAT pin is in high impedance.
4	PMID	Power MOSFET Input. Connect this pin with a 10uF ceramic capacitor to ground and place it as close as possible to IC.
5	PGND	Power Ground.
6	AGND	Analog Ground.
7	BST	High-side MOSFET Driver Supply Input. BST is internally connected to the cathode of the internal boost-strap diode. Connect 47nF bootstrap capacitor from BST to SW.
8	SW	Switching Node. Internally SW is connected to the source of the n-channel HSFET and the drain of the N-channel LSFET. Connect this pin to external inductor.
9	CSP	Charge Current Sensing Positive Input. Connect this pin to external current sensing resistor Rcs.
10	BAT	Battery Voltage Sensing and Charge Current Sensing Negative Input. Connect this pin to the positive terminal of the battery pack.10μF ceramic capacitor is recommended to connect from this pin to PGND.
11	PAD	Ground reference for the device that is also the thermal pad used to conduct heat from the device.

Functional Block Diagram



Absolute Maximum Ratings (1)

- IN, PMID, SW, STAT, BAT, CSP, TS Voltage to GND---------- -0.3V to 28V
- BST to SW Voltage----------0.3V to 6V
- STAT Sink Current---------- 10mA
- Maximum Junction Temperature (T_J)---------- 150℃
- Operating Ambient Temperature Range (T_A)---------- -40℃ to 85℃
- Maximum Soldering Temperature (at leads, 10 sec)---------- 260℃

Note: (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

- HBM(Human Body Model) ---------- 2KV
- MM(Machine Model) ---------- 200V

Recommended Operating Conditions

- Input Voltage---------- 4.5V to 20V
- Maximum Charge Current----------3.0A
- Operating Junction Temperature Range (T_J)---------- -40℃ to 150℃
- Ambient Temperature Range---------- -40℃ to 85℃
- Thermal Resistance θ_{JA}----------45℃/W
- Thermal Resistance θ_{JC}---------- 8℃/W

Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = 5V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range		4.5		20	V
I_{CC}	Input Supply Current	Standby mode (charge terminated)		500		μA
V_{UVLO}	Under Voltage Lockout of V_{IN}	V_{IN} Rising	3.7	3.9	4.1	V
V_{UVLO_HYS}	V_{UVLO} Hysteresis	V_{IN} Falling		150		mV
V_{OVP}	Over-Voltage Protection Threshold Voltage	V_{IN}Rising	21	22	23	V
V_{OVP_HYS}	OVP Hysteresis	V_{IN}Falling		700		mV
V_{DPM_THR}	Input Dynamic Power Management Threshold Voltage	Input Voltage is in regulation and charge current is reduced.	4.3	4.4	4.5	V
QUIESCENT CURRENT						
$I_{BAT\_Leakage}$	Battery Leakage Current	LP4030HAQVF V_{IN}=0V (IN floating), V_{BAT}=4.2V		-1.7		μA
$I_{BAT\_Standby}$	Battery Standby Current	Charge Terminated LP4030HAQVF V_{IN}=5V, V_{BAT}=4.2V		-2.2		μA

BATTTERY CHARGER						
V_{FLOAT}	Regulated Output Voltage	LP4030HAQVF	-1%	4.2	1%	V
		LP4030HAQVF-435	-1%	4.35	1%	V
		LP4030HAQVF-44	-1%	4.4	1%	V
		LP4030HBQVF	-1%	8.4	1%	V
		LP4030HBQVF-87	-1%	8.7	1%	V
		LP4030HCQVF	-1%	12.6	1%	V
		LP4030HDQVF	-1%	16.8	1%	V
V_{CS}	CSP to BAT Reference Voltage (Program Fast Charge Current)	$V_{TRIKL}<V_{BAT}<V_{FLOAT}$	48	51	54	mV
I_{BAT}	Constant Charge Current	R_{CS}=50mΩ, Constant Current Mode		1020		mA
		R_{CS}=25mΩ, Constant Current Mode		2040		mA
I_{TRIKL}	Trickle Charge Current	$V_{BAT}<V_{TRIKL}$, R_{CS}=50mΩ		102		mA
V_{TRIKL}	Trickle Charge Threshold Voltage	LP4030HAQVF V_{BAT} Rising		2.8		V
		LP4030HAQVF-435/44 V_{BAT} Rising		2.8		V
		LP4030HBQVF V_{BAT} Rising		5.6		V
		LP4030HCQVF V_{BAT} Rising		8.4		V
		LP4030HDQVF V_{BAT} Rising		11.2		V
V_{TRHYS}	Trickle Charge Hysteresis Voltage	LP4030HAQVF V_{BAT} Falling		170		mV
		LP4030HAQVF-435/44 V_{BAT} Falling		170		mV
		LP4030HBQVF V_{BAT} Falling		340		mV
		LP4030HCQVF V_{BAT} Falling		510		mV
		LP4030HDQVF		680		mV

		V_{BAT} Falling				
ΔV_{RECHRG}	Battery Recharge Voltage Difference Threshold (V_{FLOAT} -V_{RECHRG})	LP4030HAQVF		150		mV
		LP4030HAQVF-435		150		mV
		LP4030HBQVF		300		mV
		LP4030HCQVF		450		mV
		LP4030HDQVF		600		mV
T_{J_THR}	Junction Over Temperature Protection Threshold	Temperature Rising		150		℃
T_{J_HYS}	T_{J_THR} Hysteresis	Temperature Falling		30		℃
I_{TERM}	Termination Current	R_{CS}=50mΩ		102		mA
V_{STAT}	STAT Pin Output Low Voltage	I_{STAT}=5mA			0.5	V
SWITCHING CONVERTER						
F_{SW}	Switching Frequency			520		kHz
I_{MOS_LIM}	Switch MOSFET Current Limit			4.5		A
$R_{IN-PMID}$	IN-PMID MOSFET on-resistance			50		mΩ
$R_{PMID-SW}$	PMID-SW MOSFET on-resistance			50		mΩ
R_{SW-GND}	SW-PGND MOSFET on-resistance			50		mΩ
BATTERY TEMPERATURE MONITORING						
V_{NTC_H}	NTC threshold (Hot)	V_{NTC_H} falling, percentage to V_{IN}		30%		V_{IN}
V_{NTC_C}	NTC threshold (Cold)	V_{NTC_C} rising, percentage to V_{IN}		60%		V_{IN}

Typical Characteristics

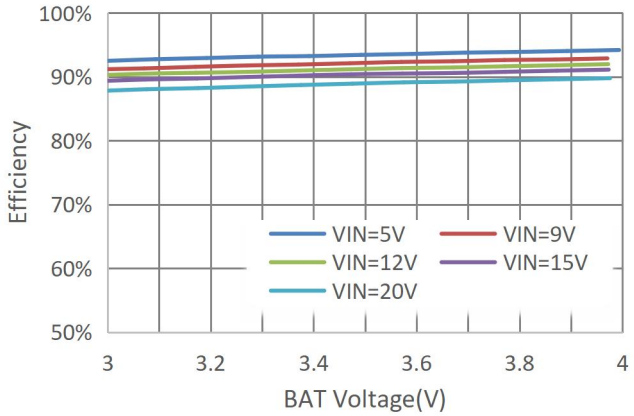


Figure 1. 1-cell constant current mode efficiency vs V_{BAT}
I_{BAT} = 1A, 25℃， LP4030HAQVF

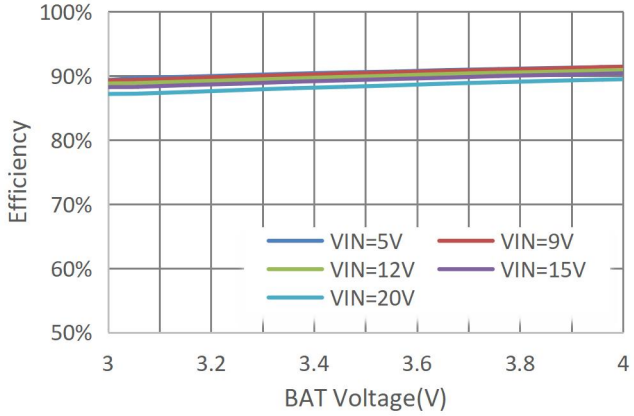


Figure 2. 1-cell constant current mode efficiency vs V_{BAT}
I_{BAT} = 2A, 25℃， LP4030HAQVF

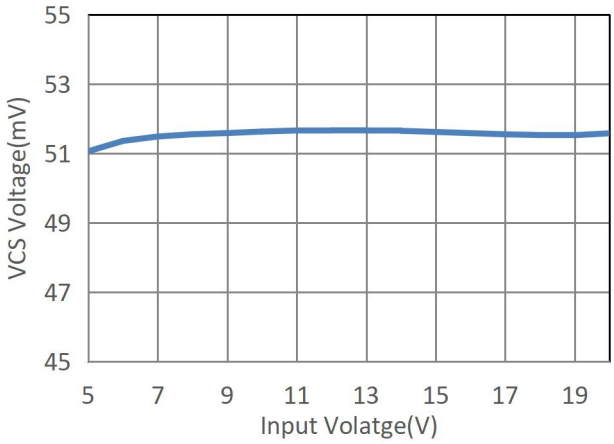


Figure 3. Constant current mode V_{CS} voltage vs V_{IN}
V_{BAT}=3.5V,R_{CS}=25mΩ, 25℃， LP4030HAQVF

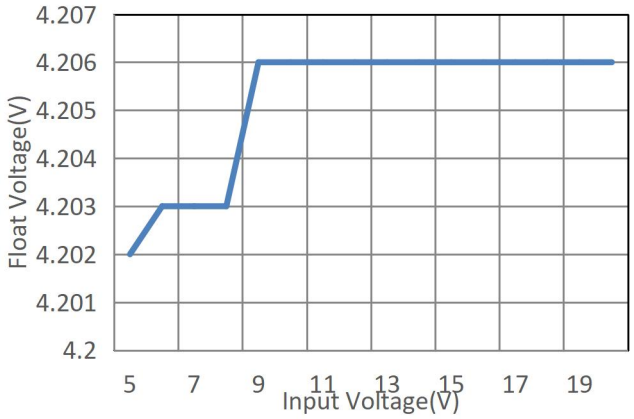


Figure 4.1-cell float voltage vs V_{IN}
25℃， LP4030HAQVF

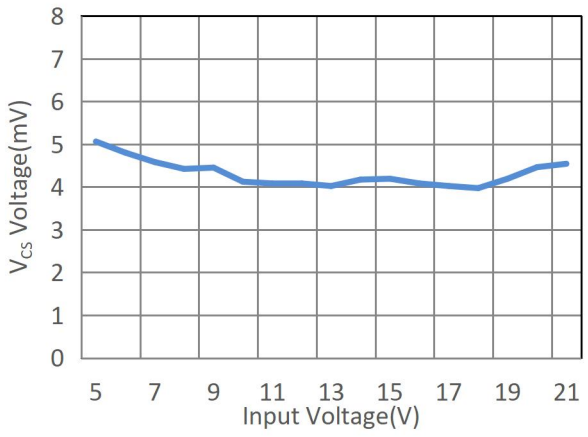


Figure 5. Terminate V_{CS} voltage vs V_{IN}
V_{BAT}=2V,R_{CS}=25mΩ, 25℃， LP4030HAQVF

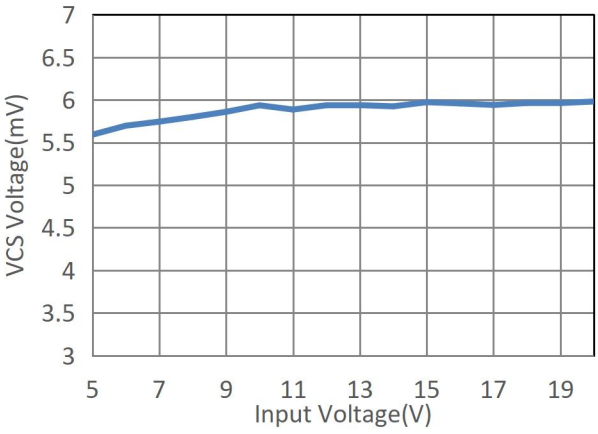


Figure 6. Trickle current mode V_{CS} voltage vs V_{IN}
V_{BAT}=2V,R_{CS}=25mΩ, 25℃， LP4030HAQVF

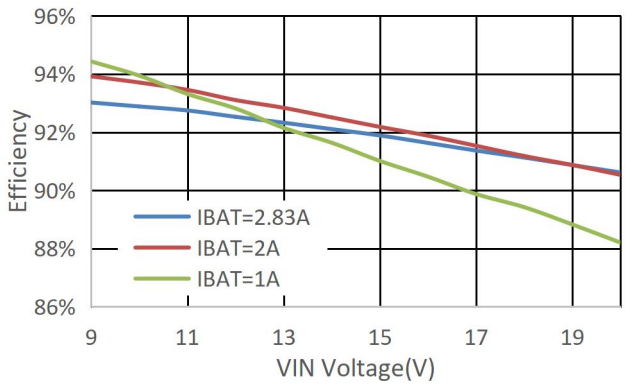


Figure 7. 2-cellsconstant current mode efficiency vs V_{IN}
V_{BAT}=7.6V, 25℃, LP4030HBQVF

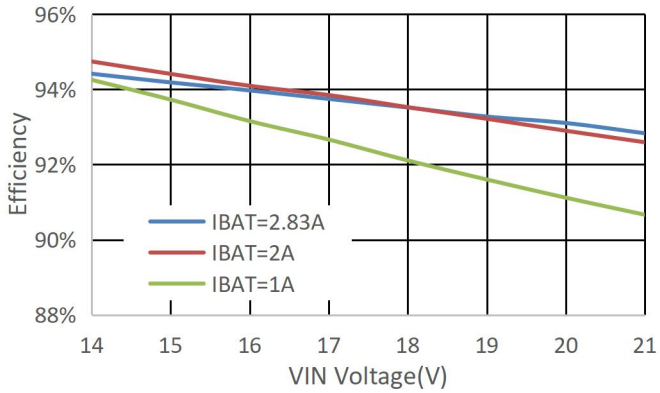


Figure 8. 3-cellsconstant current mode efficiency vs V_{IN}
V_{BAT}=11.4V, 25℃, LP4030HCQVF

Detailed Description

Overview

The LP4030H family devices are highly-integrated switching charger with up to 3A maximum charge current for 1-cell to 4-cell Li-Ion and Li-Polymer batteries. The devices charge the battery in three modes: trickle current mode, constant current mode and constant voltage mode.

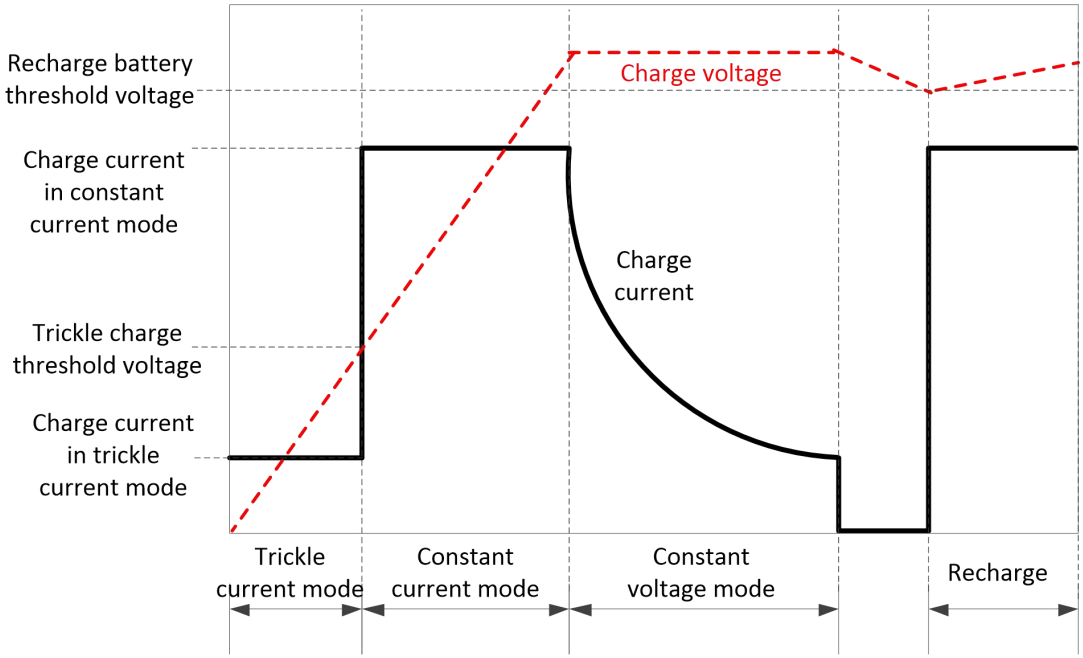


Figure 9. Typical Charge Profile

When the battery voltage is lower than trickle charge threshold voltage V_{TRIKL}, the devices are in trickle current mode, the charge current is set at 10% of fast charge current in constant current mode.

When the battery voltage increases above the trickle charge threshold voltage V_{TRIKL}, the devices enter the constant current fast charge mode, and the fast charge current is set by the external sense resistor R_{CS}. The internal reference voltage V_{CS} is regulated and the fast charge current can be calculated based on the equation showed as below:

$$I_{BAT} = \frac{V_{CS}}{R_{CS}}$$

When the battery voltage approaches the programmed float voltage, the devices enter constant voltage mode, and the charge current will start to decrease from fast charge current. When the charge current drops to 10% of fast charge current, the devices terminate the charge cycle. The devices automatically recharge the battery while the battery voltage drops by ΔV_{RECHRG} (150mV, 1-cell typical) from the float voltage.

Shutdown

The LP4030H family devices are shut down if TS pin is pulled up to IN pin. In shutdown mode, the STAT pin to GND keeps high impedance. If the voltage at the IN pin drops below (V_{BAT}+150mV) or below the UVLO level, the LP4030H devices go into a low current sleep mode with no charging, and the IN pin provides the power to

the device internal circuit to reduce the discharging current from the battery to the device.

Automatic Recharge

Once the charge cycle is terminated, the LP4030H devices continuously monitor the voltage on the BAT pin by a comparator with a 1.8ms filter. A new charge cycle restarts when the battery voltage drops by a voltage difference ΔV_{RECHRG} (150mV, 1-cell typical) from the float voltage. This ensures that the battery is always at or near a fully charged condition.

Battery Temperature Detection

The LP4030H devices continuously monitor the battery temperature by measuring the voltage between the TS pin and AGND pin. The devices compare V_{TS} to its internal thresholds V_{NTC_H} and V_{NTC_C} that is derived from internal resistor divider from V_{IN} to AGND, and then determine whether charging is allowed. The temperature sensing circuit is immune to any fluctuation in V_{IN} because both the external voltage divider and the internal thresholds (V_{NTC_H} and V_{NTC_C}) are referenced to V_{IN}.

The resistor values of R_{T1} and R_{T2} are calculated by the following equations:

For NTC Thermistors:

$$R_{T1} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{(R_{TL} - R_{TH})K_1K_2}$$

$$R_{T2} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{R_{TL}(K_1 - K_1K_2) - R_{TH}(K_2 - K_1K_2)}$$

For PTC Thermistors:

$$R_{T1} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{(R_{TH} - R_{TL})K_1K_2}$$

$$R_{T2} = \frac{R_{TL}R_{TH}(K_2 - K_1)}{R_{TH}(K_1 - K_1K_2) - R_{TL}(K_2 - K_1K_2)}$$

$K_{1(VTS\_H)}$=30%, $K_{2(VTS\_C)}$=60%.

Where R_{TL} is the low temperature resistance and R_{TH} is the high temperature resistance of thermistor, as specified by the thermistor manufacturers. If the allowed charge temperature is 0 to 45 ℃, for a typical 10kΩ-3950K NTC thermistor, R_{TL} = 32.6kΩ, R_{TH}=4.4kΩ, then R_{T1}=8.2kΩ and R_{T2}=20kΩ.

Junction Over Temperature Protection

When the internal junction temperature of LP4030H family devices exceed the junction over temperature protection threshold 150℃, the devices stop charging, after the junction temperature falls below 120℃, the charge cycle restarts.

Input Dynamic Power Management

For different input capacity source application, the LP4030H devices integrate an input current adaptive function. When the input voltage falls below the input dynamic power management threshold voltage V_{DPM_THR} as the input power capacity is not enough to charge battery at full set fast charge current, the devices begin to reduce the charge current to avoid crashing input source.

Application Information

Inductor Selection

Because the selection of inductor affects charger's steady state operation, transient behavior, loop stability and the charger's efficiency, the inductor is one of the most important components in the application design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance, and saturation current. For the LP4030H device applications, a 2.2μH~4.7μH inductor is typically selected based on cell number and input voltage. Inductor values can have typically ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. Therefore, when selecting an inductor, please make sure its rated current, especially the saturation current, is larger than its peak current during the operation. To calculate the inductor peak current in the worst case, customers need take consideration of the battery voltage, the input voltage and maximum charging current of the application. In order to leave enough design margin, the inductor value with –30% tolerance is recommended for the calculation. The inductor current ripple and peak current can be calculated as below:

$$\Delta I_{PP} = \frac{(V_{IN} - V_{BAT}) * V_{BAT}}{V_{IN} * F_{SW}} * \frac{1}{L}$$

$$I_{L\_PK} = I_{BAT} + \frac{\Delta I_{PP}}{2}$$

High inductance generates lower inductor current ripple but higher inductance has higher DCR that increases conduction loss. A good trade-off for inductance is to have inductor current ripple ΔI_{PP} within 20%-40% of fast charge current.

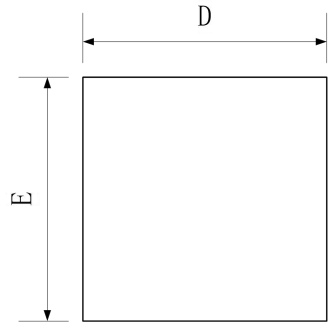
PCB Layout Consideration

As for switching charger, especially providing high current at high switching frequencies, PCB layout is important for a device to perform appropriately. If layout is not carefully done, the charger could show instability as well as EMI problems and the efficiency will be degraded as well. Here is a PCB layout priority list for proper layout.

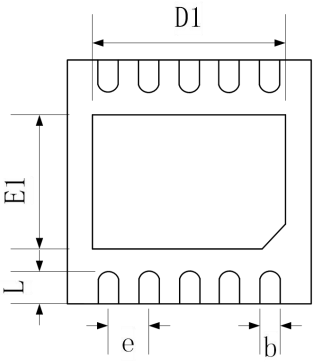
1. Place capacitor C1 as close as possible to IN pin and PGND pin.
2. Place capacitor C2 as close as possible to PMID pin and PGND pin.
3. Use single-point connection to connect charger power ground PGND to device analog ground AGND.
4. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charge current.
5. The via size and number should be enough for a given current path.
6. Place the C3 as close as possible to the BST pin.
7. Use Kevin Sense from the sensing resistor's 2 terminals to the devices' positive current sensing pin CSP and negative current sensing pin BAT. An additional 10nF ceramic capacitor can be placed close to IC.

Packaging Information

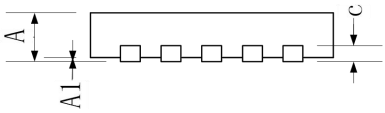
DFN-10



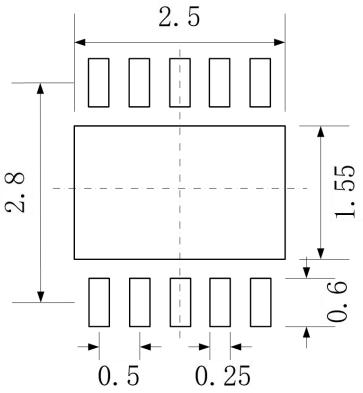
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C		0.20 REF	
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
e		0.50 BSC	
L	0.30	0.40	0.50