TEXAS INSTRUMENTS
LM64440-Q1, LM64460-Q1
ZHCSLU1B – OCTOBER 2022 – REVISED AUGUST 2024

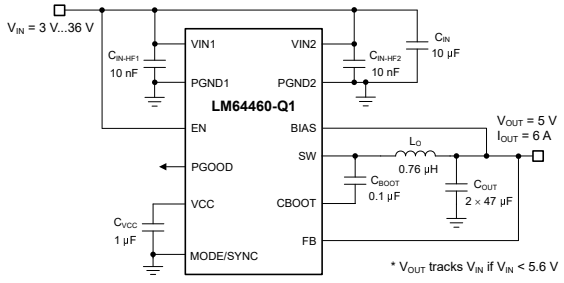
LM644x0-Q1 具有引脚可选轻负载模式、经优化可实现可靠性和低 EMI 的 3V 至 36V、4A 和 6A、汽车级同步直流/直流降压转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
- 功能安全型
  - 可帮助进行功能安全系统设计的文档
- 多功能同步直流/直流降压转换器
  - 3V 至 36V 宽输入电压范围，可耐受高达 42V 的负载突降瞬态
  - 提供 4A 和 6A 选项
  - 1% 精度、3.3V/5V 固定或可调节输出电压（1V 至 95% V_{IN}）
  - 150°C 最大结温
  - 固定的 2.1MHz 开关频率（使用 SYNC 信号时，在 200kHz 至 2.2MHz 范围内可调）
- 通过优化引脚排列设计和相邻引脚短路测试间隙提高可靠性
- 专为满足低 EMI 要求而设计
  - 具有双输入路径的增强型 HotRod™ QFN 封装可减少开关节点振铃
  - 引脚可配置的展频调制
  - 轻负载时可选择 FPWM 或 PFM 模式
- 在整个负载范围内具有高效率
  - 13.5V V_{IN}、5V V_{OUT}、6A、2.1MHz 时为 92.5%
  - 在 3.3V_{OUT} 空载输入电流下典型值为 7µA
  - 0.6µA 典型关断静态电流
  - 满载时的典型压降为 0.6V
  - 具有用于提升效率的外部偏置选项
- 使用 LM644x0-Q1 并借助 WEBENCH® Power Designer 创建定制稳压器设计方案

2 应用

- 汽车信息娱乐系统与仪表组：音响主机、媒体中心、USB 充电、显示屏
- 汽车 ADAS 和车身电子装置



典型电路原理图

3 说明

LM644x0-Q1 属于汽车级同步直流/直流降压转换器系列，具有卓越的效率和超低的 I_Q。该器件具有集成式高侧和低侧 MOSFET，能够在 3V 至 36V 的宽输入电压范围内提供高达 6A 的输出电流，支持高达 42V 的负载突降瞬态。该转换器可对压降进行软恢复，因此无需对输出进行过冲。

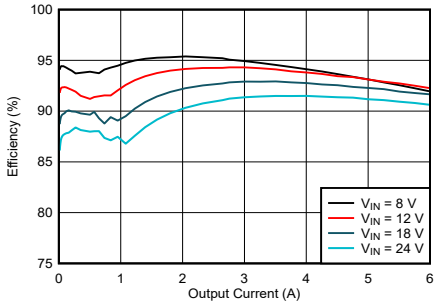
LM644x0-Q1 集成了用于实现卓越 EMI 性能的诸多特性，包括展频频率调制、低 EMI 增强型 HotRod QFN 封装（可缓解开关节点振铃）和对称引脚排列（可实现理想的输入电容器放置）。开关频率在 200kHz 和 2.2MHz 之间可同步，从而避免敏感频带，同时可根据应用的具体要求优化效率或设计尺寸。

PFM 模式可在轻负载运行时进行频率折返，实现仅 7µA（典型值）的空载电流消耗和高轻负载效率。PWM 模式和 PFM 模式之间无缝转换，以及低 MOSFET 导通电阻和外部偏置输入，可在整个负载范围内提供卓越的效率和热性能。该封装在关键电源引脚之间有多个 NC 引脚，从而改进了故障模式和影响分析 (FMEA) 结果。

器件信息

器件型号(1)	电流	封装(2)
LM64460-Q1	6A	RYF（VQFN，22）
LM64440-Q1	4A	

(1) 请参阅 *器件比较表*。
(2) 有关更多信息，请参阅节 11。



效率，V_{OUT} = 5V，f_{SW} = 2.1MHz，LM64460-Q1

Table of Contents

4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	OUTPUT VOLTAGE	CURRENT	SPREAD SPECTRUM	LIGHT-LOAD MODE	SWITCHING FREQUENCY	TEST TEMPERATURES
LM64460-Q1	LM64460APPQRYFRQ1	Adjustable	6A	Pin selectable	Pin selectable	2.1MHz	Standard
	LM64460APPSRYFRQ1	Adjustable	6A	Pin selectable	Pin selectable	2.1MHz	Tri-temperature
	LM64460BPPQRYFRQ1	3.3V	6A	Pin selectable	Pin selectable	2.1MHz	Standard
	LM64460CPPQRYFRQ1	5V	6A	Pin selectable	Pin selectable	2.1MHz	Standard
LM63460-Q1	LM63460AASQRYFRQ1	Adjustable	6A	On	AUTO	Adjustable	Standard
	LM63460AFSQRYFRQ1	Adjustable	6A	On	FPWM	Adjustable	Standard
LM64440-Q1	LM64440APPQRYFRQ1	Adjustable	4A	Pin selectable	Pin selectable	2.1MHz	Standard
	LM64440BPPQRYFRQ1	3.3V	4A	Pin selectable	Pin selectable	2.1MHz	Standard
	LM64440CPPQRYFRQ1	5V	4A	Pin selectable	Pin selectable	2.1MHz	Standard
LM63440-Q1	LM63440AASQRYFRQ1	Adjustable	4A	On	AUTO	Adjustable	Standard
	LM63440AFSQRYFRQ1	Adjustable	4A	On	FPWM	Adjustable	Standard

5 Pin Configuration and Functions

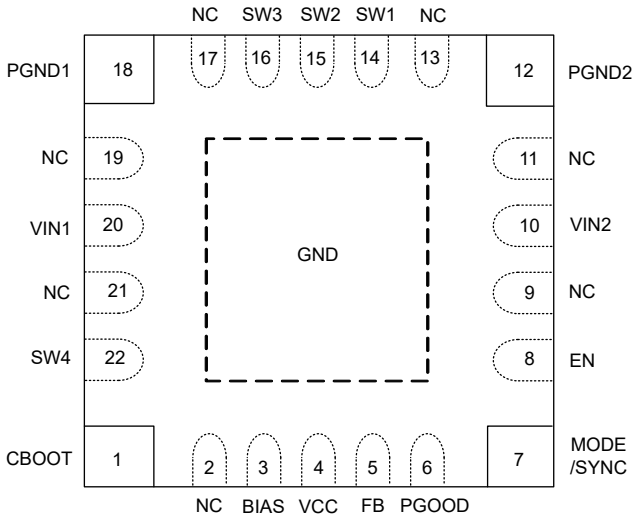


图 5-1. 22-Pin Enhanced HotRod™ VQFN-FCRLF RYF Package (Top View)

表 5-1. Pin Functions

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
CBOOT	1	P	High-side driver supply rail. Connect a 100nF capacitor between SW and CBOOT. An internal bootstrap diode connects to VCC and allows the bootstrap capacitor to charge when SW is low.
NC	2	—	No internal connection
BIAS	3	P	Input to the internal LDO. Connect to the output voltage point to improve efficiency. Connect an optional high-quality 0.1µF to 1µF capacitor from this pin to GND for improved noise immunity. If the output voltage is above 12V, connect BIAS to GND.
VCC	4	O	Internal LDO output. VCC supplies the internal control circuits. Do not connect to any external loads. Connect a high-quality 1µF capacitor from VCC to GND.
FB	5	I	Output voltage feedback input to the internal control loop. Connect to the output voltage sense point for fixed 3.3V or 5V output voltage settings. Connect to a feedback divider tap point to set an adjustable output voltage. Do not float or connect to GND.
PGOOD	6	O	Open-drain power-good status indicator output. Pull up PGOOD to a suitable voltage supply through a current-limiting resistor. High = power OK, low = fault. The PGOOD output goes low when EN = low, V_{IN} > 1V.
MODE/SYNC	7	I	MODE/SYNC controls the mode of operation of the LM64460-Q1. Modes include AUTO mode (automatic PFM / PWM operation), FPWM, and synchronization to an external clock. When synchronized, the clock triggers on rising edge of an external clock signal. Spread spectrum operation is also controlled by this pin. See *MODE/SYNC Operation* . Do not float this pin.
EN	8	I	Enable input and undervoltage lockout (UVLO) programming pin. If the EN voltage is below 0.4V, the converter is in shutdown mode with all functions disabled. If the EN voltage is greater than 1.263V (and the VCC voltage is above the UVLO threshold), the converter is active and switching. Use the precision enable function to set an adjustable input voltage UVLO with hysteresis. See *Precision Enable and Input Voltage UVLO (EN)* .
NC	9	—	No internal connection
VIN2	10	P	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. A low-impedance connection must be provided to VIN1.
NC	11	—	No internal connection
PGND2	12	G	Power-ground connection to the internal low-side MOSFET. Connect to system ground. A low-impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
NC	13	—	No internal connection

表 5-1. Pin Functions（续）

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
SW1	14	P	Switch node of the converter. Connect to the output inductor.
SW2	15		
SW3	16		
NC	17	—	No internal connection
PGND1	18	G	Power ground to the internal low-side MOSFET. Connect to system ground. A low-impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
NC	19	—	No internal connection
VIN1	20	P	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. A low-impedance connection must be provided to VIN2.
NC	21	—	No internal connection
SW4	22	P	Switch node of the converter. Connect to the bootstrap capacitor.
GND	-	G	Exposed pad of the package internally connected to ground. The exposed pad must be connected to the PCB inner-layer system ground plane or planes using numerous thermal vias to reduce thermal impedance. See *Layout Guidelines* .

(1) P = Power, G = Ground, I = Input, O = Output

5.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (VQFN) packages do not have solderable or exposed pins and terminals that are easily viewed. Therefore, visually determining whether or not the package is successfully soldered onto the printed-circuit board (PCB) is difficult. The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM644x0-Q1 is assembled using a 22-pin Enhanced HotRod QFN package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

5.2 Pinout Design for Clearance and FMEA

The LM644x0-Q1 has a carefully designed pinout arrangement that provides additional clearance spacing between high-voltage pins (VIN, SW, and CBOOT) and nearby low-voltage pins (such as PGND). Moreover, the LM644x0-Q1 pinout is designed for critical automotive applications requiring functional safety system design with stricter reliability and higher durability. In terms of pin FMEA (failure mode effects analysis), the typical failure scenarios considered include short circuit to ground, short circuit to input supply (VIN), short circuit to a neighboring pin, and if a pin is left open circuit. These faults are considered as applied externally to the IC and therefore are board-level failures rather than IC-level reliability failures. Example sources of such faults are stray conductive filaments causing pin-to-pin shorts or a board manufacturing defect causing an open-circuit track. The LM644x0-Q1 fixed output voltage versions in particular are considered pin-FMEA compliant in the event of a pin short circuit to a neighboring pin, so the output voltage stays at or below the regulation voltage.

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	VIN1, VIN2 to PGND1, PGND2	–0.3	42	V
	CBOOT to SW	–0.3	5.5	V
	BIAS to PGND1, PGND2	–0.3	16	V
	EN to PGND1, PGND2	–0.3	42	V
	MODE/SYNC to PGND1, PGND2	–0.3	lower of 36 and V_{IN} + 5	V
	FB to PGND1, PGND2	–0.3	16	V
	PGOOD to PGND1, PGND2	0	20	V
Output Voltage	SW to PGND1, PGND2(2)	–0.3	V_{IN} + 0.3	V
	VCC to PGND1, PGND2	–0.3	5.5	V
Current	PGOOD sink current		10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A voltage of 2V below PGND and 2V above V_{IN} can appear on this pin for ≤ 200ns with a duty cycle of ≤ 0.01%.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) Device HBM Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 Device CDM Classification Level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltage	Input voltage range after start-up	3		36	V
Input voltage	BIAS pin operating voltage			12	V
Output voltage	Output voltage range for adjustable version(2)	1		0.95*V_{IN}	V
Frequency	Free-running frequency		2.1		MHz
Sync frequency	Synchronization frequency range	200		2200	kHz
Load current	Output DC current range, LM64440-Q1(3)	0		4	A
Load current	Output DC current range, LM64460-Q1(3)	0		6	A
Temperature	Operating junction temperature T_J range	–40		150	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional. For detailed specifications and conditions, see Electrical Characteristics table.
(2) Under no conditions should the output voltage be allowed to fall below zero volts.
(3) Maximum continuous DC current may be derated when operating with high switching frequency and/or high ambient temperature. See Application Information for details.

6.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7 and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, the EVM for this device achieves an $R_{\theta JA}$ of 23.5℃/W.

THERMAL METRIC[1]		LM64460-Q1, LM64440-Q1 RYF (VQFN) 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (LM64460-Q1 EVM)[3]	23.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7)[2]	38.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7 and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.
(3) Refer to the LM64460-Q1 EVM User's Guide for board layout and additional information. For thermal design information please see the Application Information section.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is the converter output voltage.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
$V_{IN\_OPERATE}$	Input operating voltage[1]	Needed to start up	3.95			V
		Once operating	3.0			
$V_{IN\_OPERATE\_H}$	Hysteresis[1]			1		V
I_{Q_VIN}	Operating quiescent current (not switching)[2]	V_{FB} = +5%, V_{BIAS} = 5V, V_{OUT} = 5V		9	18	µA
I_Q	Operating quiescent current (not switching); measured at VIN pin[3]	V_{FB} = +5%, V_{BIAS} = 5V		0.6	6	µA
I_{BIAS}	Current into BIAS pin (not switching, maximum at T_J = 125°C)[3]	V_{FB} = +5%, V_{BIAS} = 5V, AUTO mode		24	31.2	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0V, T_J = 25°C		0.6	6	µA
ENABLE						
V_{EN-TH}	Enable input threshold voltage (rising)			1.263		V
V_{EN-ACC}	Enable input threshold voltage – rising deviation from typical		–5%		5%	
$V_{EN-HYST}$	Enable threshold hysteresis as percentage of V_{EN-TH} (typical)		24%	28%	32%	
$V_{EN-WAKE}$	Enable wake-up threshold		0.4			V
I_{EN}	Enable pin input current	V_{IN} = V_{EN} = 13.5V		2.3		nA
LDO AND VCC						

6.5 Electrical Characteristics（续）

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is the converter output voltage.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Internal V_{CC} voltage	V_{BIAS} > 3.4V, CCM operation(1)		3.3		V
		V_{BIAS} = 3.1V, non-switching		3.1		
$V_{CC-UVLO}$	Internal V_{CC} undervoltage lockout	V_{CC} rising undervoltage threshold		3.6		V
$V_{CC-UVLO-HYST}$	Internal V_{CC} undervoltage lockout hysteresis	Hysteresis below $V_{CC-UVLO}$		1.1		V
FEEDBACK						
V_{FB_acc}	Initial reference voltage accuracy for 5V, 3.3V and adjustable output versions	V_{IN} = 3.3V to 36V, T_J = 25°C, FPWM mode	–1%		1%	
V_{OUT_acc}	Reference voltage accuracy for fixed 3.3V V_{OUT} trim option	FPWM mode	3.2587	3.3	3.3413	V
V_{OUT_acc}	Reference voltage accuracy for fixed 5V V_{OUT} trim option	FPWM mode	4.9375	5	5.0625	V
R_{FB}	Resistance from FB to GND	5V option		1.85		MΩ
		3.3V option		2.1		
I_{FB}	Input current from FB to GND	Adjustable versions only, V_{FB} = 1V		1	50	nA
OSCILLATOR						
f_{SW}	Switching frequency	Center frequency with or without spread spectrum, CCM operation	1.9	2.1	2.3	MHz
f_{S_SS}	Frequency span of spread spectrum operation – largest deviation from center frequency	Spread spectrum active		2%		
f_{PSS}	Spread spectrum pattern frequency(1)	Spread spectrum active, f_{SW} = 2.1MHz			1.5	Hz
MODE/SYNC						
$I_{MODE/SYNC}$	MODE/SYNC pin leakage current after startup	$V_{MODE/SYNC}$ = 3.3V		1		nA
		$V_{MODE/SYNC}$ = 5.5V		1		
V_{MODE_L}	MODE/SYNC input voltage low				0.4	V
V_{MODE_H}	MODE/SYNC input voltage high		1.6			V
V_{SYNCD_HYST}	MODE/SYNC input voltage hysteresis		0.155		1	V
V_{MODE_H2}	Spread spectrum on if MODE/SYNC voltage is below this voltage and above V_{SYNCDH}	Level-dependent operation	2.5			V
V_{MODE_H3}	Spread spectrum off if MODE/SYNC is above this voltage	Level-dependent operation			4.9	V
R_{MODE_H}	MODE/SYNC attached resistance indicating spread spectrum off	Level-dependent operation	30			kΩ
R_{MODE_L}	MODE/SYNC attached resistance indicating spread spectrum on	Level-dependent operation			6	kΩ
MOSFETS						
$R_{DS(on)HS}$	Power switch on-resistance	High-side MOSFET $R_{DS(on)}$		41	82	mΩ
$R_{DS(on)LS}$	Power switch on-resistance	Low-side MOSFET $R_{DS(on)}$		21	45	mΩ
$V_{BOOT-UVLO}$	Voltage on CBOOT relative to SW that turns off the high-side switch			2.1		V
CURRENT LIMITS						

6.5 Electrical Characteristics（续）

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is the converter output voltage.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{L-HS}	High-side switch current limit, LM64460-Q1(4)	Duty cycle approaches 0%	8.9	10.3	11.5	A
	High-side switch current limit, LM64440-Q1(4)		6	7	8.1	
I_{L-LS}	Low-side switch current limit, LM64460-Q1		6.1	7.1	8.1	A
	Low-side switch current limit, LM64440-Q1		4.0	4.8	5.4	
I_{L-ZC}	Zero-cross current limit. Positive current direction is out of the SW pin	AUTO mode, static measurement		0.25		A
I_{L-NEG}	Negative current limit. Positive current direction is out of the SW pin, LM64460-Q1	FPWM operation		–3		A
	Negative current limit FPWM and SYNC Modes. Positive current direction is out of the SW pin, LM64440-Q1			–2		
$I_{PK\_MIN\_0}$	Minimum peak command in AUTO mode / device current rating	Pulse duration < 100ns		25%		
$I_{PK\_MIN\_100}$	Minimum peak command in AUTO mode / device current rating	Pulse duration > 1µs		12.5%		
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage	Hiccup disabled during soft start		40%		
POWER GOOD						
PGD_{OV}	PGOOD upper threshold – rising	% of V_{OUT} setting	105%	107%	110%	
PGD_{UV}	PGOOD lower threshold – falling	% of V_{OUT} setting	92%	94%	96.5%	
PGD_{HYST}	PGOOD hysteresis	% of V_{OUT} setting		1.3%		
$V_{IN(PGD-VALID)}$	Input voltage for proper PGOOD function		1.0			V
$V_{PGD(LOW)}$	Low-level PGOOD function output voltage	46µA pullup to PGOOD, V_{IN} = 1V, V_{EN} = 0V			0.4	V
		1mA pullup to PGOOD, V_{EN} = 0V			0.4	
		2mA pullup to PGOOD, V_{EN} = 3.3V			0.4	
R_{PGD}	$R_{DS(on)}$ of PGOOD output	1mA pullup to PGOOD, V_{EN} = 0V		17	40	Ω
		1mA pullup to PGOOD, V_{EN} = 3.3V		40	90	Ω
I_{OV}	Pulldown current at the SW node in an overvoltage condition			0.5		mA
THERMAL SHUTDOWN						
T_{SHD}	Thermal shutdown rising threshold(1)		158	168	180	℃
$T_{SHD-HYS}$	Thermal shutdown hysteresis(1)			10		℃

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.
(2) $I_{Q\_VIN} = I_Q + I_{BIAS} \times (V_{OUT} / V_{IN})$
(3) This is the current used by the device while not switching, open loop, with FB pulled to +5% above nominal. It does not represent the total input current to the converter while regulating.
(4) High-side current limit is a function of duty cycle. High-side current limit value is highest at small duty cycle and less at higher duty cycle.

6.6 Timing Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V.

Parameter		Test Condition	MIN	TYP	MAX	UNIT
SWITCH NODE						
$t_{ON(min)}$	Minimum HS switch on time	V_{IN} = 20V, I_{OUT} = 2A		55	70	ns
$t_{ON(max)}$	Maximum HS switch on time			9		µs
$t_{OFF(min)}$	Minimum LS switch on time	V_{IN} = 4V, I_{OUT} = 1A		65	85	ns
t_{SS}	Time from first SW pulse to Vref at 90%	$V_{IN} \geqslant$ 4.2V	2	3	4	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if output not in regulation	$V_{IN} \geqslant$ 4.2V	4.5	6.5	8.5	ms
t_W	Short circuit wait time ("hiccup" time)			40		ms
ENABLE						
t_{EN}	Turn-on delay(1)	C_{VCC} = 1µF, time from EN high to first SW pulse if output starts at 0V		0.7		ms
t_B	Blanking of EN after rising or falling edges	Low level is 0.6V	4		8	µs
SYNC						
t_{PULSE_H}	High duration needed to be recognized as a pulse		100			ns
t_{PULSE_L}	Low duration needed to be recognized as a pulse		100			ns
t_{MODE}	Time at one level needed to indicate FPWM or AUTO mode		16.5			µs
t_{SYNC}	High or low signal duration in a valid synchronization signal				8	µs
t_{MEAS}	MODE/SYNC pin duration of resistance test upon entering AUTO mode	Level-dependent MODE/SYNC pin operation		25		µs
POWER GOOD						
$t_{PGDFLT(rise)}$	Delay time to PGOOD high signal		1.5	2	2.5	ms
$t_{PGDFLT(fall)}$	Glitch filter time constant for PGOOD function			24		µs

(1) Parameter specified using design, statistical analysis and production testing of correlated parameters; not tested in production.

6.7 Systems Characteristics

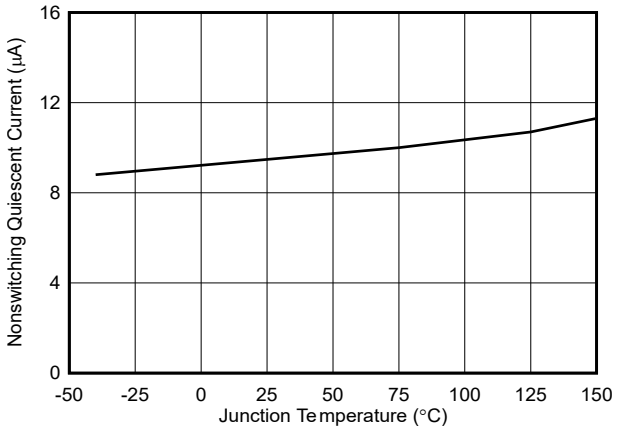
The following values are specified by design provided that the component values in the typical application circuit are used. Limits apply over the junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are derived using test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output setting. *These parameters are not tested in production.*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EFFICIENCY						
η_{5V_2p1MHz}	Typical 2.1MHz efficiency	V_{OUT} = 5V, I_{OUT} = 6A, LM64460-Q1		92.5%		
		V_{OUT} = 5V, I_{OUT} = 4A, LM64440-Q1		93%		
		V_{OUT} = 5V, I_{OUT} = 100µA, R_{FBT} = 1MΩ		73%		
η_{3p3V_2p1MHz}	Typical 2.1MHz efficiency	V_{OUT} = 3.3V, I_{OUT} = 6A, LM64460-Q1		90%		
		V_{OUT} = 3.3V, I_{OUT} = 4A, LM64440-Q1		91%		
		V_{OUT} = 3.3V, I_{OUT} = 100µA, R_{FBT} = 1MΩ		71%		
RANGE OF OPERATION						
V_{VIN_MIN1}	V_{IN} for full functionality at reduced load, after start-up	V_{OUT} set to 3.3V	3.0			V
V_{VIN_MIN2}	V_{IN} for full functionality at 100% of maximum rated load, after start-up	V_{OUT} set to 3.3V	3.95			V
I_{Q-VIN}	Operating quiescent current(1)	V_{OUT} = 3.3V, I_{OUT} = 0A, AUTO mode, R_{FBT} = 1MΩ		7		µA
		V_{OUT} = 5V, I_{OUT} = 0A, AUTO mode, R_{FBT} = 1MΩ		10		
V_{OUT5}	Output voltage for 5V factory option	V_{IN} = 5.8V to 36V, I_{OUT} = 6A, LM64460-Q1 or I_{OUT} = 4A, LM64440-Q1	4.9	5	5.1	V
		AUTO mode factory option, V_{IN} = 5.5V to 36V, I_{OUT} = 100µA to 100mA	4.9	5.05	5.125	
V_{OUT3}	Output voltage for 3.3V factory option	V_{IN} = 3.9V to 36V, I_{OUT} = 6A, LM64460-Q1 or I_{OUT} = 4A, LM64440-Q1	3.24	3.3	3.35	V
		V_{IN} = 3.9V to 36V, I_{OUT} = 100µA to 100mA	3.24	3.33	3.38	
V_{DROP1}	Input-to-output voltage differential to maintain regulation accuracy without inductor DCR drop	V_{OUT} = 3.3V, I_{OUT} = 4A, –3% output accuracy at 25°C		0.4		V
		V_{OUT} = 3.3V, I_{OUT} = 4A, –3% output accuracy at 125°C		0.55		
V_{DROP2}	Input-to-output voltage differential to maintain $f_{SW} \geqslant$ 1.85MHz, without inductor DCR drop	V_{OUT} = 3.3V, I_{OUT} = 4A, –3% regulation accuracy at 25°C		0.8		V
		V_{OUT} = 3.3V, I_{OUT} = 4A, –3% regulation accuracy at 125°C		1.2		
D_{MAX}	Maximum switch duty cycle	f_{SW} = 1.85MHz		87%		
		While in frequency foldback	98%			

(1) See detailed Input Supply Current for the meaning of this specification and how it can be calculated.

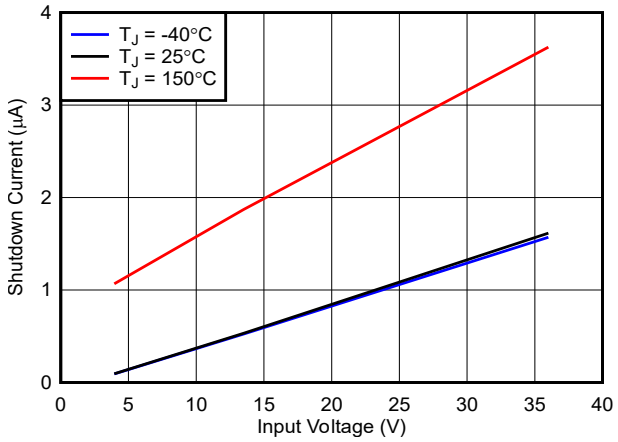
6.8 Typical Characteristics

Unless otherwise specified, V_{IN} = 13.5V and f_{SW} = 2.1MHz.



V_{BIAS} = 5V

图 6-1. Non-Switching Input Supply Current



V_{EN} = 0V

图 6-2. Shutdown Supply Current

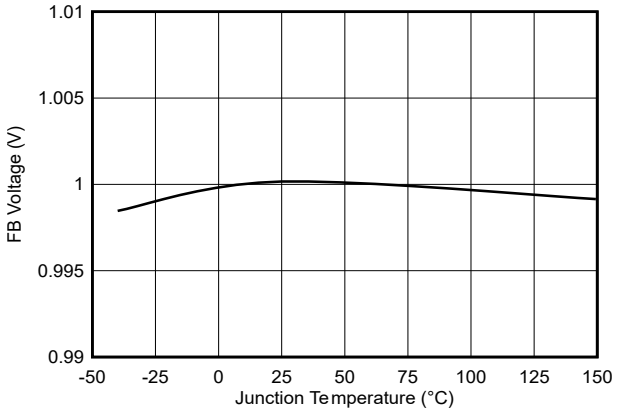


图 6-3. Feedback Voltage

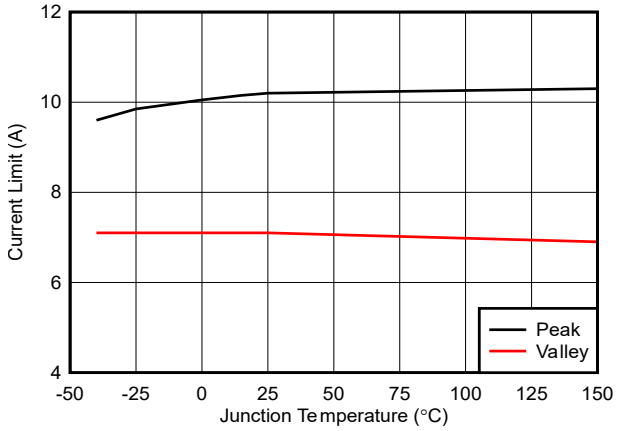


图 6-4. High-Side and Low-Side Current Limits

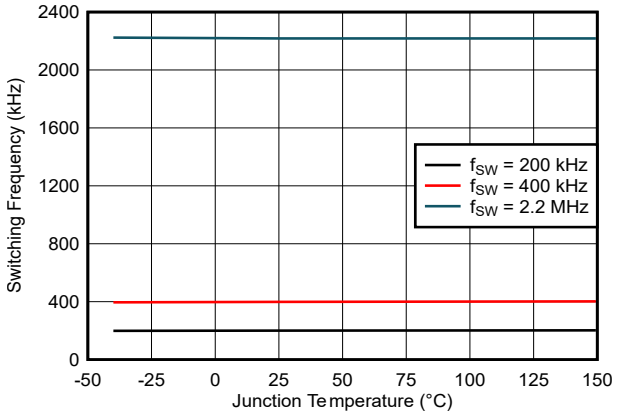


图 6-5. Switching Frequency Set by SYNC

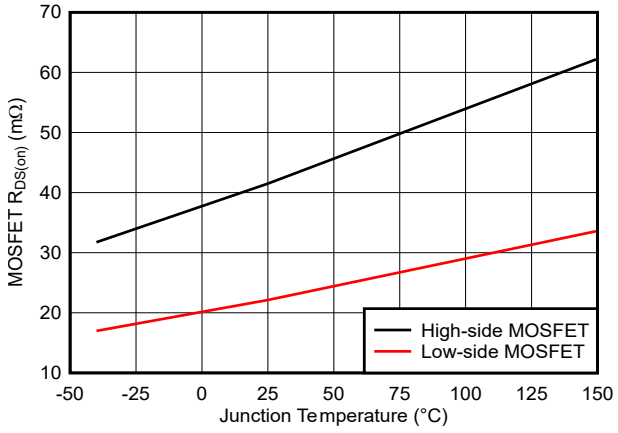


图 6-6. High-Side and Low-Side MOSFET $R_{DS(on)}$

6.8 Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 13.5V and f_{SW} = 2.1MHz.

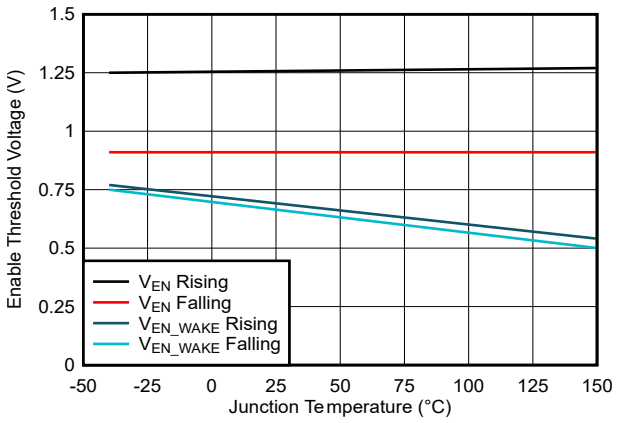


图 6-7. Enable Thresholds

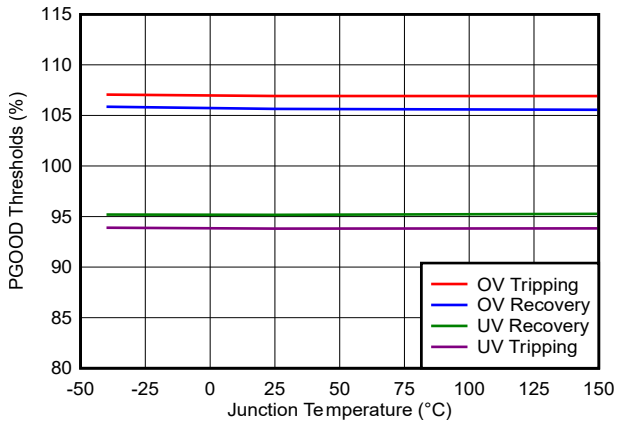


图 6-8. PGOOD Thresholds

7 Detailed Description

7.1 Overview

The LM644x0-Q1 is an easy-to-use, synchronous, buck DC/DC converter designed for a wide variety of automotive applications where strict reliability and low EMI are of paramount importance. The devices operates over an input voltage range of 3.95V to 36V, with operation down to 3V after start-up and transients as high as 42V. The LM64460-Q1 delivers up to 6A DC while the LM64440-Q1 delivers 4A DC load current with high conversion efficiency and ultra-low input quiescent current in a very small design size.

The LM644x0-Q1 operates at a default switching frequency of 2.1MHz but can be synchronized across a frequency range of 200kHz to 2.2MHz. The converter includes specific features for optimal EMI performance in noise-sensitive automotive applications, such as:

- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Parallel input paths with a symmetrical capacitor layout minimize parasitic inductance, switch-voltage ringing, and radiated field coupling.
- Pseudo-random spread spectrum (PRSS) modulation reduces peak emissions.
- Frequency synchronization and pin-selectable FPWM mode enable constant switching frequency across the full load current range.
- Integrated high-side and low-side power MOSFETs with enhanced gate-drive control enable low-noise PWM switching.

Together, these features significantly reduce EMI filtering requirements, thus eliminating shielding and other expensive EMI mitigation measures, while helping to meet the CISPR 25 Class 5 automotive EMI standard for conducted and radiated emissions.

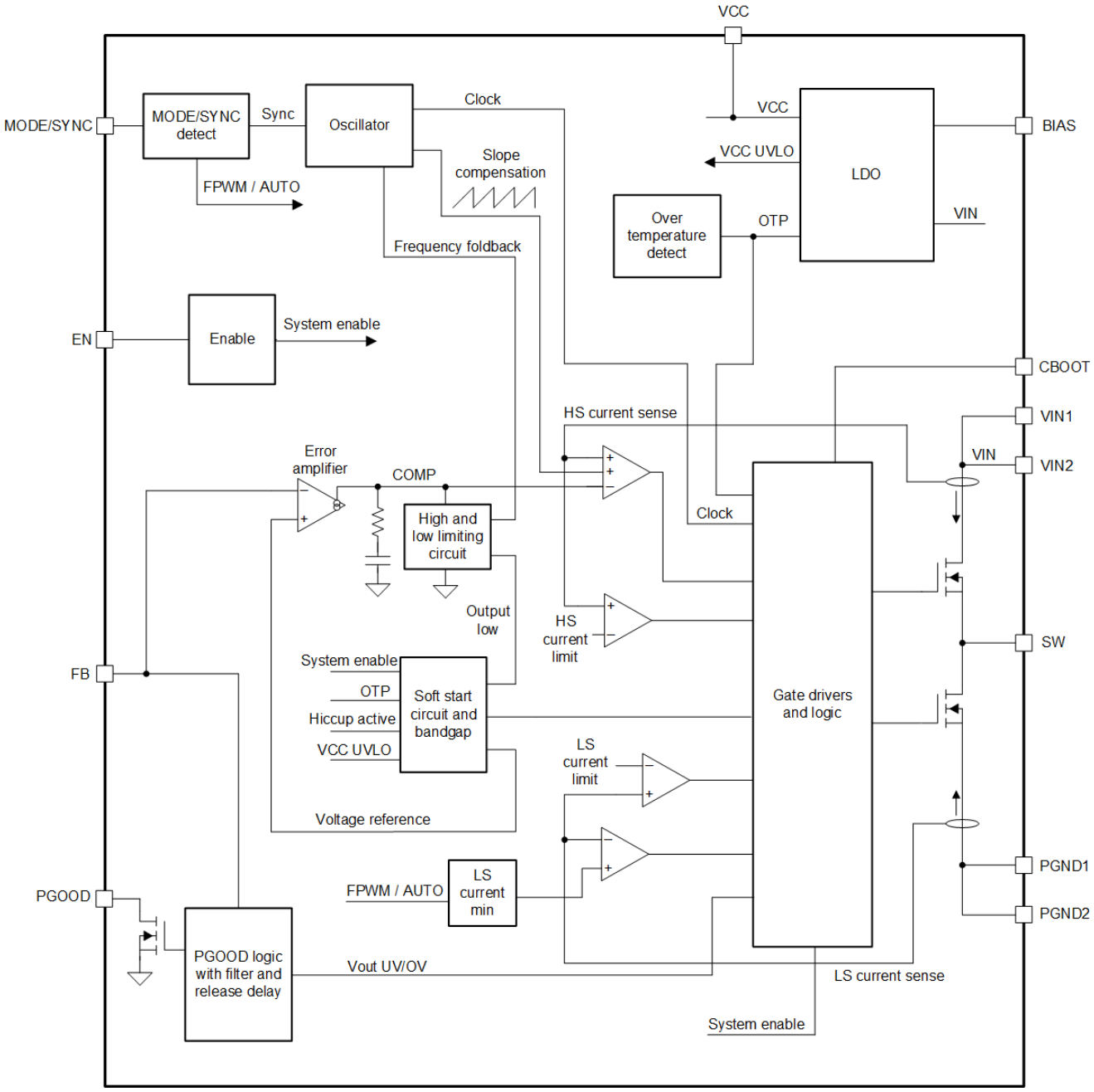
The enhanced HotRod QFN package of the LM644x0-Q1 has a carefully designed wettable-flank pinout arrangement that provides additional clearance spacing between adjacent VIN, SW, or PGND power pins to improve reliability and pin FMEA. The converter also incorporates other features for comprehensive system requirements, including:

- A precision enable input with hysteresis for programmable line undervoltage lockout (UVLO)
- Cycle-by-cycle peak and valley current limits for excellent inductor sizing
- An open-drain power-good monitor for power-rail sequencing and fault reporting
- Internally fixed output voltage soft start
- Monotonic start-up into prebiased loads
- Thermal shutdown with automatic recovery

The LM644x0-Q1 is qualified to AEC-Q100 grade 1 and has electrical characteristics specified up to a maximum junction temperature of 150°C. The following help provide an excellent point-of-load regulator design for automotive applications requiring enhanced reliability and durability:

- Wide input voltage range
- Low quiescent current consumption
- Optimized thermal design and high-temperature operation
- Improved pin FMEA
- Small design size

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range (VIN1, VIN2)

With a steady-state input voltage range from 3V to 36V, the LM644x0-Q1 is intended for step-down conversions from typical 12V and 24V automotive supply rails. The schematic circuit in 图 7-1 shows all the necessary components to implement an LM644x0-Q1 step-down regulator using a single input supply.

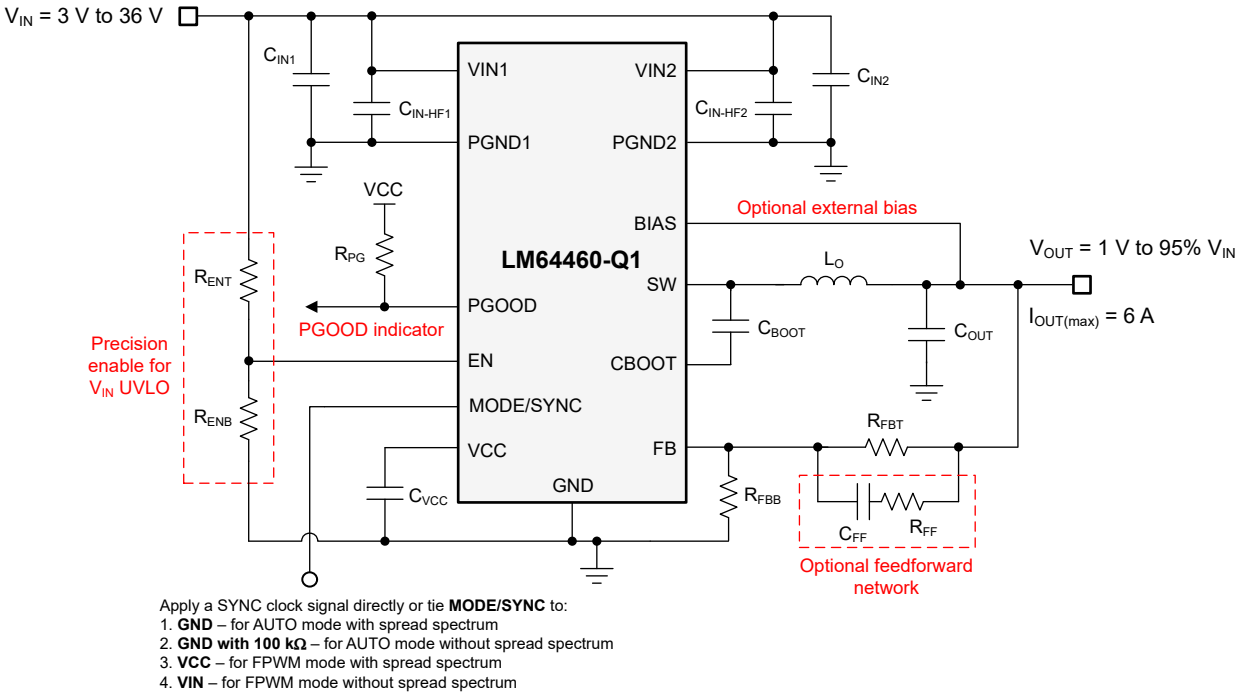


图 7-1. LM64460-Q1 Schematic Diagram with Input Voltage Operating Range of 3V to 36V

The minimum input voltage required for start-up is 3.95V. Take extra care to make sure that the voltage at the VIN pins of the converter (VIN1 and VIN2) does not exceed the absolute maximum voltage rating of 42V during line or load transient events. Voltage ringing at the VIN pins that exceeds the *Absolute Maximum Ratings* can damage the IC.

7.3.2 Output Voltage Setpoint (FB)

While dependent on switching frequency and load current levels, the LM644x0-Q1 is generally capable of providing an output voltage in the range of 1V to a maximum of slightly less than the input voltage. If the LM64460-Q1 converter is a fixed 3.3V or 5V output option, simply connect FB to the output at the point of regulation. With an adjustable output voltage version, define the output voltage setpoint with feedback resistors designated as R_{FBT} and R_{FBB} as shown in 图 7-1.

Adjustable versions of the converter use a 1V reference voltage, and the internal error amplifier regulates the FB voltage to be equal to the reference voltage. Use 方程式 1 to determine R_{FBB} for a desired output voltage setpoint and a given value of R_{FBT}.

$$R_{FBB}[k\Omega] = \left(\frac{1V}{V_{OUT}[V] - 1V} \right) \cdot R_{FBT}[k\Omega] \quad (1)$$

While R_{FBT} is generally in the range of 10kΩ to 1MΩ, use a value of 100kΩ for improved noise immunity (relative to higher resistances such as 1MΩ) and reduced current consumption (compared to lower resistance values).

7.3.3 Precision Enable and Input Voltage UVLO (EN)

The EN input supports adjustable input undervoltage lockout (UVLO) programmed by resistor values for application-specific power-up and power-down requirements. Also, an external logic signal can be used to drive the EN input to toggle the output ON or OFF and for system sequencing or protection.

The LM644x0-Q1 enters a low-I_Q shutdown mode when EN is pulled below 0.4V. The internal LDO regulator powers off, shutting down the bias currents of the LM644x0-Q1. When the EN voltage is between the hard shutdown and the precision enable thresholds, the LM644x0-Q1 operates in standby mode with the VCC voltage in regulation. After the voltage at EN is above V_{EN-TH}, the converter begins to switch normally, provided the input voltage drives the internal VCC above the rising UVLO threshold of 3.6V (typical).

The EN pin cannot be left floating. The simplest way to enable operation is to connect the EN pin to VIN, allowing self-start-up of the LM644x0-Q1. However, many applications benefit from the use of a divider network from VIN to EN as shown in 图 7-1 , which establishes a precision input voltage UVLO. This can be used for sequencing, to prevent re-triggering of the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. Note that the precision enable threshold, V_{EN-TH}, has a 28% hysteresis to prevent ON/OFF re-triggering. An external logic output of another IC can also be used to drive EN, allowing system power sequencing.

Calculate the resistor divider values using 方程式 2. See *Input Voltage UVLO* for additional information.

$$R_{ENT}\left[k\Omega\right] = R_{ENB}\left[k\Omega\right] \cdot \left(\frac{V_{IN(on)}\left[V\right]}{V_{EN-TH}\left[V\right]} - 1 \right) \tag{2}$$

where

- $V_{IN(on)}$ is the required input voltage turn-on threshold.

7.3.4 MODE/SYNC Operation

The LM644x0-Q1 features selectable operating modes through the MODE/SYNC input pin. The LM644x0-Q1 can operate in one of three selectable modes:

- AUTO Mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation to prevent reverse current through the inductor. See 节 *7.4.3.2* for more detail.
- FPWM Mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current. See 节 *7.4.3.3* for more detail.
- SYNC Mode: The LM644x0-Q1 clock locks to an external signal applied to the MODE/SYNC pin. As long as the output voltage can be regulated at full frequency and is not limited by the minimum off time or minimum on time, the clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the LM644x0-Q1 is in SYNC mode, it operates as though in FPWM mode: diode emulation is disabled, allowing the frequency applied to the MODE/SYNC pin to be matched without an applied load at the output.

In addition, the MODE/SYNC pin can be used to activate or deactivate the spread spectrum feature of the LM644x0-Q1. The MODE/SYNC pin can be configured in two ways: level-dependent MODE/SYNC control (see 节 *7.3.4.1*) or pulse-dependent MODE/SYNC control (see 节 *7.3.4.2*).

7.3.4.1 Level-Dependent MODE/SYNC Control

If only a single mode is used, configure the converter using level-dependent control. Note that the LM644x0-Q1 cannot be synchronized to an external clock signal in level-dependent mode. 表 7-1 shows a summary of level-dependent mode selection settings. The level-dependent mode selection setting registers after expiration of t_{MODE}. 图 7-2 also depicts a summary of the level-dependent modes.

表 7-1. Level-Dependent Mode Selection Settings

MODE/SYNC	MODE
Tie to GND	AUTO mode with spread spectrum
Tie to GND through 100kΩ	AUTO mode without spread spectrum
Tie to VCC or set $V_{MODE\_H} < V_{MODE/SYNC} < V_{MODE\_H2}$	FPWM mode with spread spectrum
Tie to VIN or set $V_{MODE/SYNC} > V_{MODE\_H3}$	FPWM mode without spread spectrum

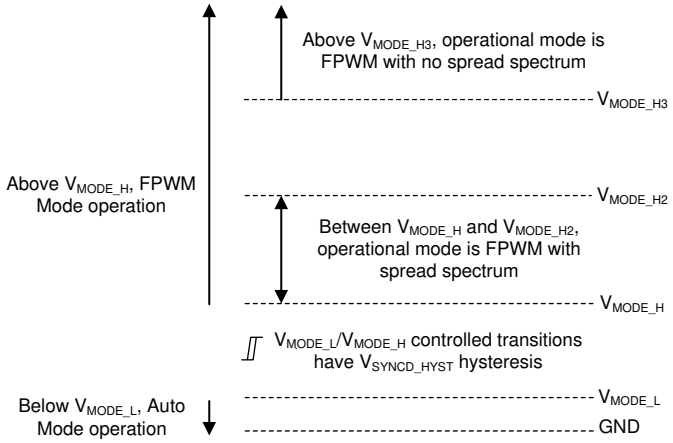


图 7-2. Level-Dependent Mode Selection Settings

Note that during dropout operation, the input voltage is close to VCC. Because this condition is typically seen while operating in dropout, the switching frequency is typically folded back and spread spectrum is deactivated. When VIN increases and the device is no longer in frequency foldback, spread spectrum is reactivated. Also, when the input voltage is between 3V to 3.7V and the LM644x0-Q1 is not in dropout operation and spread spectrum operation is not assured.

One purpose of level-dependent MODE/SYNC pin control is to dynamically change between FPWM and AUTO modes. To make sure the resistance from MODE/SYNC to ground is less than R_{SYNC_L}, use 6kΩ to ground. The MODE/SYNC pin can then be toggled between FPWM and AUTO modes as shown in 表 7-1.

If AUTO mode without spread spectrum operation is desired, tie MODE/SYNC to ground through a 100kΩ resistor. AUTO mode without spread spectrum is a fixed option, and the mode cannot be changed dynamically.

7.3.4.2 Pulse-Dependent MODE/SYNC Control

Most systems that require more than a single mode of operation from the LM644x0-Q1 are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-dependent MODE/SYNC control is useful with these systems.

To initiate pulse-dependent MODE/SYNC control, a valid synchronization signal must be applied. Upon completion of the fourth pulse in a valid synchronization pulse train, MODE/SYNC operates in pulse-dependent MODE/SYNC control mode, shown in 图 7-3 and 图 7-4. The only way to return to Level-dependent MODE/SYNC control is to restart the LM644x0-Q1.

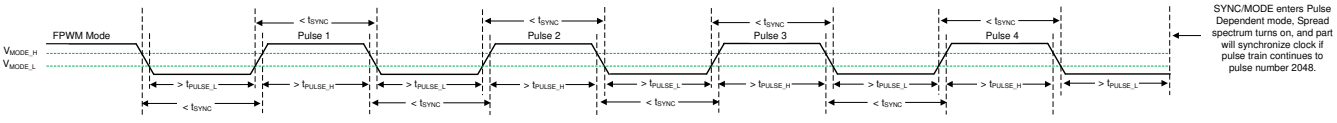


图 7-3. Transition from FPWM Mode to Pulse-Dependent Control

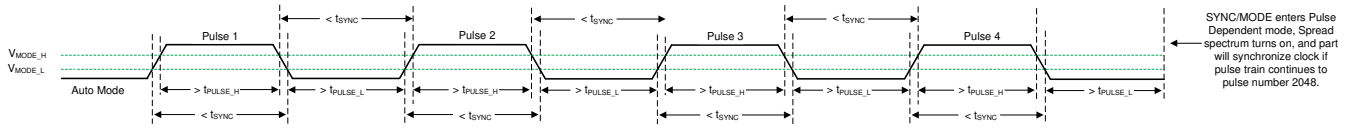


图 7-4. Transition from AUTO Mode to Pulse-Dependent Control

After Pulse-dependent MODE/SYNC control has been initiated, 表 7-2 shows a summary of the pulse-dependent mode selection settings.

表 7-2. Pulse-Dependent Mode Selection Settings

MODE/SYNC	MODE
$V_{MODE/SYNC} > V_{MODE\_H}$	FPWM mode with spread spectrum
$V_{MODE/SYNC} < V_{MODE\_L}$	AUTO mode with spread spectrum
Synchronization clock	SYNC mode without spread spectrum
$V_{MODE/SYNC} > V_{MODE\_H}$ and Double Pulse (图 7-6)	FPWM mode without spread spectrum
$V_{MODE/SYNC} < V_{MODE\_L}$ and Double Pulse (图 7-7)	AUTO mode without spread spectrum

图 7-5 shows the transition between AUTO mode and FPWM mode while in Pulse-dependent MODE/SYNC control. The LM644x0-Q1 transitions to a new mode of operation after t_{MODE} has expired.

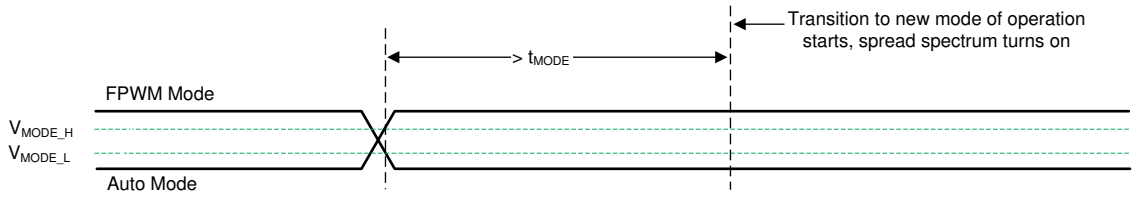


图 7-5. Transition from AUTO Mode and FPWM Mode

Two positive-going pulses can be used to turn off spread spectrum in AUTO and FPWM modes. The two positive pulses must be consistent with the characteristics of a valid sync signal. 图 7-6 through 图 7-9 show the only waveforms that result in spread spectrum being turned off. Refer to the *Electrical Characteristics* for more information about the timing specifications.

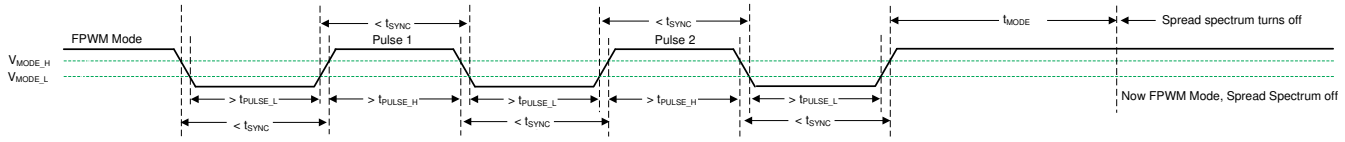


图 7-6. Spread Spectrum Disabled in FPWM Mode

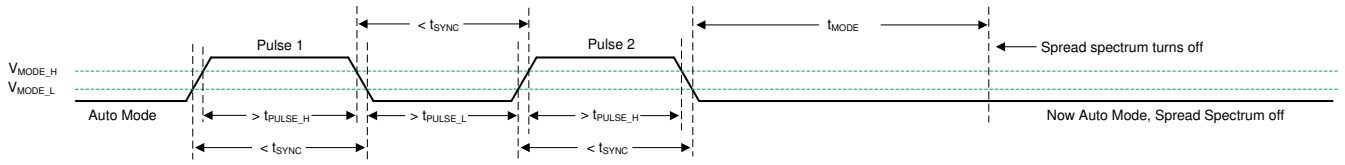


图 7-7. Spread Spectrum Disabled in AUTO Mode

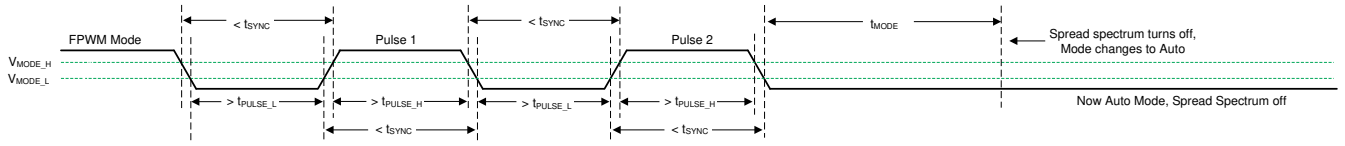


图 7-8. Spread Spectrum Disabled in Transition from FPWM Mode to AUTO Mode

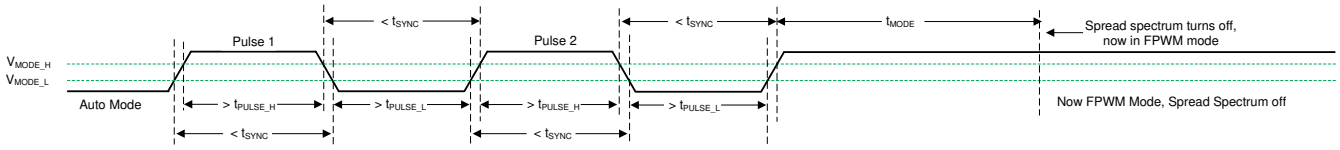


图 7-9. Spread Spectrum Disabled in Transition from AUTO Mode to FPWM Mode

To enter SYNC mode, the valid synchronization signal must be present for 2048 cycles.

If the MODE/SYNC voltage becomes constant longer than t_{MODE}, the LM644x0-Q1 enters either AUTO mode or FPWM mode. At this time, spread spectrum is turned on and MODE/SYNC operates in pulse-dependent mode.

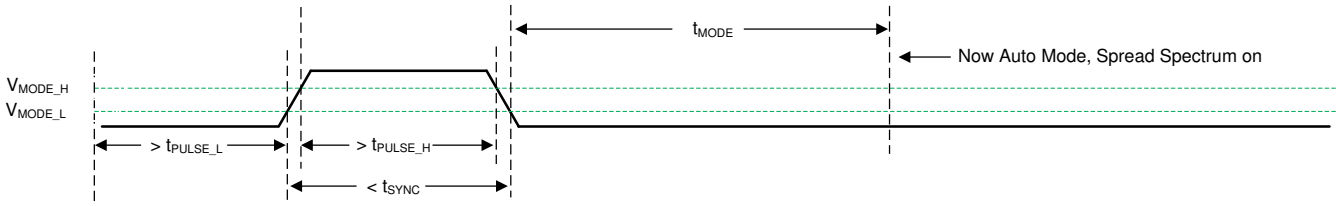


图 7-10. Transition from SYNC Mode to AUTO Mode

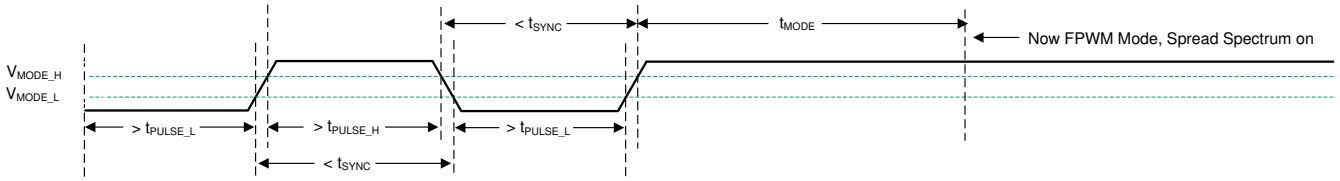
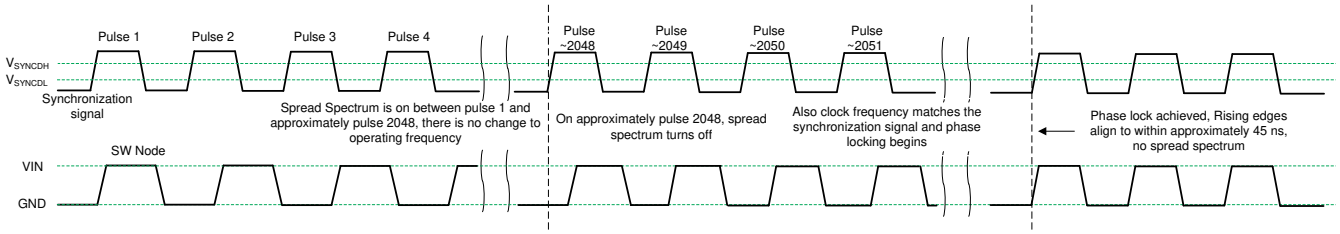


图 7-11. Transition from SYNC Mode to FPWM Mode

7.3.5 Clock Locking

A clock locking procedure initiates after a valid synchronization signal is detected. The LM644x0-Q1 receives this signal at the MODE/SYNC pin. After approximately 2048 pulses, the clock frequency completes a smooth transition to the frequency of the synchronization signal without output voltage variation. Note that when the frequency is adjusted suddenly, the phase is maintained so the clock cycle that lies between operation at the default frequency and at the synchronization frequency is of intermediate length. This action eliminates very long or very short pulses. After the frequency is adjusted, the phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising switch (SW) node pulses. See 图 7-12.



The synchronization signal is detected after four pulses. The converter is ready to synchronize after approximately 2048 pulses, and the frequency is adjusted using a glitch-free technique. Phase locking is subsequently achieved.

图 7-12. Synchronization Process

Note also that the LM644x0-Q1 turns on spread spectrum after the first edge in the synchronization pulse. See the MODE/SYNC pin description in *Pin Configuration and Functions* . Upon adjustment of the frequency at the approximate 2048th pulse, spread spectrum is turned off. Finally, if the converter runs at reduced switching frequency due to low or high input voltage or during current limit, frequency lock does not occur until the condition causing low-frequency operation has been removed.

7.3.6 Power-Good Monitor (PGOOD)

The PGOOD function is implemented to replace a discrete reset device, reducing BOM count and cost. The PGOOD voltage goes low when the feedback (FB) voltage is outside of the specified PGOOD thresholds (see 图 6-8). This can occur during current limit and thermal shutdown, as well as when disabled and during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions that are shorter than $t_{PGDFLT(fall)}$ do not trip the PGOOD flag. Refer to 图 7-13 to best understand PGOOD operation.

The PGOOD output consists of an open-drain N-channel transistor, requiring an external pullup resistor to a suitable logic supply or V_{OUT}. When EN is pulled low, the flag output is also forced low. With EN low, PGOOD remains valid as long as the input voltage is above 1V (typical).

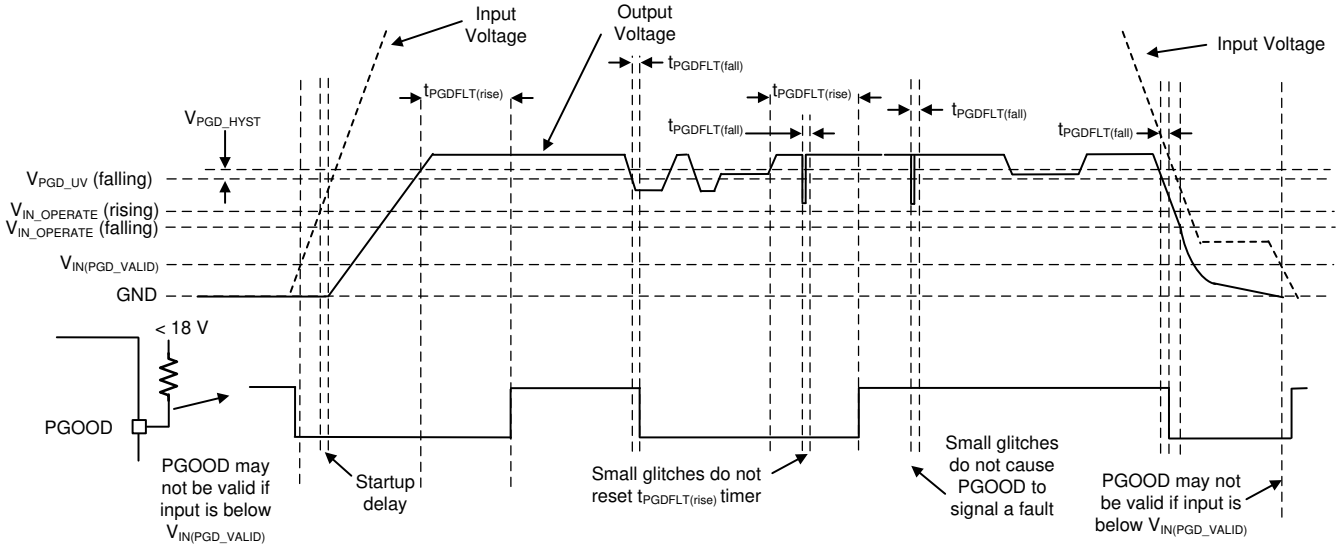


图 7-13. PGOOD Timing Diagram (Excludes OV Events)

表 7-3. Conditions That Cause PGOOD to Signal a Fault (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH $t_{PGDFLT(rise)}$ MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)(1)
$V_{OUT} < V_{OUT\text{-}target} \times PGD_{UV}$ AND $t > t_{PGDFLT(fall)}$	Output voltage in regulation: $V_{OUT\text{-}target} \times (PGD_{UV} + PGD_{HYST}) < V_{OUT} < V_{OUT\text{-}target} \times (PGD_{OV} - PGD_{HYST})$ (see 图 6-8)
$V_{OUT} > V_{OUT\text{-}target} \times PGD_{OV}$ AND $t > t_{PGDFLT(fall)}$	Output voltage in regulation
$T_J > T_{SHD}$	$T_J < T_{SHD\text{-}F}$ AND output voltage in regulation
$V_{EN} < V_{EN\text{-}TH}$ falling	$V_{EN} > V_{EN\text{-}TH}$ rising AND output voltage in regulation
$V_{CC} < V_{CC\text{-}UVLO} - V_{CC\text{-}UVLO\text{-}HYST}$	$V_{CC} > V_{CC\text{-}UVLO}$ AND output voltage in regulation

(1) As an additional operational check, PGOOD remains low during the soft-start time, which is defined as the time for the output voltage to reach the setpoint or t_{SS2} has passed since initiation (whichever is lower).

7.3.7 Bias Supply Regulator (VCC, BIAS)

VCC is the output of the internal LDO subregulator used to supply the control circuits of the LM644x0-Q1. The nominal VCC voltage is 3.3V. The BIAS pin is the input to the internal LDO. This input can be connected to V_{OUT} to provide the lowest possible input supply current. If the BIAS voltage is less than 3.1V, VIN1 and VIN2 directly power the internal LDO.

To prevent unsafe operation, VCC has UVLO protection that prevents switching if the internal voltage is too low. See $V_{CC\text{-}UVLO}$ and $V_{CC\text{-}UVLO\text{-}HYST}$ in the *Electrical Characteristics* . Note that these UVLO levels and the dropout voltage of the LDO are used to derive the minimum $V_{IN\_OPERATE}$ and $V_{IN\_OPERATE\_H}$ values.

7.3.8 Bootstrap Voltage and UVLO (CBOOT)

The gate driver of the high-side (HS) switch requires a bias voltage higher than V_{IN}. The bootstrap capacitor, C_{BOOT}, connected between CBOOT and SW, works as a charge pump to boost the voltage on CBOOT to a level of VCC above the SW voltage. The LM644x0-Q1 has an integrated bootstrap diode to minimize external component count. Use a 100nF bootstrap capacitor rated for 10V or higher. The $V_{BOOT-UVLO}$ threshold (2.1V typical) is designed to maintain proper HS switch operation. If the bootstrap capacitor voltage drops below $V_{BOOT-UVLO}$, then the converter initiates a charging sequence, turning on the low-side switch before attempting to turn on the HS switch.

7.3.9 Spread Spectrum

The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies. In most systems containing the LM644x0-Q1, low-frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of the emissions at higher harmonics that fall in the FM frequency band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LM644x0-Q1 uses a ±2% spread of frequencies, which can spread energy smoothly across the FM and TV bands but is small enough to limit subharmonic emissions below the converter switching frequency. Peak emissions at the switching frequency of the converter are only reduced slightly, by less than 1dB, while peaks in the FM band are typically reduced by more than 6dB.

Use the MODE/SYNC pin to enable or disable spread spectrum in the LM644x0-Q1. The LM644x0-Q1 uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). This intelligent pseudo-random generator limits cycle-to-cycle frequency changes to limit output ripple. The pseudo-random pattern repeats at less than 1.5Hz, which is below the audio band.

Spread spectrum is only available while the clock of the LM644x0-Q1 is free running at the natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed when operating in dropout.
- The clock is slowed at light load in AUTO mode. In FPWM mode, spread spectrum is active even if there is no load.
- At a high-input-voltage to low-output-voltage conversion ratio when the device operates at the minimum on time, the internal clock is slowed, disabling spread spectrum. Refer to the *Timing Characteristics* for more detail.
- The clock is synchronized to an external clock signal.

7.3.10 Soft Start and Recovery From Dropout

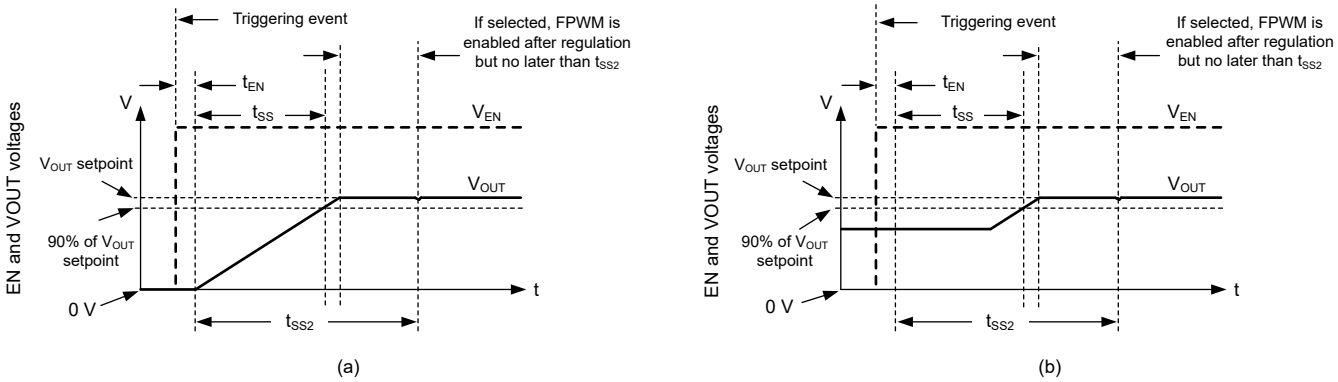
The converter uses a reference-based soft start that prevents output voltage overshoot and large inrush current during start-up. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pins of the IC, releasing UVLO.
- EN goes high to turn on the device.
- Recovery from a hiccup-waiting period
- Recovery from thermal shutdown protection

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate the output voltage is slowly ramped. The net result is that the output voltage takes t_{SS} to reach 90% of the desired value.
- The operating mode is set to AUTO, activating diode emulation. This action allows a pre-biased start-up without pulling the output voltage low if there is a voltage already present on the output.

Together, these actions provide start-up with limited inrush currents and also facilitate the use of high output capacitance and higher loading conditions that cause the peak inductor current to border on current limit during start-up without triggering hiccup. See 图 7-14.



Soft start functions with the output voltage starting from 0V in (a), or if there is already a prebiased output as shown in (b). In either case, the output voltage must reach within 10% of the setpoint within t_{SS} after soft start initiates. FPWM and hiccup are disabled during soft start, with both FPWM and hiccup enabled after the output voltage reaches regulation or after the t_{SS2} time interval expires, whichever happens first.

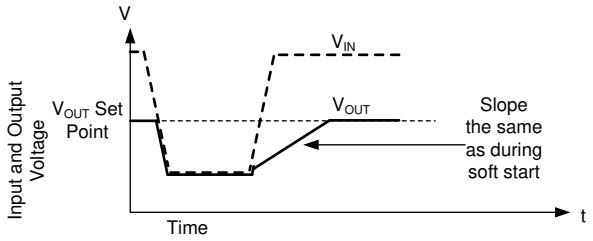
图 7-14. Soft-Start Operation

Any time the output voltage falls more than a few percent, the output voltage ramps up slowly. This condition is called recovery from dropout and differs from soft start in three important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the preset output voltage setpoint.
- Hiccup is allowed if the output voltage is less than 40% of the nominal setpoint. Note that during dropout regulation, hiccup is inhibited.
- FPWM mode is allowed during recovery from dropout. If the output voltage were to suddenly be pulled up by an external supply, the converter can pull down on the output.

Despite being called recovery from dropout, this feature is active whenever the output voltage drops to a few percent lower than the setpoint. This action primarily occurs under the following conditions:

- Dropout: When there is insufficient input voltage to maintain the desired output voltage
- Overcurrent: When there is an overcurrent event that is not severe enough to trigger hiccup



Whether the output voltage falls due to high load current or low input voltage, after the condition that causes the output to fall below the setpoint is removed, the output recovers at the same rate as during start-up. Even though hiccup does not trigger due to dropout, it can, in principle, be triggered during recovery if output voltage is below 40% of the output voltage setpoint for more than 128 clock cycles.

图 7-15. Recovery From Dropout

7.3.11 Overcurrent and Short-Circuit Protection

The converter protects from overcurrent conditions with cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs. High-side MOSFET overcurrent protection is implemented by nature of peak-current mode control. The HS switch current is sensed when the HS switch is turned on after a short blanking time. Every switching cycle, this switch current is compared to the minimum of a fixed current setpoint or the output of

the voltage regulation loop minus slope compensation. Because the voltage loop output has a maximum value and slope compensation increases with duty cycle, the HS current limit decreases with increased duty cycle when the duty cycle is above 35%. See 图 7-16.

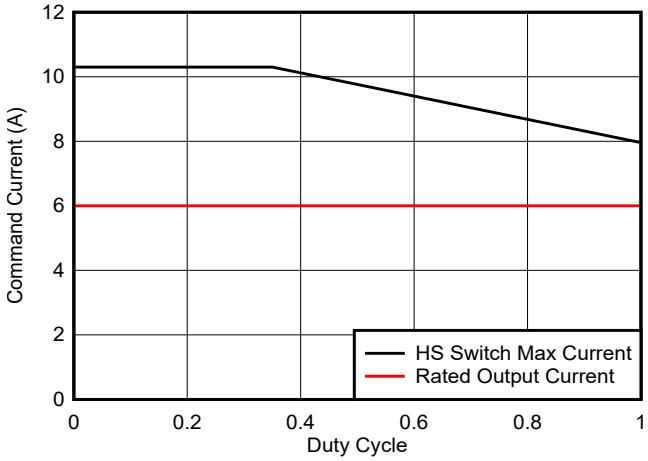


图 7-16. HS Switch Maximum Current as a Function of Duty Cycle for the LM64460-Q1

When the LS switch is turned on, the switch current is also sensed and monitored. Like the HS device, the LS switch turns off as commanded by the voltage control loop and low-side current limit. If the LS switch current is higher than I_{L-LS} at the end of a switching cycle, the switching cycle is extended until the LS current reduces below the limit. The LS switch is turned off after the LS current falls below the limit, and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

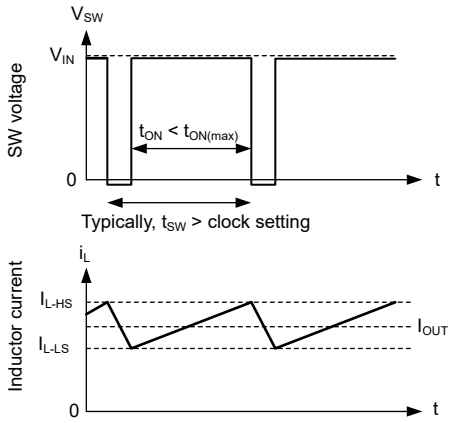


图 7-17. Current Limit Waveforms

Because the current waveform assumes values between I_{L-HS} and I_{L-LS}, the maximum output current is very close to the average of these two values. Hysteretic control is used and current does not increase as output voltage approaches zero.

The converter employs hiccup overcurrent protection if there is an extreme overload, and the following conditions are met for 128 consecutive switching cycles:

- The output voltage is below approximately 0.4 times the output voltage setpoint.
- Greater than t_{SS2} has passed since soft start has started; see *Soft Start and Recovery from Dropout* .
- The converter is not operating in dropout, which is defined as having minimum off time controlled duty cycle.

In hiccup mode, the device shuts down and attempts to soft start after t_W. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions and short circuits. See 图 7-18. After the overload is removed, the device recovers as though in soft start; see 图 7-19.

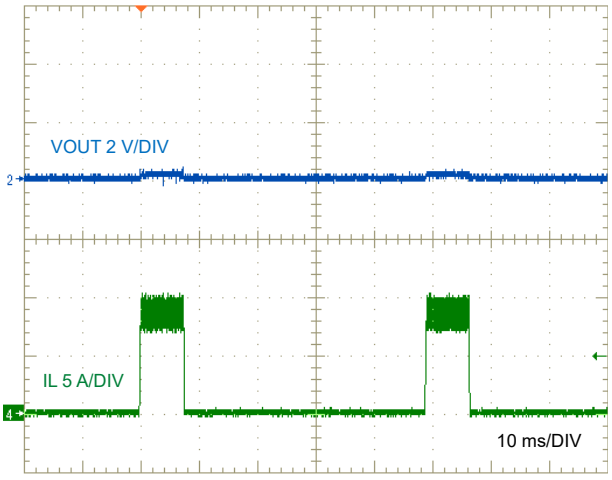


图 7-18. Inductor Current Bursts During Hiccup

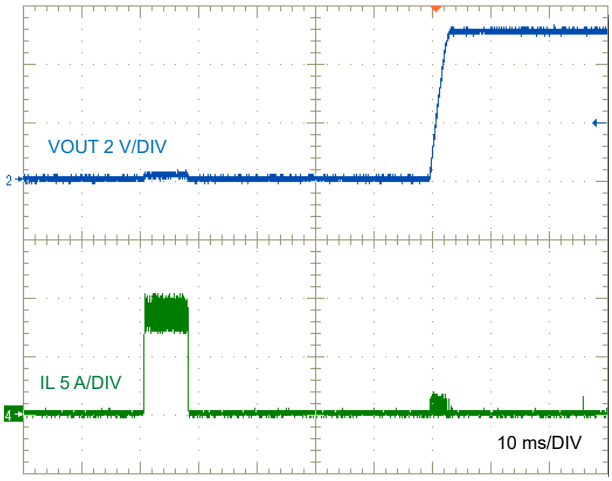


图 7-19. Short-Circuit Recovery

7.3.12 Thermal Shutdown

Thermal shutdown prevents the device from extreme junction temperatures by turning off the internal switches when the IC junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 158°C. When the junction temperature falls below 158°C (typical), the converter attempts to soft start.

While the converter is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the converter is disabled due to high junction temperature. The VCC current limit is reduced to a few milliamperes during thermal shutdown.

7.3.13 Input Supply Current

The converter is designed to have very low input supply current when regulating at light loads. This is achieved by powering much of the internal circuits from the output. The BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting BIAS to the regulator output, a small amount of current is drawn from the output. This current is reduced at the input by the ratio of V_{OUT} / V_{IN}. 方程式 3 defines the current consumed by the operating (switching) buck converter at no load:

$$I_{Q\_VIN(SW)}[\mu A] = I_{Q\_VIN}[\mu A] + I_{EN}[\mu A] + I_{DIV}[\mu A] \cdot \frac{V_{OUT}[V]}{V_{IN}[V] \cdot \eta_{eff}} \quad (3)$$

where

- I_{Q_VIN} is the current into the VIN pins – see the *Electrical Characteristics* .
- I_{EN} is current into the EN pin – see the *Electrical Characteristics* . Include this current if EN is connected to VIN. Note that this current drops to a very low value if EN connects to a voltage less than 5V.
- I_{DIV} is the current consumption of the feedback divider used to set output voltage.
- η_{eff} is the light-load efficiency when I_{Q_VIN} is removed from the input current of the buck converter. η_{eff} = 0.8 is a conservative value that can be used under normal operating conditions.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN voltage is less than 0.4V, both the regulator and the internal LDO have no output voltage. The converter is in shutdown mode, and the quiescent current drops to 0.6µA typical.

7.4.2 Standby Mode

The internal LDO has a lower enable threshold than the output of the converter. When the EN pin voltage is above 1.1V (maximum) and below the precision enable threshold, the internal LDO regulates the VCC voltage at 3.3V typical. The precision enable circuitry is ON after VCC is above the UVLO. The internal power MOSFETs remain off unless the voltage on EN goes above the precision enable threshold. The converter also employs UVLO protection. If the VCC voltage is below the UVLO level, the output of the converter is turned off.

7.4.3 Active Mode

The converter is in active mode whenever the EN voltage is above the threshold voltage, V_{IN}, is high enough to satisfy $V_{IN\_OPERATE}$, and no other fault conditions are present. The simplest way to enable operation is to connect EN to VIN, which allows self start-up when the applied input voltage exceeds the minimum $V_{IN\_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the converter is in one of five modes:

- Continuous conduction mode (CCM) with fixed switching frequency when the load current is above half of the inductor current ripple.
- AUTO mode – Light-load operation with PFM where the switching frequency decreases at very light load.
- FPWM mode – Light-load operation that maintains constant switching frequency across the full load range.
- Minimum on time: The switching frequency reduces to maintain regulation with high step-down conversion ratios, that is, high input voltage to low output voltage.
- Dropout mode: The switching frequency reduces to minimize the dropout voltage.

7.4.3.1 CCM Mode

The following operating description of the converter refers to the *Functional Block Diagram* and to the waveforms in 图 7-20. In CCM, the converter supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on time, the SW voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces V_{SW} to swing below ground by the voltage drop across the LS switch. The control loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = t_{ON} / t_{SW} \quad (4)$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (5)$$

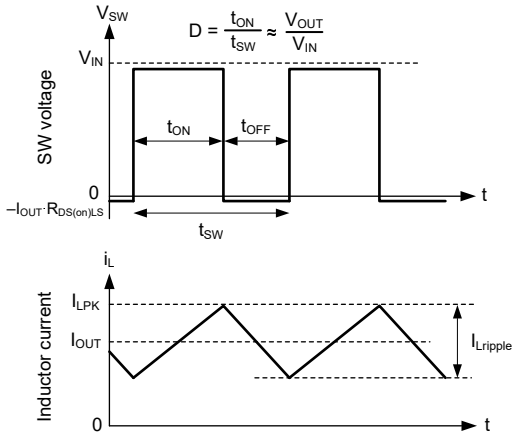


图 7-20. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

7.4.3.2 AUTO Mode – Light-Load Operation

The converter can have two behaviors while lightly loaded. AUTO mode operation allows for a seamless transition between normal current-mode operation while heavily loaded and in highly efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the converter operates in depends on the configuration of the MODE/SYNC pin. See 表 7-1 . When using the LM64460-Q1, select the light-load behavior using the MODE/SYNC pin. Note that the converter operates in FPWM mode when synchronizing frequency to an external clock signal.

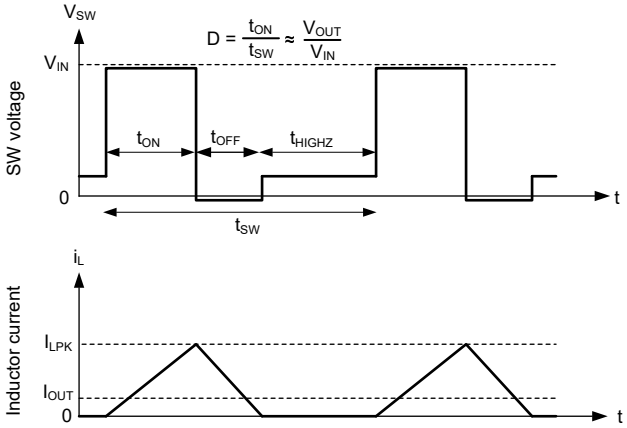
In AUTO mode, the converter employs two techniques to improve efficiency during light-load operation:

- Diode emulation, which allows DCM operation
- Switching frequency reduction

Note that while these two features operate together to create excellent light-load behavior, the features operate independently of each other.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor, which requires a lower frequency to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



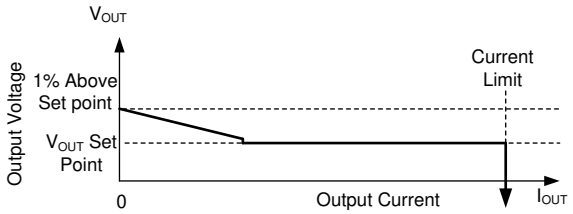
In AUTO mode, the low-side MOSFET is turned off after the inductor current is near zero. As a result, after the output current is less than half of what the inductor ripple is in CCM, the converter operates in DCM and diode emulation is active.

图 7-21. PFM Mode Operation at Light Loads

The converter has a minimum peak inductor current setting while operating in AUTO mode. After current is reduced to a low value with fixed input voltage, the on time remains constant. Regulation is then achieved by adjusting the switching frequency. This mode of operation is called PFM mode regulation.

7.4.3.2.2 Frequency Foldback

The converter reduces the switching frequency whenever the output voltage is higher than the setpoint. This function is enabled whenever COMP, an internal signal, is low and there is an offset between the FB regulation setpoint and the voltage applied at FB. The net effect is that there is a larger output impedance while lightly loaded in AUTO mode than in normal operation. The output voltage is approximately 1% high when the converter is completely unloaded.



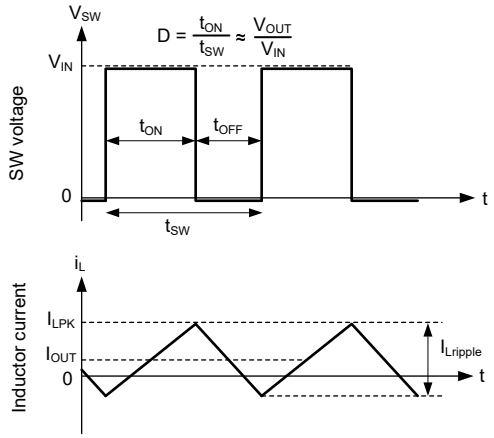
In AUTO mode, after the output current drops below approximately 1/10th the rated current of the converter, the output resistance increases so that output voltage is 1% high while the converter is completely unloaded.

图 7-22. Steady-State Output Voltage Versus Output Current in AUTO Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, use a dummy load at the output or select FPWM mode to reduce or eliminate this offset.

7.4.3.3 FPWM Mode – Light-Load Operation

Like AUTO mode operation, select FPWM operation using the MODE/SYNC pin. FPWM applies by default during synchronization. In FPWM mode, the switching frequency is maintained constant while lightly loaded by allowing negative current to flow in the inductor. Negative current is limited to –3A for LM64460-Q1 and –2A for LM64440-Q1 devices by a reverse current limit circuit.



In FPWM mode, continuous conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

图 7-23. FPWM Mode Operation

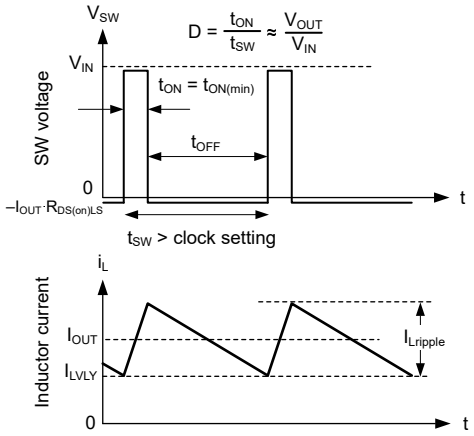
Transitions between AUTO mode and FPWM mode can be commanded during operation. Such transitions are gradual, taking tens of clock cycles, allowing minimal disruption of the output voltage during transitions. If the

load is heavy enough to operate in CCM, because operation is identical in FPWM and AUTO modes, no change in behavior is visible until the next time the circuit is lightly loaded.

Frequency reduction is still available in FPWM mode if the output voltage is high enough to command minimum on time even while lightly loaded, allowing good behavior during faults that involve the output being pulled up.

7.4.3.4 Minimum On-Time (High Input Voltage) Operation

The converter continues to regulate the output voltage even if the input-to-output voltage ratio requires an on time less than the minimum on time of the converter with a given clock setting. This is accomplished using valley current control as shown in 图 7-24.



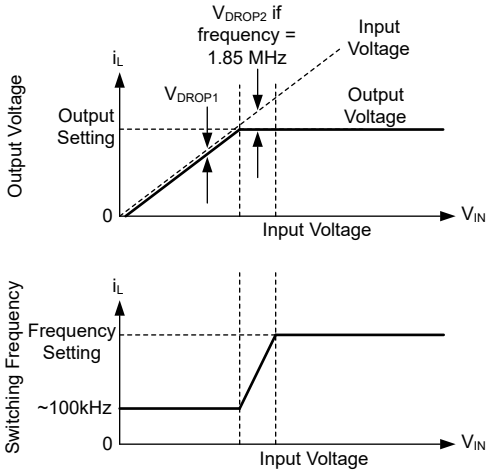
In valley control mode, the inductor valley current is regulated, not inductor peak current.

图 7-24. Valley Current Operation

At all times, the compensation circuit dictates maximum peak and valley inductor currents. If for any reason, the valley current setpoint is exceeded, the clock cycle is extended until the valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate solely using peak current. If the input-to-output voltage ratio is too high, even though current exceeds the peak value dictated by compensation, the high-side switch cannot be turned off quickly enough to regulate the output voltage. As a result, the compensation circuit reduces both peak and valley currents. After a low enough current is established, the valley inductor current matches that being commanded by the compensation circuit. Under these conditions, the low-side switch is kept on and the next clock cycle is delayed until the inductor current drops below the desired valley current threshold. Because the on time is fixed at the minimum value, this type of operation resembles that of a device using a constant on-time (COT) control scheme.

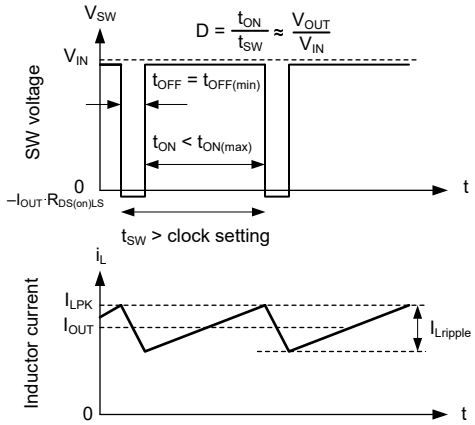
7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires the switching frequency to decrease to achieve the required duty cycle. At a given clock frequency, the duty cycle is limited by the converter minimum off time. After this limit is reached, if the clock frequency were maintained, the output voltage falls. Instead of allowing the output voltage to drop, the converter extends on time past the end of the clock cycle until the required peak inductor current is achieved. The clock is allowed to start a new cycle after the required peak inductor current is reached or after a pre-determined maximum on time, $t_{ON(max)}$, of approximately 9 µs passes. As a result, after the required duty cycle cannot be achieved at the selected clock frequency due to the minimum off-time requirement, the switching frequency decreases to maintain regulation. If the input voltage is low enough such that output voltage cannot be regulated even with an on time of $t_{ON(max)}$, the output voltage drops to slightly below the input voltage, V_{DROP1}. See the *Systems Characteristics* . Refer to 图 7-15 for additional information on recovery from dropout.



Output voltage and switching frequency vs. input voltage: if there is little difference between the input voltage and output voltage setpoint, the converter reduces switching frequency to maintain regulation. If the input voltage is too low to provide the desired output voltage at approximately 110kHz, the output voltage tracks the input voltage.

图 7-25. Switching Frequency and Output Voltage in Dropout



The inductor current takes longer than a normal clock period to reach the desired peak value, and consequently the switching frequency decreases to maintain regulation. This frequency reduction is limited by $t_{ON(max)}$.

图 7-26. Dropout Waveforms

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The LM64440-Q1 and LM64460-Q1 are synchronous buck converters that requires only a few external components to convert from a wide range of supply voltages to a fixed output voltage at an output current up to 6A. A comprehensive LM64440-Q1 or LM64460-Q1 quickstart calculator is available by download to expedite and streamline the process of designing of a LM64440-Q1 or LM64460-Q1 -based regulator circuit.

8.2 Typical Applications

For the circuit schematics, bill of materials, PCB layout files, and test results of an LM644x0-Q1 implementation, see the LM64460-Q1 EVM.

8.2.1 Design 1 – Automotive Synchronous 6A Buck Regulator at 2.1MHz

图 8-1 shows the schematic diagram of a synchronous buck regulator with an output voltage set at 5V and a rated load current of 6A. In this example, the target half-load and full-load efficiencies are 94.5% and 92.5%, respectively, based on a nominal input voltage of 13.5V that ranges from 5V to 36V. The switching frequency is set at the default 2.1MHz of the LM64460-Q1. The BIAS input is connected to the 5V output, thus reducing IC bias power dissipation and improving efficiency performance. Connecting MODE/SYNC to GND configures the LM64460-Q1 for AUTO mode with spread spectrum enabled.

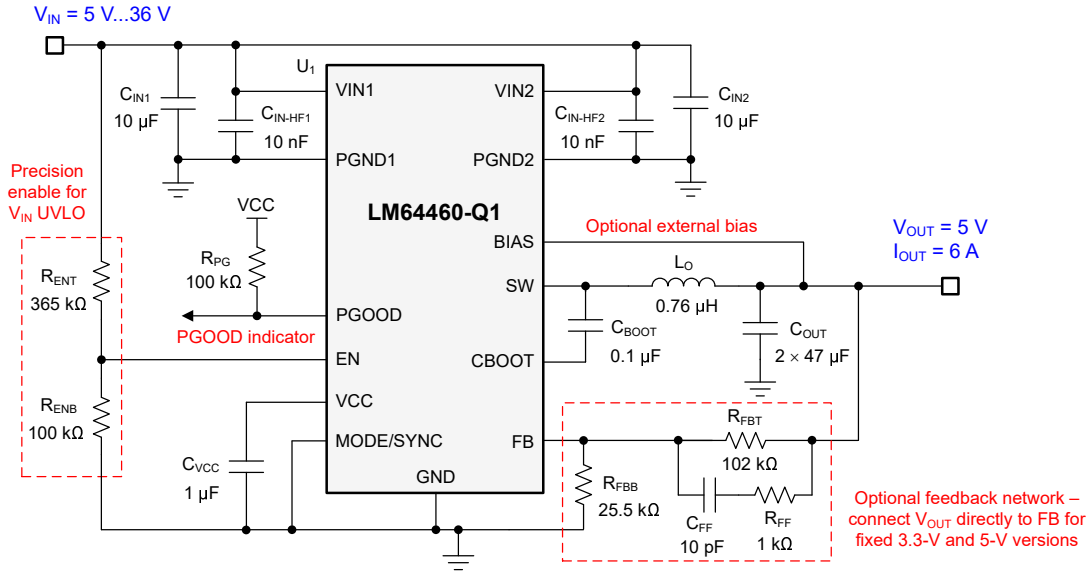


图 8-1. Application Circuit 1 – 5V, 6A at 2.1MHz

备注

This application example is provided herein to showcase the LM64460-Q1 buck converter in several different implementation scenarios. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input for stability, particularly at low input voltage and high output current operating conditions. See the *Power Supply Recommendations* for more detail.

8.2.1.1 Design Requirements

表 8-1 shows the intended input, output, and performance parameters for this application example. The converter operates in dropout during cold crank when the input voltage decreases to 5V, with the output voltage slightly below the 5V setpoint.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (for constant f_{SW})	6V to 18V
Minimum transient input voltage, cold crank	5V
Maximum transient input voltage, load dump	36V
Output voltage and full-load current	5V, 6A
Switching frequency	2.1MHz
IC input current, no-load	< 10µA
IC shutdown current	< 1µA

表 8-2 gives the selected buck converter power-stage components with availability from multiple vendors. This design uses a low-DCR inductor and all-ceramic output capacitor implementation.

表 8-2. List of Materials for Application Circuit 1

REF DES	QTY	SPECIFICATION		VENDOR (1)	PART NUMBER
C_{IN}	2	10µF, 50V, X7R, 1206, ceramic, AEC-Q200		Samsung	CL31Y106KBKVPNE
				TDK	CGA5L1X7R1H106K
		10µF, 50V, X7S, 1210, ceramic, AEC-Q200		Murata	GCM32EC71H106KA03
				TDK	CGA6P3X7S1H106M
C_{OUT}	2	47µF, 6.3V, X7R, 1210, ceramic, AEC-Q200		Murata	GCM32ER70J476KE19L
		47µF, 10V, X7S, 1210, ceramic, AEC-Q200		TDK	CGA6P1X7S1A476M
				Murata	GCM32EC71A476KE02
	3	22µF, 16V, X7R, 1210, ceramic, AEC-Q200		TDK	CGA6P1X7R1C226M
L_O	1	0.76µH, 4.9mΩ, 11.8A, 4.0mm × 4.0mm × 3.1mm, AEC-Q200		Coilcraft	XGL4030-761MEC
		1µH, 9.1mΩ, 7.9A, 4.2mm × 4.0mm × 2.1mm, AEC-Q200		Cyntec	VCHA042A-1R0M
		1µH, 9.6mΩ, 14.7A, 5.3mm × 5.1mm × 3.0mm, AEC-Q200		TDK	SPM5030VT-1R0M-D
		1µH, 12mΩ, 11.6A, 4.1mm × 4.1mm × 3.1mm, AEC-Q200		Würth Electronik	74438357010
U_1	1	LM64460-Q1 synchronous buck converter, AEC-Q100	Adjustable	Texas Instruments	LM64460APPQRYFRQ1
			Fixed 5V		LM64460CPPQRYFRQ1

(1) See the *Third-Party Products Disclaimer*.

More generally, the LM64460-Q1 converter is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of buck inductance and output capacitance. As a starting point, 表 8-3 provides typical component values for several common application configurations.

表 8-3. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L_O (µH)	$C_{OUT-EFF(min)}$ (µF)	Typical C_{OUT} Components (1210, X7R)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF} (pF)	R_{FF} (kΩ)
2100	3.3	0.68	50	3 × 47µF, 6.3V or 4 × 22µF, 16V	100	43.2	10	1
2100	5	0.76	30	2 × 47µF, 10V or 3 × 22µF, 16V	100	24.9	10	1
400	1.8	2.2	120	3 × 100µF, 4V	80.6	100	22	1
400	3.3	3.3	70	3 × 47µF, 6.3V or 5 × 22µF, 16V	100	43.2	15	1
400	5	4.7	50	3 × 47µF, 10V or 4 × 22µF, 16V	100	24.9	15	1

表 8-3. Typical External Component Values（续）

f_{SW} (kHz)	V_{OUT} (V)	L_O (µH)	$C_{OUT-EFF(min)}$ (µF)	Typical C_{OUT} Components (1210, X7R)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF} (pF)	R_{FF} (kΩ)
400	12	6.8	20	3 × 22µF, 25V	100	9.09	4.7	1

Note that the minimum output capacitances listed in 表 8-3 represents *effective* values for ceramic capacitors derated for DC bias voltage and temperature.

8.2.2 Design 2 – Automotive Synchronous 4A Buck Regulator at 2.1MHz

图 8-2 shows the schematic diagram of a synchronous buck regulator with an output voltage set at 5V and a rated load current of 4A. In this example, the target half-load and full-load efficiencies are 94.25% and 94%, respectively, based on a nominal input voltage of 13.5V that ranges from 5V to 36V. The switching frequency is set at the default 2.1MHz of the LM64440-Q1. The BIAS input is connected to the 5V output, thus reducing IC bias power dissipation and improving efficiency performance. Connecting MODE/SYNC to GND configures the LM64440-Q1 for AUTO mode with spread spectrum enabled.

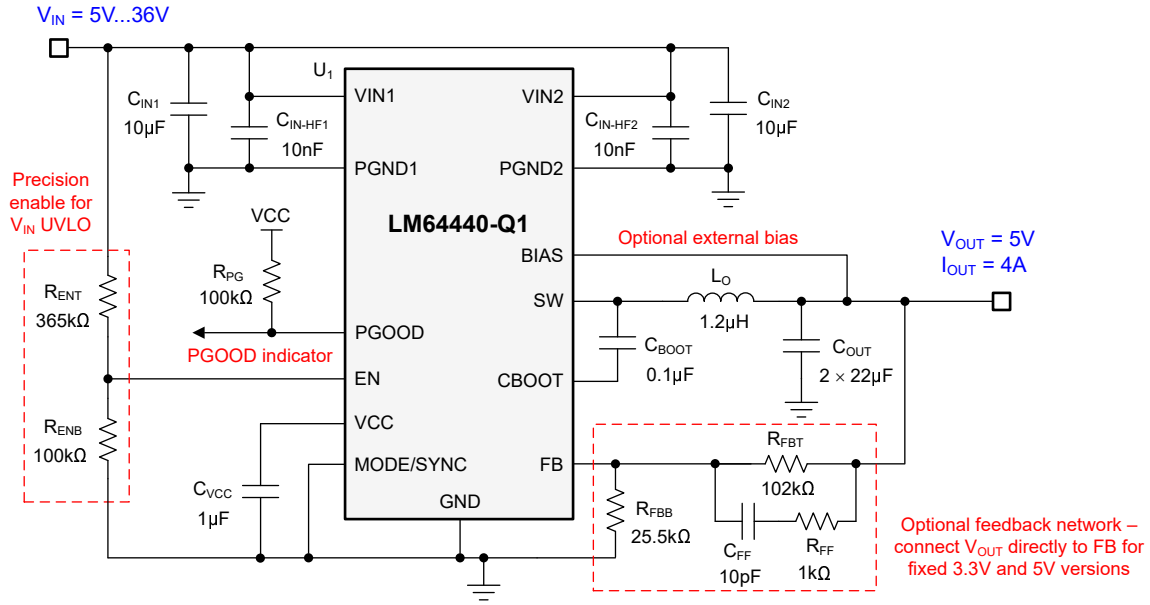


图 8-2. Application Circuit 2 – 5V, 4A at 2.1MHz

备注

This application example is provided herein to showcase the LM64440-Q1 buck converter in several different implementation scenarios. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input for stability, particularly at low input voltage and high output current operating conditions. See the *Power Supply Recommendations* for more detail.

8.2.2.1 Design Requirements

The following table shows the intended input, output, and performance parameters for this application example. The converter operates in dropout during cold crank when the input voltage decreases to 5V, with the output voltage slightly below the 5V setpoint.

表 8-4. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (for constant f_{SW})	6V to 18V
Minimum transient input voltage, cold crank	5V
Maximum transient input voltage, load dump	36V

表 8-4. Design Parameters（续）

DESIGN PARAMETER	VALUE
Output voltage and full-load current	5V, 4A
Switching frequency	2.1MHz
IC input current, no-load	< 10μA
IC shutdown current	< 1μA

The following table gives the selected buck converter power-stage components with availability from multiple vendors. This design uses a low-DCR inductor and all-ceramic output capacitor implementation.

表 8-5. List of Materials for Application Circuit 2

REF DES	QTY	SPECIFICATION		VENDOR (1)	PART NUMBER
C_{IN}	2	10μF, 50V, X7R, 1206, ceramic, AEC-Q200		Samsung	CL31Y106KBKVPNE
				TDK	CGA5L1X7R1H106K
		10μF, 50V, X7S, 1210, ceramic, AEC-Q200		Murata	GCM32EC71H106KA03
				TDK	CGA6P3X7S1H106M
C_{OUT}	1	47μF, 10V, X7S, 1210, ceramic, AEC-Q200		Murata	GCM32EC71A476KE02
				TDK	CGA6P1X7S1A476M
	2	22μF, 16V, X7S, 1206, ceramic, AEC-Q200		Murata	GCM31CC71C226ME36
L_O	1	1.2μH, 8.7mΩ, 8.2A, 4.0mm × 4.0mm × 2.5mm, AEC-Q200		Coilcraft	XGL4025-122MEC
		1.5μH, 13.4mΩ, 6.2A, 4.2mm × 4.0mm × 2.1mm, AEC-Q200		Cyntec	VCHA042A-1R5MS62M
		1.5μH, 14.1mΩ, 12.7A, 5.3mm × 5.1mm × 3.0mm, AEC-Q200		TDK	SPM5030VT-1R5M-D
		1.2μH, 13.4mΩ, 11.6A, 4.1mm × 4.1mm × 3.1mm, AEC-Q200		Würth Electronik	74438357012
U_1	1	LM64440-Q1 synchronous buck converter, AEC-Q100	Adjustable	Texas Instruments	LM64440APPQRYFRQ1
			Fixed 5V		LM64440CPPQRYFRQ1

(1) See the *Third-Party Products Disclaimer*.

More generally, the LM64440-Q1 converter is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of buck inductance and output capacitance. As a starting point, the following table provides typical component values for several common application configurations.

表 8-6. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L_O (μH)	$C_{OUT-EFF(min)}$ (μF)	TYPICAL C_{OUT} COMPONENTS (1210)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF} (pF)	R_{FF} (kΩ)
2100	3.3	0.68	30	2 × 22μF, 10V (X7R) or 1 × 47μF, 10V (X7S)	100	43.2	10	1
2100	5	0.82	20	1 × 47μF, 10V (X7S)	100	24.9	10	1
400	1.8	3.3	150	4 × 100μF, 4V (X7R)	80.6	100	47	1
400	3.3	4.7	75	2 × 47μF, 10V (X7S) or 4 × 22μF, 10V (X7R)	100	43.2	33	1
400	5	6.8	40	2 × 47μF, 10V (X7S) or 3 × 22μF, 16V (X7S)	100	24.9	22	1
400	12	8.2	20	2 × 22μF, 25V (X7S)	100	9.09	15	1

Note that the minimum output capacitances listed in 表 8-6 represents *effective* values for ceramic capacitors derated for DC bias voltage and temperature.

8.2.2.2 Detailed Design Procedure

The following design procedure applies to either schematic of 图 8-1 or 图 8-2.

8.2.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM64440-Q1 or LM64460-Q1 converter with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2.2 Setting the Output Voltage

The adjustable output voltage version of the LM64440-Q1 or LM64460-Q1 uses a feedback divider network to set the output voltage. The divider network comprises top and bottom feedback resistors designated as R_{FBT} and R_{FBB}, respectively. The resistances of the feedback divider are a compromise between excessive noise pickup and quiescent current consumption. Lower resistance values reduce noise sensitivity but also impact light-load efficiency. The recommended value for R_{FBT} is 100kΩ with a maximum value of 1MΩ. If 1MΩ is selected for R_{FBT}, then use a feedforward capacitor in parallel to provide adequate loop phase margin. Use 方程式 1 to find R_{FBB} for a given value of R_{FBT}. Choosing R_{FBT} and R_{FBB} values of 102kΩ and 25.5kΩ, respectively, sets the output voltage at exactly 5V.

With the 3.3V or 5V fixed-output version of the LM64440-Q1 or LM64460-Q1, connect FB directly to the output voltage node, preferably near the output capacitor. If the feedback point is located further away from the output capacitors (that is, remote sensing), place a small 100nF capacitor at the sensing point.

8.2.2.2.3 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses, resulting in higher system efficiency and less power dissipated in the converter. However, higher switching frequency enables the use of smaller inductors and capacitors, enabling a more compact design.

Many automotive applications require that the AM radio band be strictly avoided. Such applications tend to operate at either 2.1MHz or 400kHz, above and below the AM band, respectively. To achieve small design size for either LM64440-Q1 or LM64460-Q1, choose the default switching frequency of 2.1MHz for this application example.

8.2.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current, which is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage. For systems with a variable input voltage such as the 12V automotive battery, 25% is commonly used.

When selecting the ripple current for applications with lower maximum load than the maximum available from the device, the maximum device current must still be used. For the 4A device, use 方程式 6 to determine the value of inductance. The constant K is the percentage of peak-to-peak inductor current ripple to rated output current. Choose K = 0.3 for this 5V, 4A, 2.1MHz example, resulting in an inductance of approximately 1.2µH.

$$L_O[\mu H] = \frac{V_{IN}[V] - V_{OUT}[V]}{f_{SW}[MHz] \cdot K \cdot I_{OUT(max)}[A]} \cdot \frac{V_{OUT}[V]}{V_{IN}[V]} = \frac{13.5\,V - 5\,V}{2.1\,MHz \cdot 0.3 \cdot 4\,A} \cdot \frac{5\,V}{13.5\,V} = 1.25\mu H \quad (6)$$

For the 6A device, use 方程式 7 to determine the value of inductance. The constant K is the percentage of peak-to-peak inductor current ripple to rated output current. Choose K = 0.3 for this 5V, 6A, 2.1MHz example, resulting in an inductance of approximately 0.8µH.

$$L_O[\mu H] = \frac{V_{IN}[V] - V_{OUT}[V]}{f_{SW}[MHz] \cdot K \cdot I_{OUT(max)}[A]} \cdot \frac{V_{OUT}[V]}{V_{IN}[V]} = \frac{13.5\,V - 5\,V}{2.1\,MHz \cdot 0.3 \cdot 6\,A} \cdot \frac{5\,V}{13.5\,V} = 0.83\mu H \quad (7)$$

The saturation current rating of the inductor must be higher than the high-side switch current limit, $I_{L\text{-}HS}$ (see the *Electrical Characteristics*). These requirements prevent inductor saturation during an overload condition on the output. While an output short-circuit condition causes the LM64440-Q1 or LM64460-Q1 to enter hiccup mode, an overload condition can hold the output current at current limit without triggering hiccup. When the inductor core material saturates, the inductance can fall to a low value, causing the inductor current to rise rapidly. Although the valley current limit, $I_{L\text{-}LS}$, reduces the risk of current runaway, a saturated inductor causes the instantaneous current to increase to a high value. This can lead to component damage, avoiding inductor saturation is crucial.

Inductors with a ferrite core material have hard saturation characteristics but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, powdered iron cores typically have higher core losses at frequencies above 1MHz.

To avoid subharmonic oscillation, the inductance value must not be less than that given by 方程式 8. The maximum inductance is limited by the minimum current ripple required for current-mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the converter maximum rated current under nominal conditions.

$$L_O[\mu H] \geq 0.32 \cdot \frac{V_{OUT}[V]}{f_{SW}[MHz]} \quad (8)$$

方程式 8 assumes that this design must operate with the input voltage near or in dropout. Use 方程式 9 instead if the minimum input voltage for a given design is high enough to limit the duty cycle to less than 40%.

$$L_O[\mu H] \geq 0.2 \cdot \frac{V_{OUT}[V]}{f_{SW}[MHz]} \quad (9)$$

8.2.2.2.5 Output Capacitor Selection

The value of the output capacitor and the ESR determine the output voltage ripple and load transient performance. The output capacitor is usually determined by load transient and stability requirements rather than the output voltage ripple. For LM64440-Q1, use 表 8-7 and for LM64460-Q1, use 表 8-8 to select the output capacitance and C_{FF} feedforward capacitance values for a few common applications. Use a 1kΩ R_{FF} in series with C_{FF} to further improve noise performance.

表 8-7. Recommended Output Capacitors and C_{FF} Values for LM64440-Q1

CONFIGURATION	3.3V OUTPUT		5V OUTPUT	
	C_{OUT}	C_{FF}	C_{OUT}	C_{FF}
2.1MHz – Ceramic	3 × 22µF, 16V ceramic	10pF	2 × 47µF, 10V ceramic	10pF
2.1MHz – Alternative	2 × 22µF, 16V ceramic + 47µF, 10mΩ electrolytic	–	2 × 47µF, 10V ceramic + 47µF, 10mΩ electrolytic	–
400kHz – Ceramic	4 × 22µF, 16V ceramic	33pF	2 × 47µF, 10V ceramic	22pF

表 8-7. Recommended Output Capacitors and C_{FF} Values for LM64440-Q1 （续）

CONFIGURATION	3.3V OUTPUT		5V OUTPUT	
	C_{OUT}	C_{FF}	C_{OUT}	C_{FF}
400kHz – Alternative	1 × 22µF, 16V ceramic + 100µF, 10mΩ electrolytic	15pF	1 × 47µF, 10V ceramic + 47µF, 10mΩ electrolytic	10pF

表 8-8. Recommended Output Capacitors and C_{FF} Values for LM64460-Q1

CONFIGURATION	3.3V OUTPUT		5V OUTPUT	
	C_{OUT}	C_{FF}	C_{OUT}	C_{FF}
2.1MHz – Ceramic	4 × 22µF, 16V ceramic	10pF	2 × 47µF, 10V ceramic	10pF
2.1MHz – Alternative	2 × 22µF, 16V ceramic + 100µF, 10mΩ electrolytic	–	2 × 47µF, 10V ceramic + 100µF, 10mΩ electrolytic	–
400kHz – Ceramic	5 × 22µF, 16V ceramic	15pF	3 × 47µF, 10V ceramic	15pF
400kHz – Alternative	2 × 22µF, 16V ceramic + 100µF, 10mΩ electrolytic	–	1 × 47µF, 10V ceramic + 100µF, 10mΩ electrolytic	–

备注

Most ceramic capacitors deliver less capacitance than the rating of the capacitor indicates. Be sure to check selected capacitors for initial accuracy, temperature derating, and particularly voltage derating. 表 8-7 and 表 8-8 assumes typical derating for X7R-dielectric capacitors. If lower voltage or lower temperature-rated capacitors are used, more capacitance than listed can be required.

More conveniently, 方程式 10 calculates the required effective ceramic capacitance for a given application:

$$C_{OUT}[\mu F] \simeq \frac{14000}{F_C[kHz] \cdot V_{OUT}[V]} \tag{10}$$

where F_C is the target loop crossover frequency in units of kHz, which can be set at 10% to 15% of switching frequency and up to a maximum of 100kHz.

This example requires improved transient performance, resulting in two 47µF, 10V, X7R ceramics as the output capacitance and 10pF for C_{FF}. An alternative configuration is to use a low-ESR electrolytic capacitor in parallel with a reduced ceramic capacitance.

8.2.2.2.6 Input Capacitor Selection

Input capacitors are necessary to limit the input ripple voltage of the converter due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. 方程式 11 gives the input capacitor RMS current, where D = V_{OUT}/V_{IN} is the converter duty cycle. The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the capacitors must be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \cdot \left(I_{OUT}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \tag{11}$$

Ideally, the DC and AC components of input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} – I_{IN}) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, 方程式 12 gives the peak-to-peak ripple voltage amplitude:

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \quad (12)$$

方程式 13 gives the input capacitance required for a particular load current:

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \quad (13)$$

where

- ΔV_{IN} is the input voltage ripple specification.

The Enhanced HotRod QFN package of the LM64440-Q1 and LM64460-Q1 provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. The converter requires a minimum of two 4.7µF ceramic input capacitors, preferably with X7R or X7S dielectric and in 1206 or 1210 footprint. In this example, place two 10 µF, 50V ceramic capacitors in a symmetrical layout immediately adjacent to the converter – one at each input-to-ground pin pair: [VIN1, PGND1] and [VIN2, PGND2].

Install additional capacitance for automotive applications to meet conducted EMI specifications, such as CISPR 25 Class 5 (that limits EMI over a frequency range from 150kHz to 108MHz). For example, place a 10nF, 0402 ceramic capacitor at each input-to-ground pin pair immediately adjacent to the converter. These capacitors minimize the parasitic inductance in the switching loops and can suppress switch-node voltage overshoot and ringing, which reduces high-frequency EMI. The two 10nF capacitors, designated as C_{IN-HF1} and C_{IN-HF2} in 图 8-1 or 图 8-2, must be rated at 50V with an X7R or better dielectric.

As discussed in 节 8.3, a moderate-ESR electrolytic bulk capacitance (68µF to 100µF) at the input in parallel with the ceramics provides low-frequency filtering and parallel damping to mitigate the effects of input parasitic inductance resonating with the low-ESR, high-Q ceramic input capacitors. This is especially true if long leads or traces are used to connect the input supply to the converter.

8.2.2.2.7 Bootstrap Capacitor

The LM64440-Q1 and LM64460-Q1 requires a bootstrap capacitor connected between the CBOOT and SW pins. This capacitor stores energy that is used to supply the gate driver for the integrated high-side power MOSFET. Use a 100nF, X7R-dielectric, ceramic capacitor rated for at least 10V.

8.2.2.2.8 VCC Capacitor

The VCC pin is the output of the internal LDO subregulator used to supply the control circuits of the converter. Connect a 1 µF, 16V ceramic capacitor from VCC to AGND for proper operation. In general, avoid loading VCC with any external circuitry. However, VCC can be used as the pullup supply for the PGOOD indicator – a 100kΩ pullup resistor is a good choice in this case. Note that VCC remains high when $V_{EN-WAKE} < V_{EN} < V_{EN-TH}$. The nominal VCC voltage is 3.3V. Do not short VCC to ground or connect to an external voltage.

8.2.2.2.9 BIAS Power Connection

Because the output voltage is 5V in this design, connect the BIAS pin to V_{OUT} to reduce the VCC LDO power loss. The output voltage is supplying the LDO current instead of the input voltage. The power saving is I_{VCC} × (V_{IN} – V_{OUT}). The power saving is more significant when V_{IN} is much higher than V_{OUT} and at high switching frequencies. To prevent output voltage noise and transients from coupling to BIAS, add a series resistor between 1Ω and 10Ω between V_{OUT} and BIAS. In addition, add a bypass capacitor with a value of 1 µF or higher close to the BIAS pin to filter noise. Note the maximum allowed voltage on BIAS is 16V.

8.2.2.2.10 Feedforward Network

Use a feedforward capacitor, C_{FF}, to improve the phase margin and transient response of converter circuits that have low-ESR output capacitors. Because this capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, connect a 1kΩ resistor, designated as R_{FF} in 图 8-1 or 图 8-2, in series with C_{FF}. If the ESR zero of the output capacitor is below 200kHz, feedforward network components are not required.

Capacitor C_{FF} has little effect if the output voltage is less than 2.5V, so C_{FF} can be omitted. If the output voltage setpoint is greater than 14V, do not use C_{FF} because it introduces too much gain at higher frequencies. Use the LM64440-Q1 or LM64460-Q1 *Quickstart Calculator* to review bode plot performance for a given combination of output capacitance and feedforward capacitance.

8.2.2.2.11 Input Voltage UVLO

In some cases, an input UVLO level different than that provided internal to the device is required. Based on the circuit shown in 图 8-1 or 图 8-2, $V_{IN(on)}$ and $V_{IN(off)}$ designate the input voltages thresholds at which the converter turns on and off, respectively. First, choose a value for the lower resistance R_{ENB} in the range of 10kΩ to 100kΩ. Then use 方程式 14 to calculate the upper resistance R_{ENT} based on a target input voltage turn-on threshold of 5.9V.

$$R_{ENT}\left[k\Omega\right] = R_{ENB}\left[k\Omega\right] \cdot \left(\frac{V_{IN(on)}\left[V\right]}{V_{EN\text{-}TH}\left[V\right]} - 1 \right) = 100k\Omega \cdot \left(\frac{5.9\,V}{1.263V} - 1 \right) = 367k\Omega \tag{14}$$

Selecting upper and lower resistances of 365kΩ and 100kΩ gives input voltage turn-on and turn-off thresholds of 5.87V and 4.23V, respectively.

8.2.2.3 Application Curves

Unless otherwise indicated, V_{IN} = 13.5V, V_{OUT} = 5V, I_{OUT} = 6A, f_{SW} = 2.1MHz, AUTO mode, and T_A = 25°C. 图 8-1 shows the circuit schematic with relevant BOM components specified in 表 8-2.

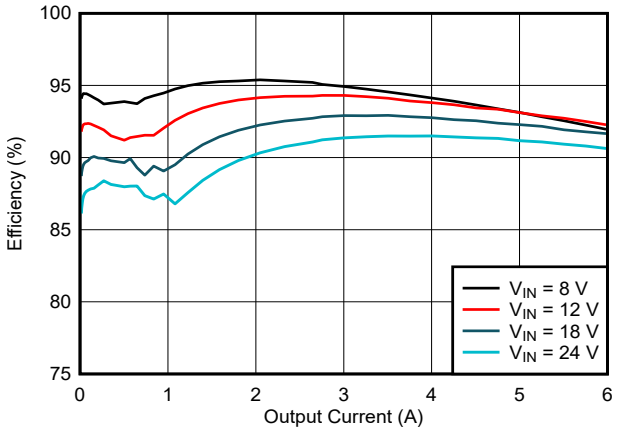


图 8-3. LM644x0-Q1 Efficiency

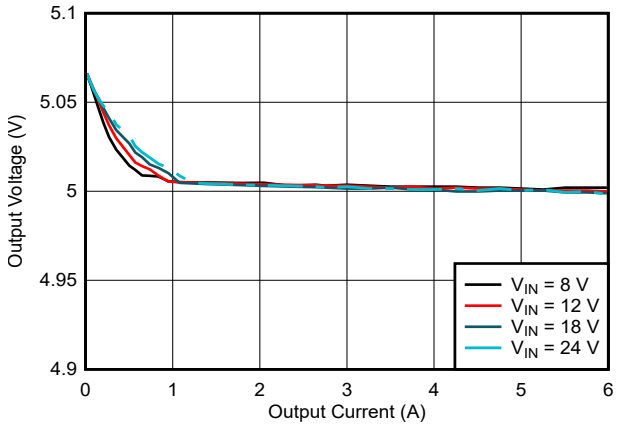


图 8-4. LM644x0-Q1 Load and Line Regulation

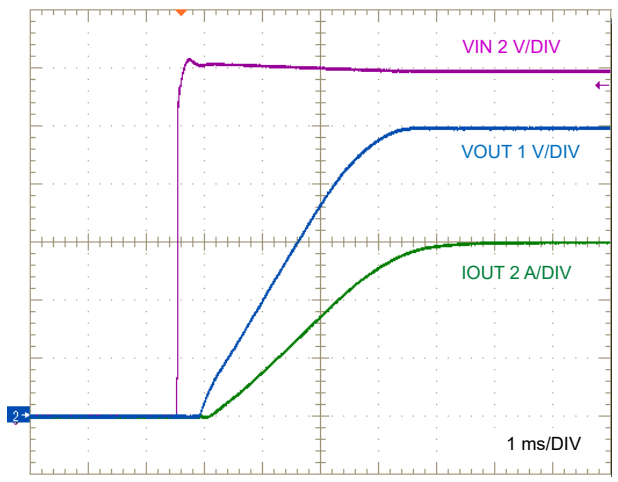


图 8-5. LM644x0-Q1 Start-Up, 6A Resistive Load

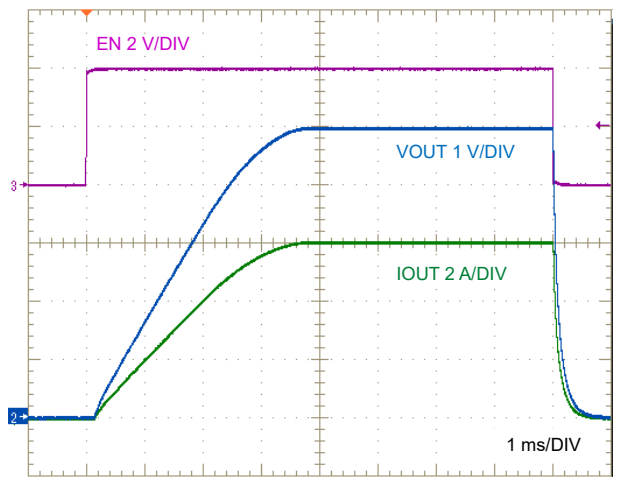


图 8-6. LM644x0-Q1 Enable On and Off, 6A Resistive Load

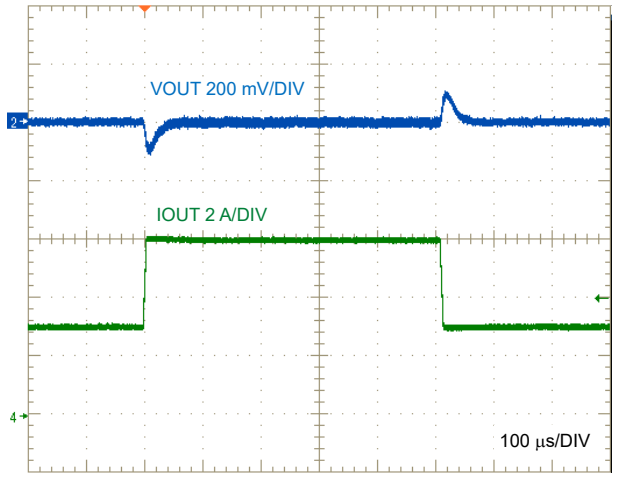


图 8-7. LM644x0-Q1 Load Transient, I_{OUT} = 3A to 6A

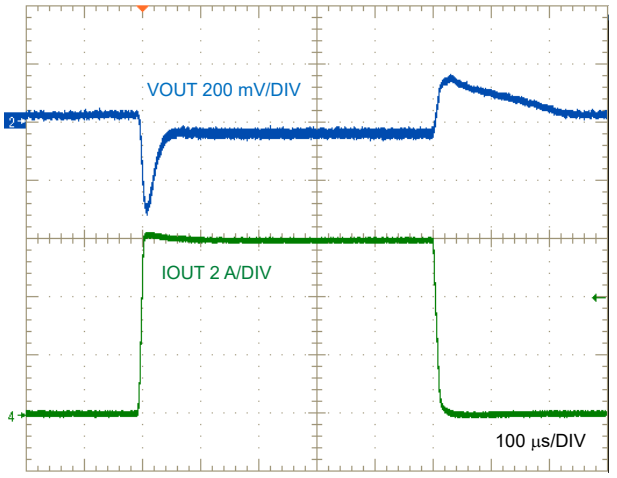


图 8-8. LM644x0-Q1 Load Transient, I_{OUT} = 0A to 6A

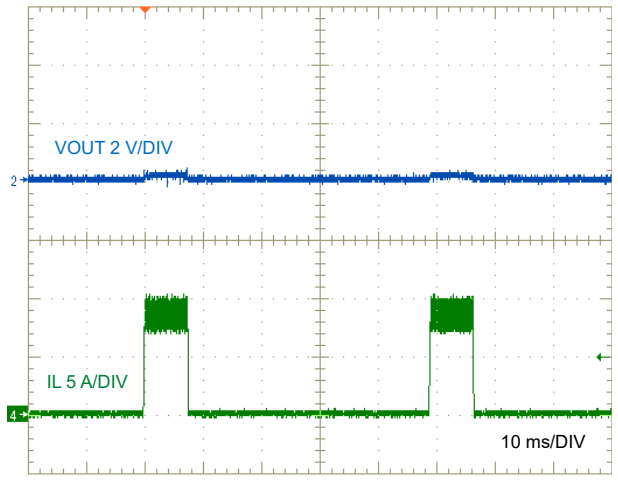


图 8-9. LM644x0-Q1 Short-Circuit Hiccup

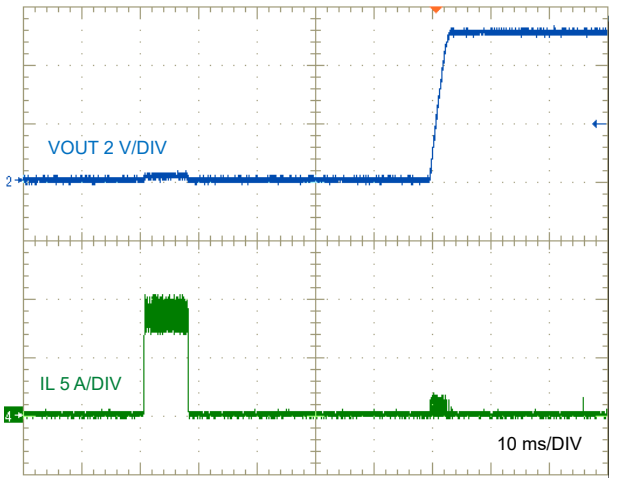


图 8-10. LM644x0-Q1 Short-Circuit Recovery to No Load

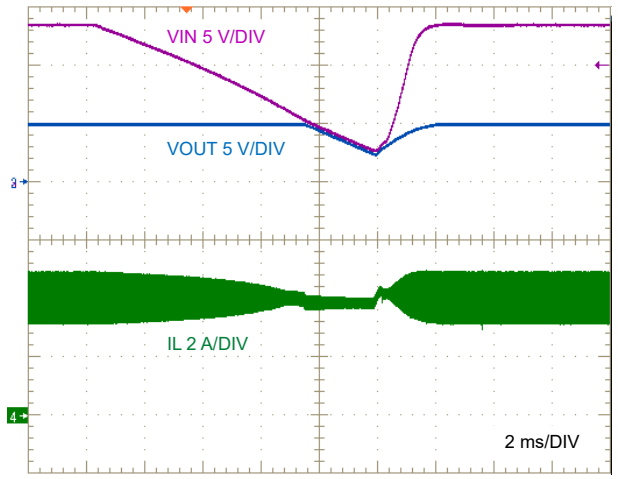


图 8-11. LM644x0-Q1 Line Transient and Recovery from Dropout

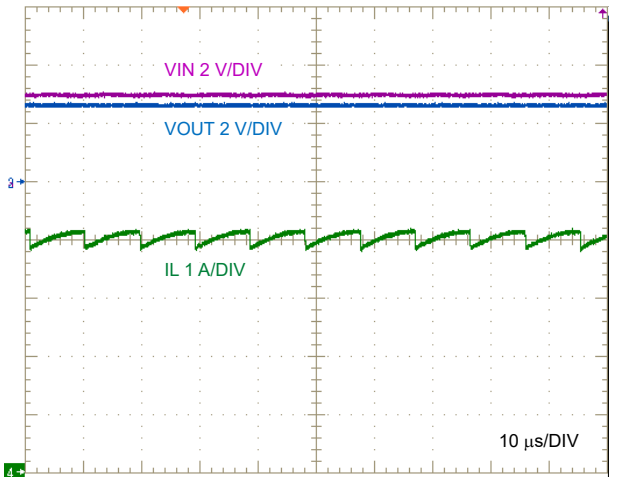
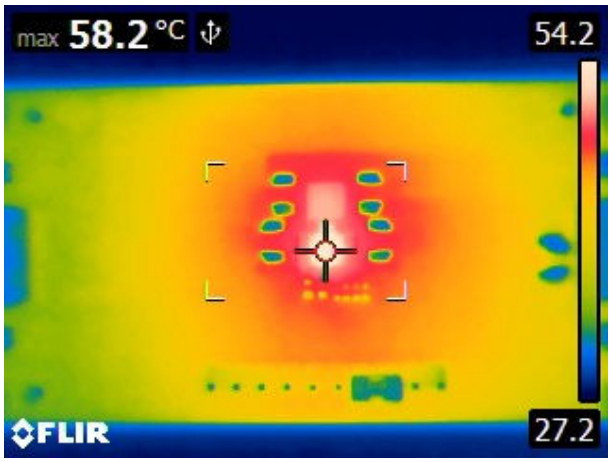
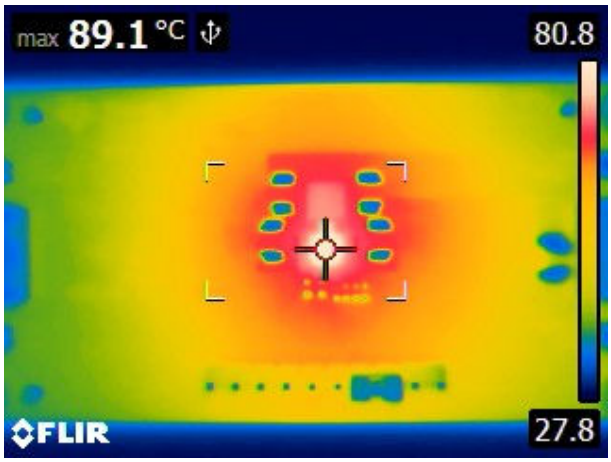


图 8-12. LM644x0-Q1 Frequency Foldback in Dropout, V_{IN} = 3V



76mm × 38mm, 4-layer PCB

图 8-13. Thermal Performance, 4A Load



76mm × 38mm, 4-layer PCB

图 8-14. Thermal Performance, 6A Load

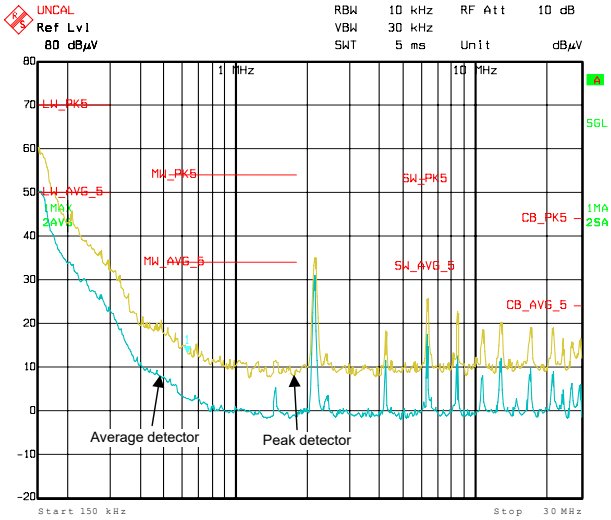


图 8-15. CISPR 25 Class 5 Conducted EMI, 150kHz to 30MHz

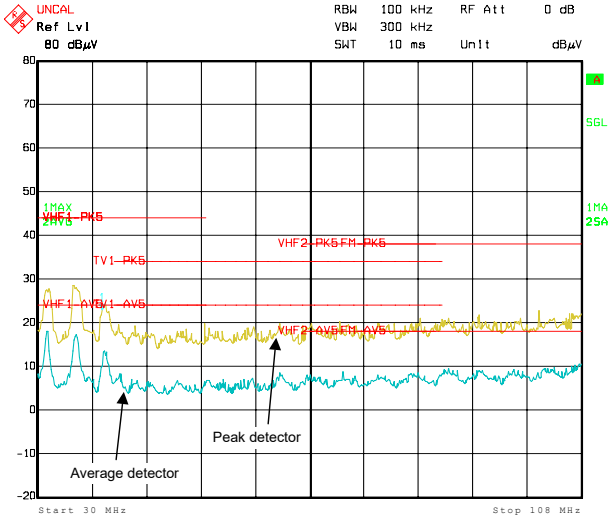


图 8-16. CISPR 25 Class 5 Conducted EMI, 30MHz to 108MHz

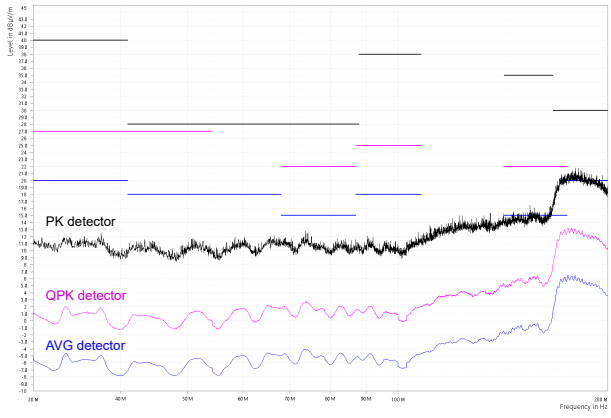


图 8-17. CISPR 25 Class 5 Radiated EMI, Bicon Antenna, Horizontal Polarization, 30MHz to 200MHz

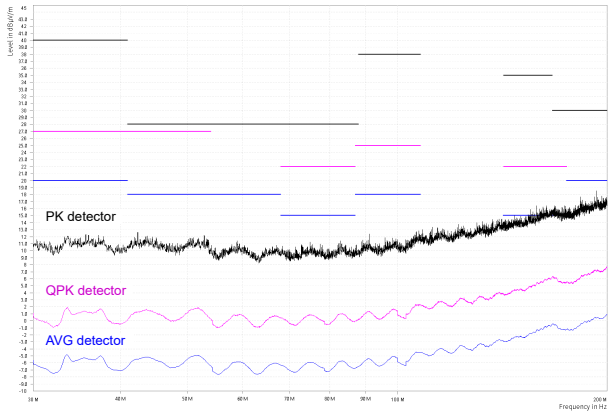


图 8-18. CISPR 25 Class 5 Radiated EMI, Bicon Antenna, Vertical Polarization, 30MHz to 200MHz

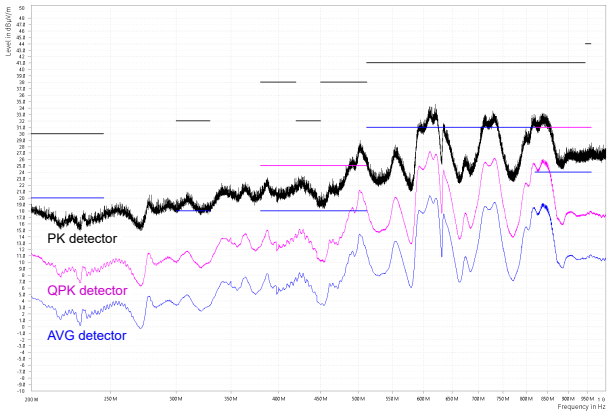


图 8-19. CISPR 25 Class 5 Radiated EMI, Log Antenna, Horizontal Polarization, 200MHz to 1GHz

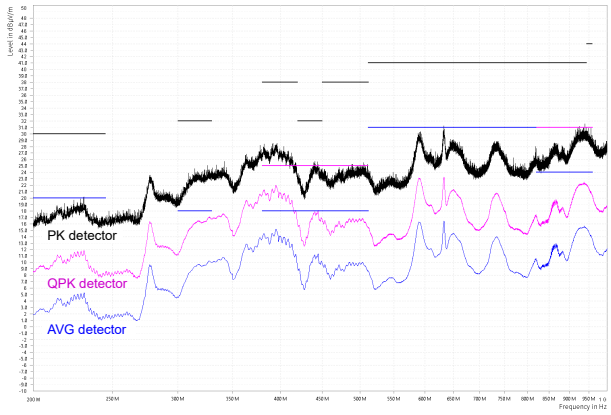


图 8-20. CISPR 25 Class 5 Radiated EMI, Log Antenna, Vertical Polarization, 200MHz to 1GHz

8.3 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter. Estimate the average input current with 方程式 15.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{15}$$

where

- η is the efficiency.

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability and voltage transients each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the converter is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the converter and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. An ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

The input voltage must not be allowed to suddenly fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the body diode of the internal high-side power MOSFET. The current is effectively uncontrolled during this condition, possibly causing damage to the device. If this scenario is considered likely, then connect a Schottky bypass diode between the output and the input supply.

8.4 Layout

8.4.1 Layout Guidelines

Proper PCB design and layout is important in high-current, fast-switching converter circuits (with high current and voltage slew rates) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the converter depends to a large extent on PCB layout.

图 8-21 denotes the high-frequency switching power loops of the LM64440-Q1 or LM64460-Q1 power stage. The topological architecture of a buck converter means that particularly high di/dt current flows in the power MOSFETs and input capacitors, and reducing the parasitic inductance by minimizing the effective power loop areas becomes mandatory. For both LM64440-Q1 and LM64460-Q1, note the dual and symmetrical arrangement of the input capacitors based on the VIN and PGND pins located on each side of the IC package. The high-frequency currents are split in two and effectively flow in opposing directions such that the related magnetic fields contributions cancel each other, leading to improved EMI performance.

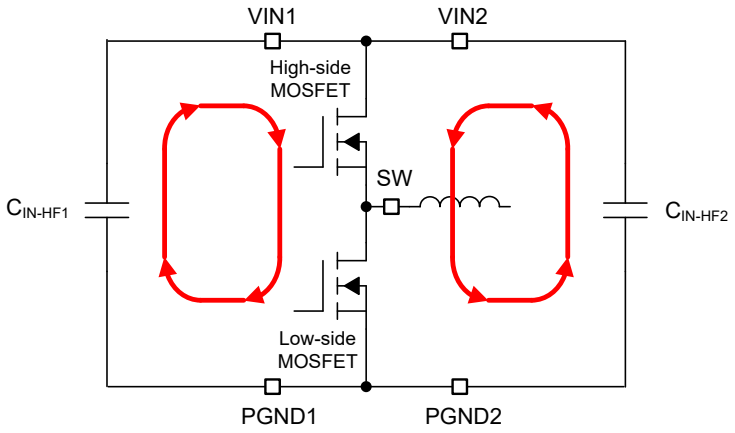


图 8-21. Input Current Loops

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC converter performance, including thermals and EMI signature. 图 8-22 shows a recommended layout of either the LM64440-Q1 or LM64460-Q1 with optimized placement and routing of the power-stage and small-signal components.

- *Place the input capacitors as close as possible to the input pin pairs [VIN1, PGND1] and [VIN2, PGND2]*: The respective VIN and PGND pins pairs are close together (with an NC pin in between to increase clearance), thus simplifying input capacitor placement. The Enhanced HotRod QFN package provides VIN and PGND pins on either side of the package to enable a symmetrical layout that helps to minimize switching noise and EMI.
  - Use low-ESR ceramic capacitors with X7R or X7S dielectric from VIN1 to PGND1 and VIN2 to PGND2. Place an 0402 capacitor close to each pin pair for high-frequency bypass as shown in 图 8-22. Use an adjacent 1206 or 1210 capacitor on each side for bulk capacitance.
  - Ground return paths for both the input and output capacitors must consist of localized top-side planes that connect to the PGND1 and PGND2 pins.
  - Use a wide polygon plane on a lower PCB layer to connect VIN1 and VIN2 together and to the input supply.
- *Use a solid ground plane on the PCB layer beneath the top layer with the IC*: This plane acts as a noise shield and a heat dissipation path. Using the PCB layer directly below the IC minimizes the magnetic field associated with the currents in the switching loops, thus reducing parasitic inductance and switch voltage overshoot and ringing. Use numerous thermal vias near PGND1 and PGND2 for heatsinking to the inner ground planes.
- *Make the VIN, VOUT, and GND bus connections as wide as possible*: These paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter, thus maximizing efficiency.
- *Locate the buck inductor close to the SW1, SW2, and SW3 pins*: Use a short, wide connection trace from the converter SW pins to the inductor. At the same time, minimize the length (and area) of this high-dv/dt surface to help reduce capacitive coupling and radiated EMI. Connect the dotted terminal of the inductor to the SW pins.
- *Place the VCC and BOOT capacitors close to the respective pins*: The VCC and BOOT capacitors represent the supplies for the internal low-side and high-side MOSFET gate drivers, respectively, and thus carry high-frequency currents. Locate C_{VCC} close to the VCC pin and place a GND via at the return terminal to connect to the GND plane and thus back to IC GND at the exposed pad. Connect C_{BOOT} close to the CBOOT and SW4 pins.
- *Place the feedback divider as close as possible to the FB pin*: For adjustable output versions of LM64440-Q1 and LM64460-Q1, reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This placement reduces the FB trace length and related noise coupling. The FB pin is the input to the voltage-loop error amplifier and represents a high-impedance

node sensitive to noise. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the switch node) that can capacitively couple into the feedback path of the converter. For fixed output versions, connect FB directly to the point of output voltage regulation.

- *Provide enough PCB area for proper heatsinking*: Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heatsinking for the LM64440-Q1 or LM64460-Q1 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad (GND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. Make the top and bottom PCB layers preferably with two-ounce copper thickness (and no less than one ounce).

8.4.1.1 Thermal Design and Layout

For a DC/DC converter to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM64440-Q1 and LM64460-Q1 converter are available in a small 3.5mm × 4mm 22-pin Enhanced HotRod QFN (RYF) package to cover a range of application requirements. The *Thermal Information* table summarizes the thermal metrics of this package, with related detail provided by the *Semiconductor and IC Package Thermal Metrics Application Report* .

The 22-pin Enhanced HotRod QFN package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. The exposed pad of the package is thermally connected to the substrate of the LM64440-Q1 or LM64460-Q1 device (ground). This allows a significant improvement in heatsinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and one or more ground planes to complete the heat removal subsystem. The exposed pad of the LM64440-Q1 or LM64460-Q1 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the IC thermal resistance to a very low value.

Preferably, use a four-layer board with 2oz copper thickness for all layers to provide low impedance, proper shielding and lower thermal resistance. Numerous vias with a 0.3mm diameter connected from the thermal land (and from the area around the PGND1 and PGND2 pins) to the internal and solder-side ground planes are vital to promote heat transfer. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power-stage components. Not only does this provide a plane for the power-stage currents to flow, but it also represents a thermally conductive path away from the heat-generating devices.

8.4.2 Layout Example

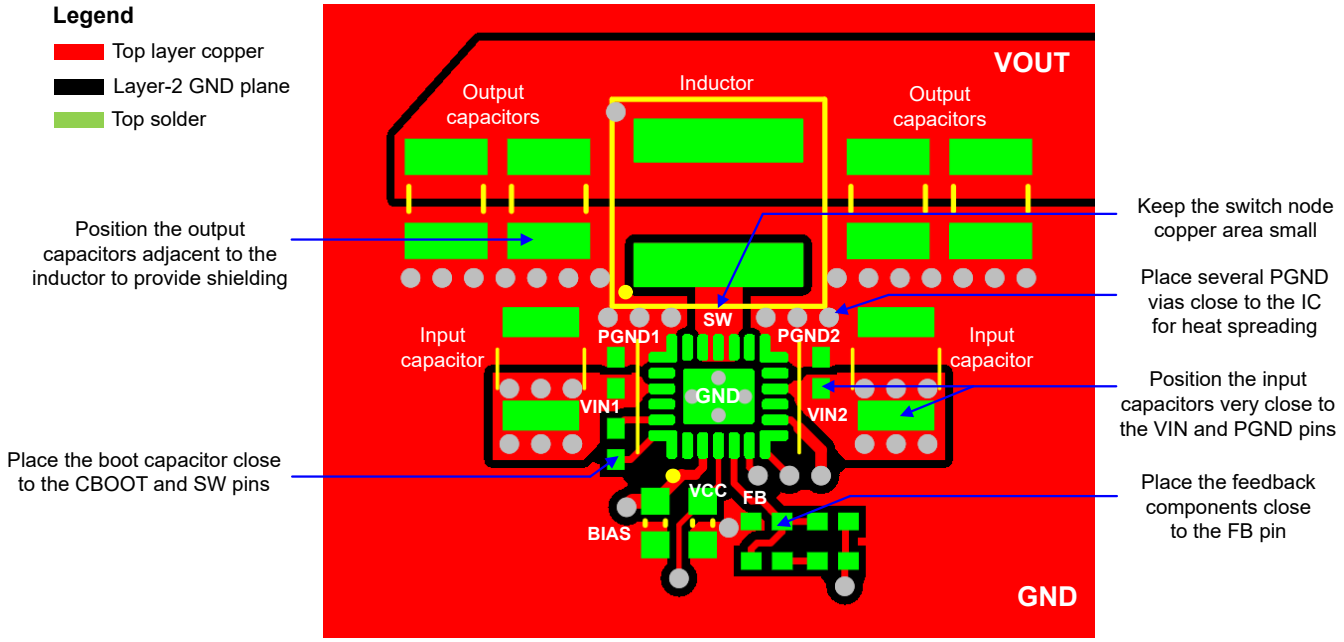


图 8-22. PCB Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.1.2 Development Support

With an input operating voltage as low as 3V and up to 36V as specified in 表 9-1, the LM6k-Q1 family of automotive synchronous buck converters from TI provides flexibility, scalability and optimized design size for a range of applications. These converters enable DC/DC designs with high density, low EMI and increased flexibility. Available EMI mitigation features include pseudo-random spread spectrum (PRSS), integrated input bypass capacitors, RBOOT-configured switch-node slew rate control, and optimized package design with symmetrical VIN and PGND pins that shield a small switch-node copper area. All converters are rated for a maximum operating junction temperature of 150°C, have AEC-Q100 grade 1 qualification, and are functional safety capable.

表 9-1. Automotive Synchronous Buck DC/DC Converter Family

DC/DC CONVERTER	RATED I_{OUT}	PACKAGE	FEATURES	EMI MITIGATION
LM60430-Q1, LM60440-Q1	3A, 4A	WQFN (13)	400kHz fixed f_{SW}, 3mm × 2mm package	Shielded switch node
LM63610-Q1, LM63615-Q1, LM63625-Q1, LM63635-Q1	1A, 1.5A, 2.5A, 3.25A	WSON (12), HTSSOP (16)	RT adjustable f_{SW}, MODE/SYNC	PRSS
LM61430-Q1, LM61435-Q1, LM61440-Q1, LM61460-Q1	3A, 3.5A, 4A, 6A	VQFN-HR (14)	RT adjustable f_{SW}, EN/SYNC	PRSS, RBOOT
LM62435-Q1, LM62440-Q1	3.5A, 4A		2.1MHz default f_{SW}, MODE/SYNC	
LMQ61460-Q1	6A		RT adjustable f_{SW}, EN/SYNC	PRSS, RBOOT, integrated capacitors
LMQ62440-Q1	4A		2.1MHz default f_{SW}, MODE/SYNC	
LM62460-Q1, LM61480-Q1, LM61495-Q1	6A, 8A, 10A	VQFN-HR (16)	RT adjustable f_{SW}, MODE/SYNC	DRSS, RBOOT
LM63440-Q1, LM63460-Q1	4A, 6A	VQFN-FCRLF (22)	RT adjustable f_{SW}, EN/SYNC, pin FMEA	PRSS
LM64440-Q1, LM64460-Q1			2.1MHz default f_{SW}, MODE/SYNC, pin FMEA	

For development support see the following:

- LM644x0-Q1 *EVM User's Guide*
- LM644x0-Q1 *Quickstart Calculator*
- LM64460-Q1 *Simulation Models*
- LM644x0-Q1 *EVM Altium Layout Files*
- For TI's reference design library, visit TI Designs.
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center.
- To design a low-EMI power supply, review TI's comprehensive EMI Training Series.
- TI reference designs:
  - *30-W Power For Automotive Dual USB Type-C™ Charge Port Reference Design*
  - *High Efficiency, Low Noise, 5-V/3.3-V/1.8-V/1.1-V Automotive Display Reference Design*
- Technical articles:
  - *How Device-level Features And Package Options Can Help Minimize EMI In Automotive Designs*
  - *Optimizing Flip-chip IC Thermal Performance In Automotive Designs*
  - *Powering Levels Of Autonomy: A Quick Guide To DC/DC Solutions For SAE Autonomy Levels*
  - *Powering Infotainment Systems Of The Future*
- To view related devices of this product, see the LM63460-Q1 6-A converter and the TPSM63606 6-A power module.

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM64440-Q1 or LM64460-Q1 converter with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Enhanced HotRod™ QFN Package: Achieving Low EMI Performance in Industry's Smallest 4-A Converter* application report
- Texas Instruments, *Designing High Performance, Low-EMI, Automotive Power Supplies* application report
- Texas Instruments, *EMI Filter Components And Their Nonidealities For Automotive DC/DC Regulators* technical brief
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC/DC Converters Application Report* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.5 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (October 2023) to Revision B (August 2024)	Page
• 在整个数据表中添加了 LM64440-Q1 和支持信息	1
• Updated *Device Comparison Table* to include 4A devices	3
• Added recommended operating current for the LM64440-Q1 and added GPN to the description of operating current for the LM64460-Q1	6
• Added LM64440-Q1 to the header of the Thermal Information table	7
• Added high side, low side, and negative current limits for the LM64440-Q1 and added GPN to current limit descriptions for the LM64460-Q1	7
• Added efficiency specifications for the LM64440-Q1 and added GPN to the test conditions for efficiency specifications for the LM64460-Q1	11
• Added 4A test condition for output accuracy specifications for the LM64440-Q1 in Systems Characteristics table	11
• Added LM64440-Q1 application circuit in the *Typical Application* section	33
• Updated *Development Support* to include LM63440-Q1 and LM64440-Q1	48

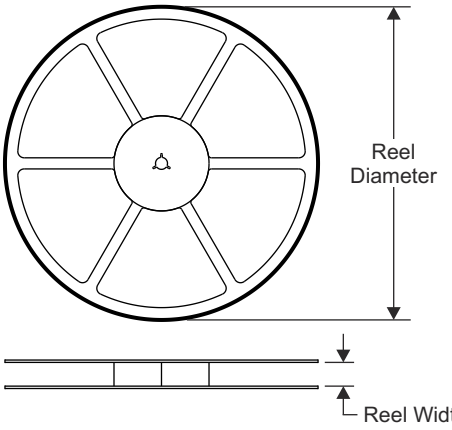
Changes from Revision * (October 2022) to Revision A (October 2023)	Page
• 更新了 *器件信息* 表标题	1
• Updated *Device Comparison Table*	3

11 Mechanical, Packaging, and Orderable Information

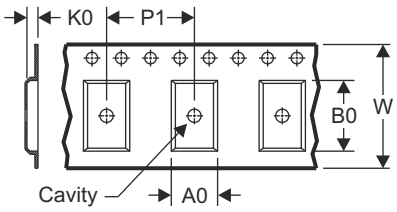
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

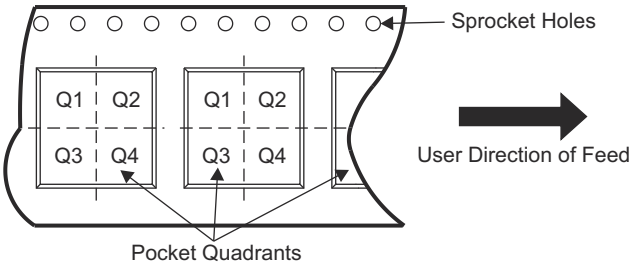


TAPE DIMENSIONS



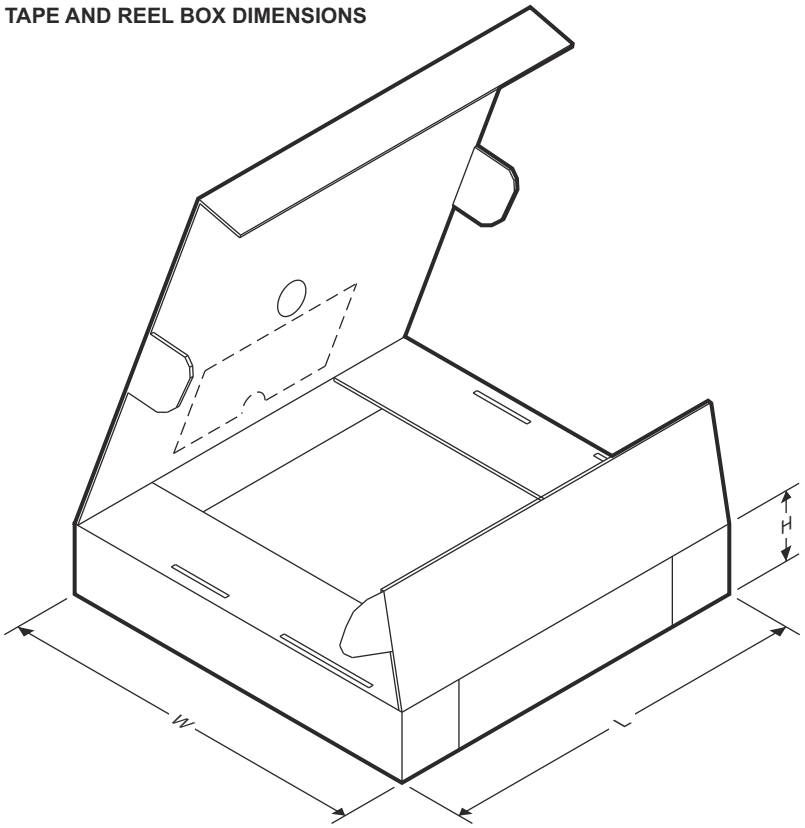
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM64460APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64460APPSRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64460BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64460CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64440APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64440BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64440CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



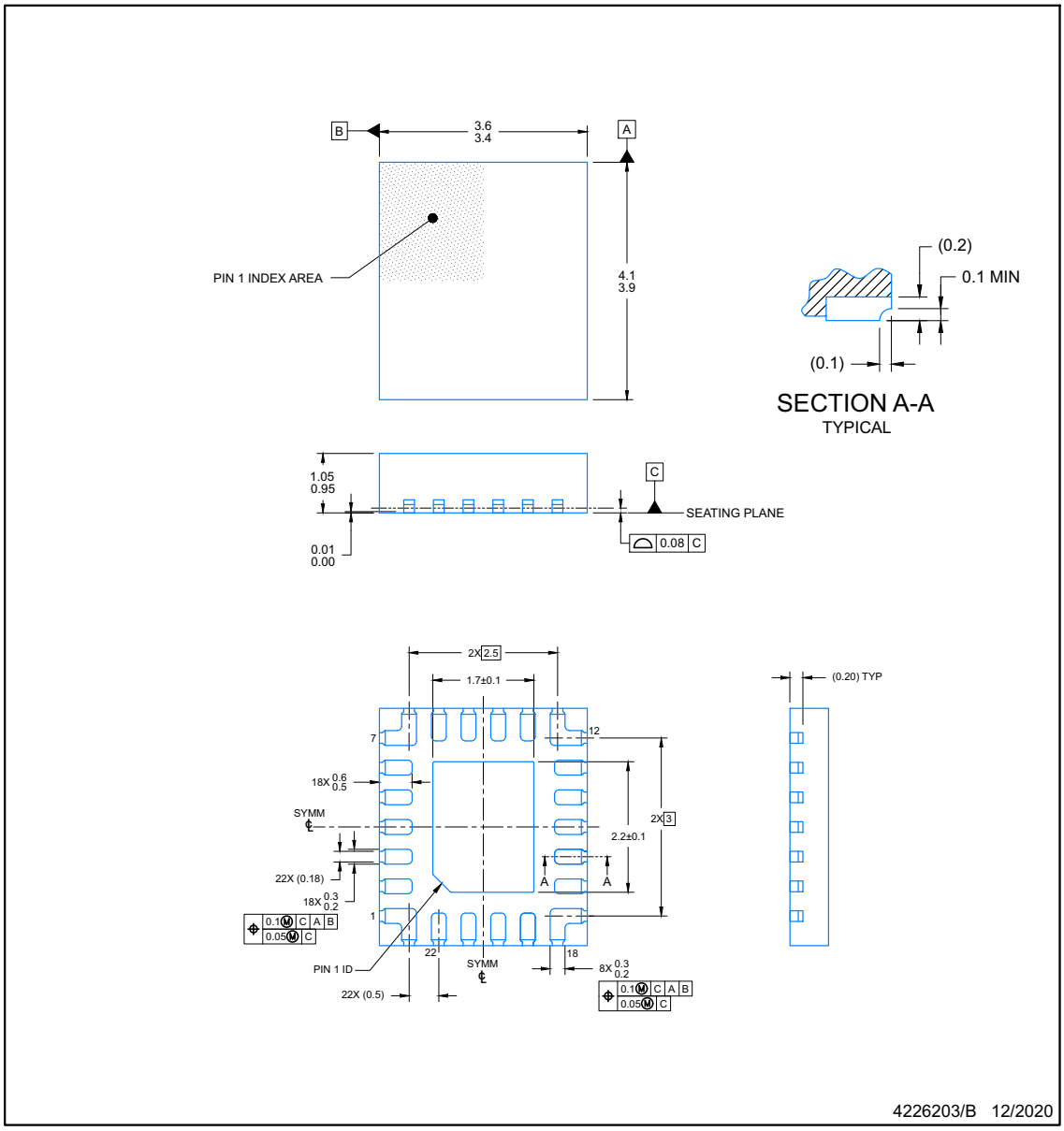
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM64460APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64460APPSRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64460BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64460CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64440APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64440BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64440CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RYF0022A

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

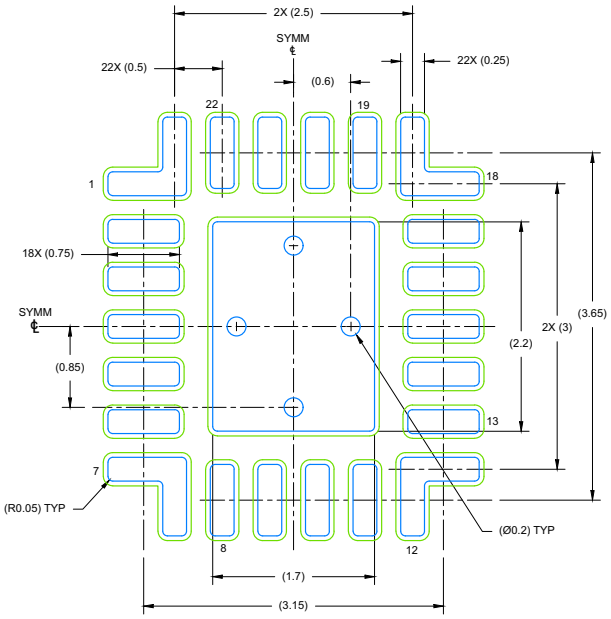
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

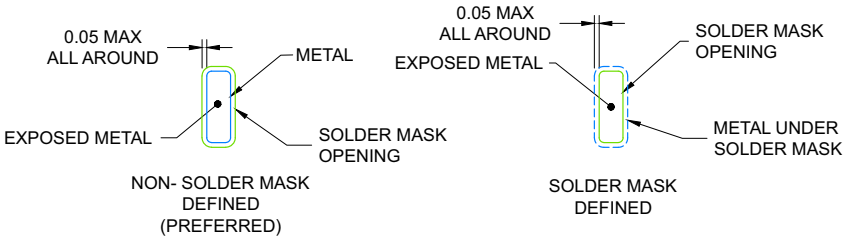
RYF0022A

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4226203/B 12/2020

NOTES: (continued)

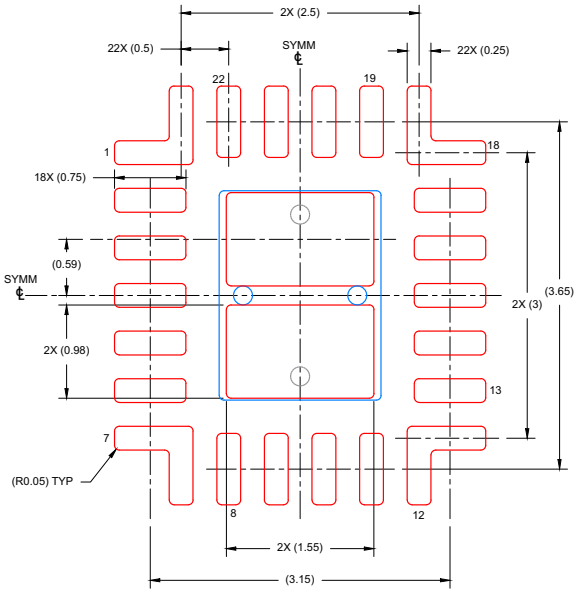
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RYF0022A

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD:
81% PRINTED SOLDER COVERAGE BY AREA

SCALE: 15X

4226203/B 12/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM64440APPQRYFRQ1	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6444APP
LM64440APPQRYFRQ1.A	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6444APP
LM64440BPPQRYFRQ1	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6444BPP
LM64440BPPQRYFRQ1.A	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6444BPP
LM64440CPPQRYFRQ1	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6444CPP
LM64440CPPQRYFRQ1.A	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6444CPP
LM64460APPQRYFRQ1	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6446APP
LM64460APPQRYFRQ1.A	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6446APP
LM64460APPSRYFRQ1	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	644APPS
LM64460APPSRYFRQ1.A	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	644APPS
LM64460BPPQRYFRQ1	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6446BPP
LM64460BPPQRYFRQ1.A	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6446BPP
LM64460CPPQRYFRQ1	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6446CPP
LM64460CPPQRYFRQ1.A	Active	Production	VQFN-FCRLF (RYF) | 22	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6446CPP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

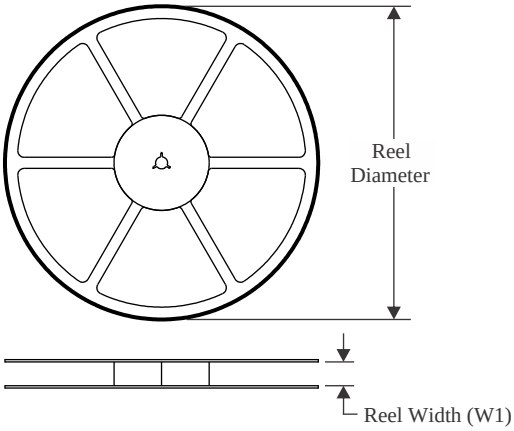
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

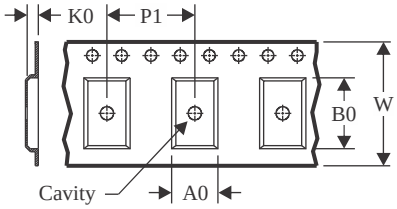
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

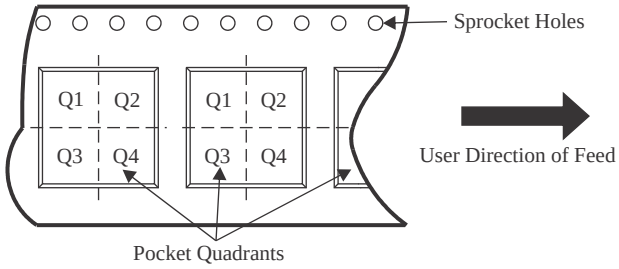


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

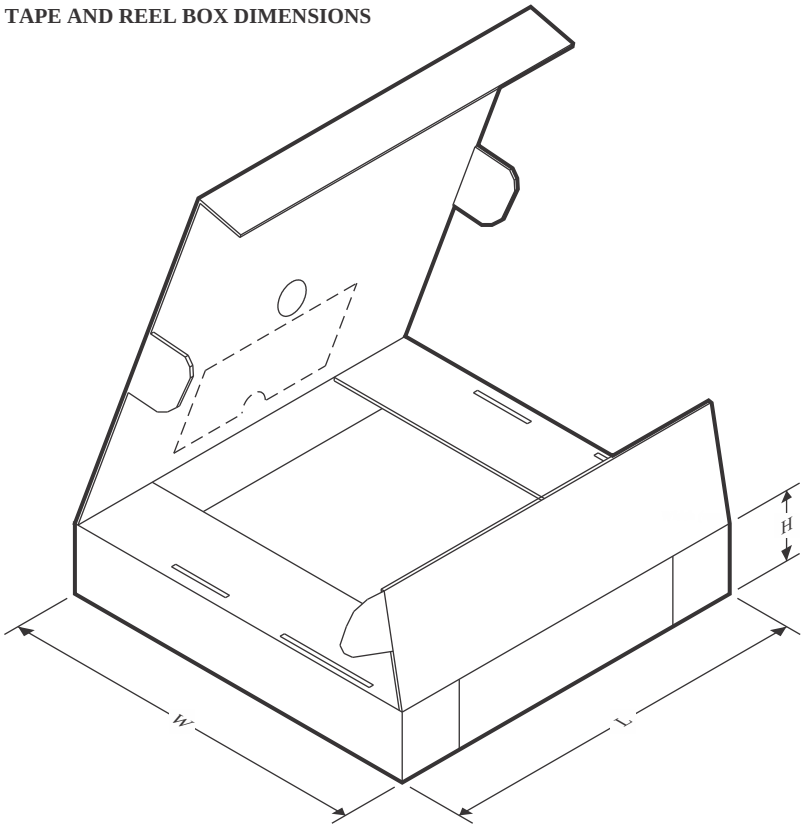
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM64440APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64440BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64440CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64460APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64460APPSRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64460BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
LM64460CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

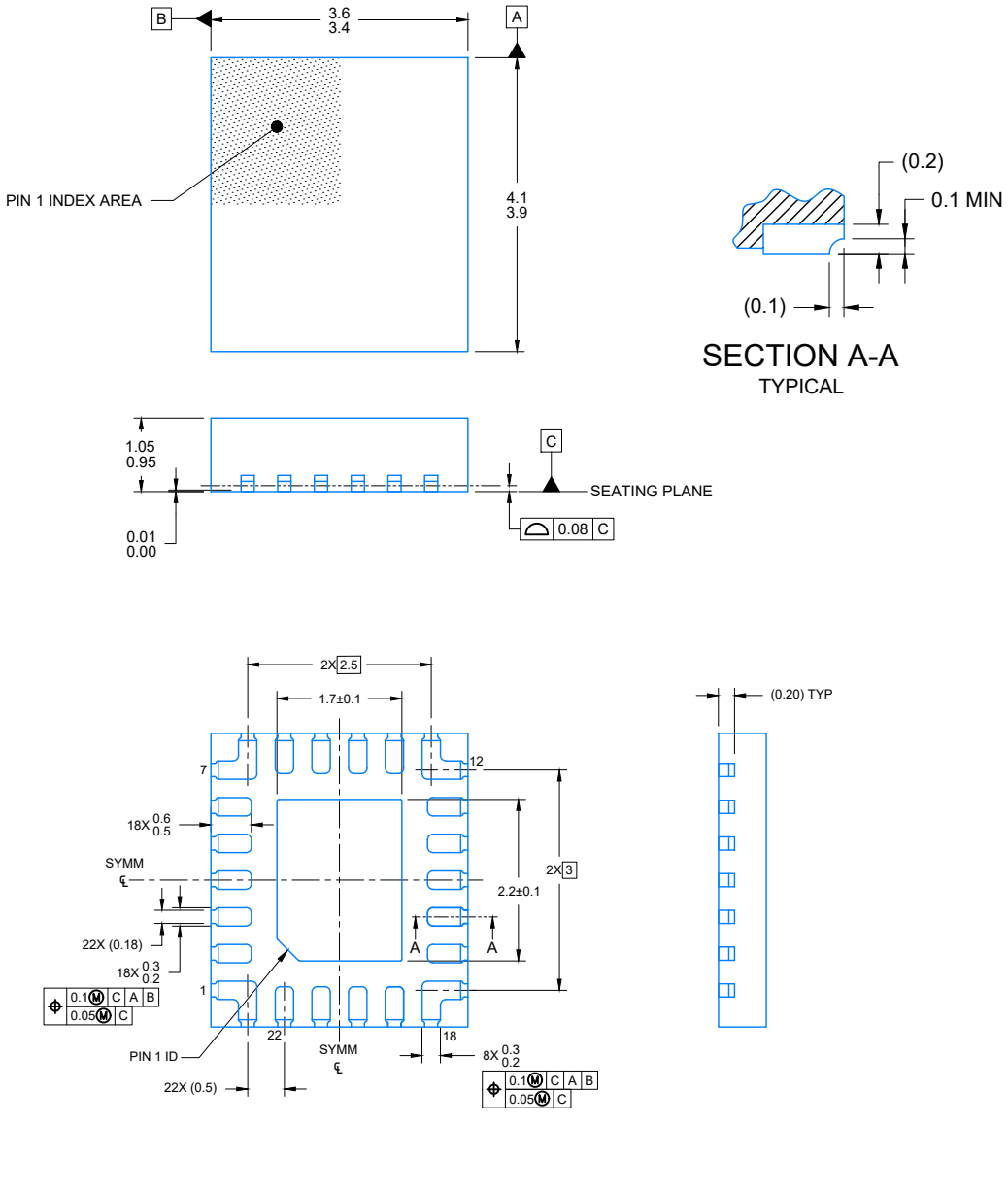
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM64440APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64440BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64440CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64460APPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64460APPSRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64460BPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0
LM64460CPPQRYFRQ1	VQFN-FCRLF	RYF	22	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RYF0022A

VQFN-FCRLF - 1.05 mm max height

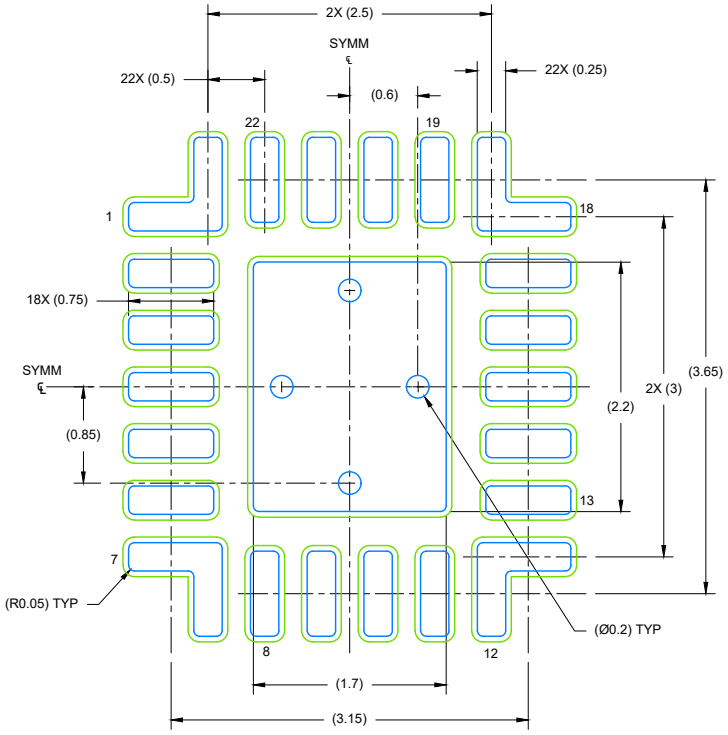
PLASTIC QUAD FLAT PACK- NO LEAD



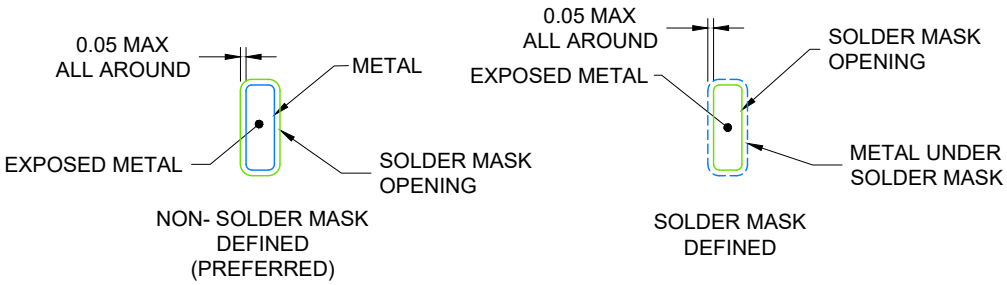
4226203/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4226203/B 12/2020

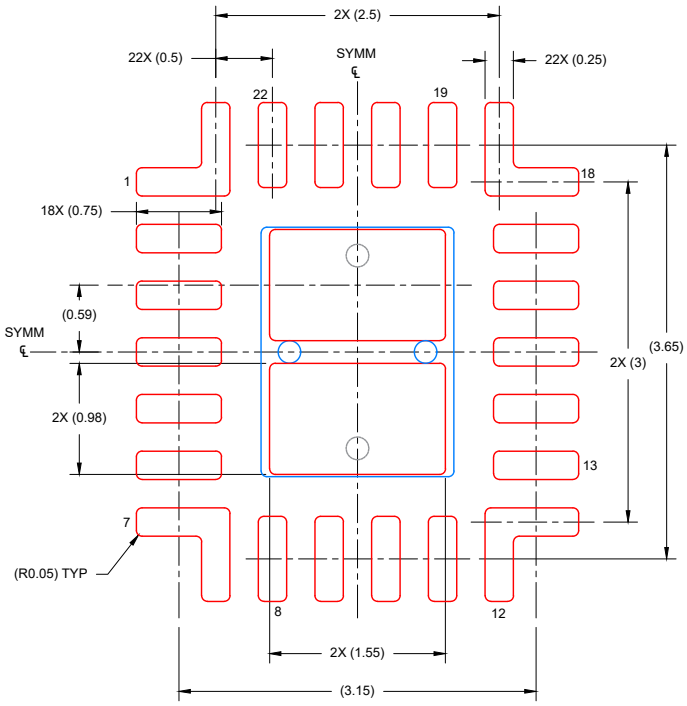
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD:
81% PRINTED SOLDER COVERAGE BY AREA

SCALE: 15X

4226203/B 12/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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