BCM® Bus Converter

BCM6123xD1E2662yzz

Fixed Ratio DC-DC Converter

Features

- Up to 62.5A continuous secondary current
- Up to 2352W/in^3 power density
- 97.4% peak efficiency
- 4,242V_{DC} isolation
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 6123 through-hole ChiP package
  - 2.402" x 0.990" x 0.286" (61.00mm x 25.14mm x 7.26mm)
- PMBus™ management interface*

Typical Applications

- 380V_{DC} Power Distribution
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

Product Ratings	
V_{PRI} = 384V (260 – 410V)	I_{SEC}= up to 62.5A
V_{SEC} = 24V (16.3 – 25.6V) (NO LOAD)	K = 1/16

Product Description

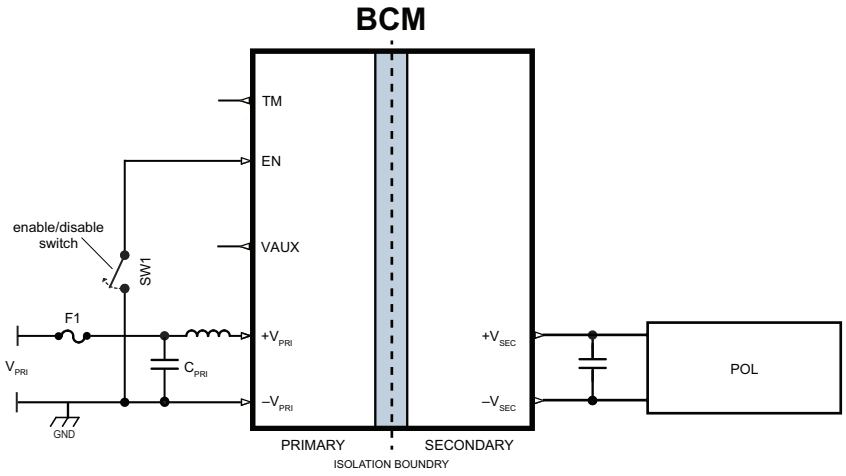
The BCM6123xD1E2662yzz Bus Converter (BCM) is a high efficiency Sine Amplitude Converter™ (SAC™), operating from a 260 to 410V_{DC} primary bus to deliver an isolated, ratiometric secondary voltage from 16.3 to 25.6V_{DC}.

The BCM6123xD1E2662yzz offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a POL regulator to be located at the primary side of the BCM module. With a primary to secondary K factor of 1/16, that capacitance value can be reduced by a factor of 256x, resulting in savings of board area, material and total system cost.

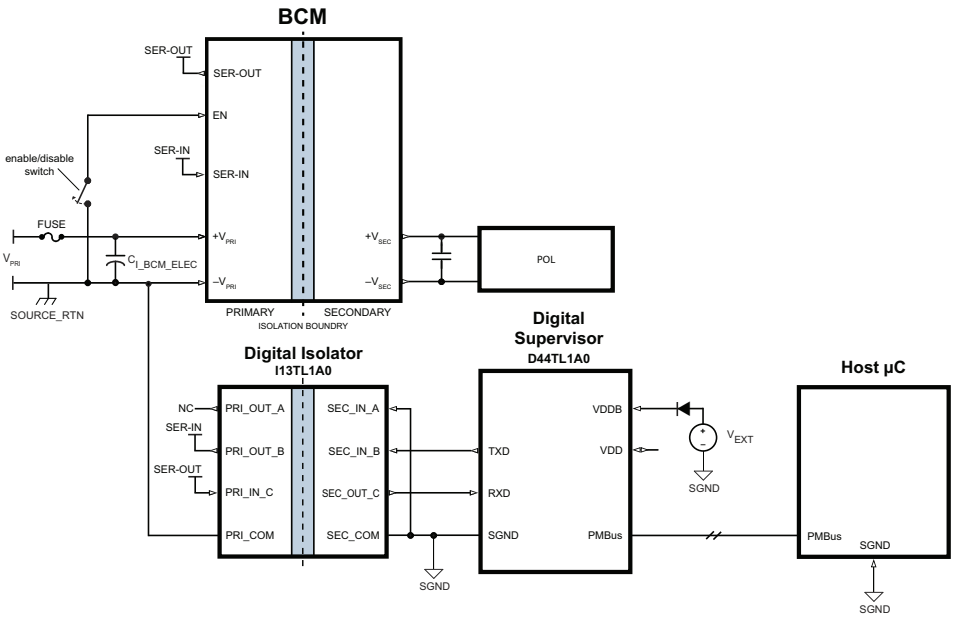
Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components, enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

*When used with D44TL1A0 and I13TL1A0 chipset

Typical Application

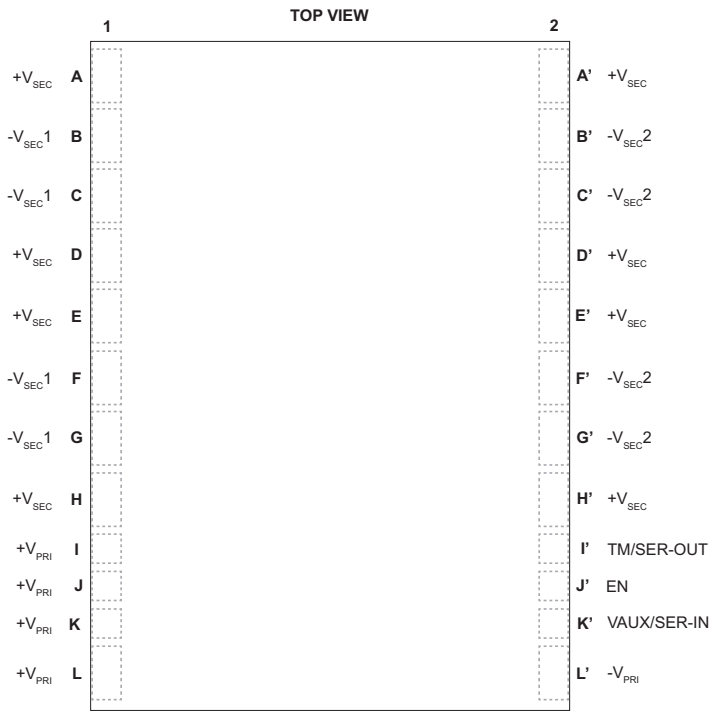


BCM6123xD1E2662y00 at Point of load



BCM6123xD1E2662y01 at Point of load

Pin Configuration



6123 ChiP Package

Pin Descriptions

Power Pins			
Pin Number	**Signal Name**	**Type**	**Function**
I1, J1, K1, L1	$+V_{PRI}$	PRIMARY POWER	Positive primary transformer power terminal
L'2	$-V_{PRI}$	PRIMARY POWER RETURN	Negative primary transformer power terminal
A1, D1, E1, H1, A'2, D'2, E'2, H'2	$+V_{SEC}$	SECONDARY POWER	Positive secondary transformer power terminal
B1, C1, F1, G1 B'2, C'2, F'2, G'2	$-V_{SEC}$*	SECONDARY POWER RETURN	Negative secondary transformer power terminal
Analog Control Signal Pins			
Pin Number	**Signal Name**	**Type**	**Function**
I'2	TM	OUTPUT	Temperature Monitor; primary side referenced signals
J'2	EN	INPUT	Enables and disables power supply; primary side referenced signals
K'2	VAUX	OUTPUT	Auxilary Voltage Source; primary side referenced signals
PMBus Control Signal Pins			
Pin Number	**Signal Name**	**Type**	**Function**
I'2	SER-OUT	OUTPUT	UART transmit pin; Primary side referenced signals
J'2	EN	INPUT	Enables and disables power supply; Primary side referenced signals
K'2	SER-IN	INPUT	UART receive pin; Primary side referenced signals

*For proper operation an external low impedance connection must be made between listed $-V_{SEC}1$ and $-V_{SEC}2$ terminals.

Part Ordering Information

Product Function	Package Size	Package Mounting	Max Primary Input Voltage	Range Identifier	Max Secondary Voltage	Secondary Output Current	Temperature Grade	Option
BCM	6123	x	D1	E	26	62	y	zz
Bus Converter Module	61 = L 23 = W	**T** = TH **S** = SMT	410V	260 – 410V	25.6V No Load	62.5A	**T** = -40°C – 125°C **M** = -55°C – 125°C	**00** = Analog Ctrl **01** = PMBus Ctrl **0R** = Reversible Analog Ctrl **0P** = Reversible PMBus Ctrl

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Standard Models

Product Function	Package Size	Package Mounting	Max Primary Input Voltage	Range Identifier	Max Secondary Voltage	Secondary Output Current	Temperature Grade	Option
BCM	6123	T	D1	E	26	62	M	00
BCM	6123	T	D1	E	26	62	T	00
BCM	6123	T	D1	E	26	62	M	01
BCM	6123	T	D1	E	26	62	T	01

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
$+V_{PRI\_DC}$ to $-V_{PRI\_DC}$		-1	480	V
V_{PRI_DC} or V_{SEC_DC} slew rate (operational)			1	V/µs
$+V_{SEC\_DC}$ to $-V_{SEC\_DC}$		-1	30	V
TM / SER-OUT to $-V_{PRI\_DC}$		-0.3	4.6	V
EN to $-V_{PRI\_DC}$			5.5	V
VAUX / SER-IN to $-V_{PRI\_DC}$			4.6	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powetrain PRIMARY to SECONDARY Specification (Forward Direction)						
Primary Input Voltage range, continuous	V_{PRI_DC}		**260**		**410**	V
V_{PRI} µController	$V_{\mu C\_ACTIVE}$	V_{PRI_DC} voltage where µC is initialized, (ie VAUX = Low, powertrain inactive)			130	V
PRI to SEC Input Quiescent Current	I_{PRI_Q}	Disabled, EN Low, V_{PRI_DC} = 384V		2		mA
		$T_{INTERNAL}$ ≤ 100°C			4	
PRI to SEC No Load Power Dissipation	P_{PRI_NL}	V_{PRI_DC} = 384V, $T_{INTERNAL}$ = 25°C		13	20	W
		V_{PRI_DC} = 384V	**6**		**27**	
		V_{PRI_DC} = 260V to 410V, $T_{INTERNAL}$ = 25 °C			21	
		V_{PRI_DC} = 260V to 410V			**29**	
PRI to SEC Inrush Current Peak	$I_{PRI\_INR\_PK}$	V_{PRI_DC} = 410V, C_{SEC_EXT} = 1000µF, R_{LOAD_SEC} = 20% of full load current		4		A
		$T_{INTERNAL}$ ≤ 100°C			10	
DC Primary Input Current	$I_{PRI\_IN\_DC}$	At $I_{SEC\_OUT\_DC}$ = 62.5A, $T_{INTERNAL}$ ≤ 100°C			4.0	A
Transformation Ratio	K	Primary to secondary, K = V_{SEC_DC} / V_{PRI_DC}, at no load		1/16		V/V
Secondary Output Current (continuous)	$I_{SEC\_OUT\_DC}$				62.5	A
Secondary Output Current (pulsed)	$I_{SEC\_OUT\_PULSE}$	2 ms pulse, 25% Duty cycle, $I_{SEC\_OUT\_AVG}$ ≤ 50% rated $I_{SEC\_OUT\_DC}$			75	A
PRI to SEC Efficiency (ambient)	η_{AMB}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 62.5A	96.4	97.2		%
		V_{PRI_DC} = 260V to 410V, $I_{SEC\_OUT\_DC}$ = 62.5A	95.5			
		V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 31.25A	96.5	97.3		
PRI to SEC Efficiency (hot)	η_{HOT}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 62.5A	96.3	96.7		%
PRI to SEC Efficiency (over load range)	$\eta_{20\%}$	12.5A < $I_{SEC\_OUT\_DC}$ < 62.5A	90			%
PRI to SEC Output Resistance	R_{SEC_COLD}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 62.5A, $T_{INTERNAL}$ = -55°C	3	5	7	mΩ
	R_{SEC_AMB}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 62.5A	5	7	9	
	R_{SEC_HOT}	V_{PRI_DC} = 384V, $I_{SEC\_OUT\_DC}$ = 62.5A, $T_{INTERNAL}$ = 100°C	6.5	8.5	10.5	
Switching Frequency	F_{SW}	Frequency of the Output Voltage Ripple = 2x F_{SW}	**1.00**	1.05	**1.10**	MHz
Secondary Output Voltage Ripple	$V_{SEC\_OUT\_PP}$	C_{SEC_EXT} = 0µF, $I_{SEC\_OUT\_DC}$ = 62.5A, V_{PRI_DC} = 384V, 20MHz BW		150		mV
		$T_{INTERNAL}$ ≤ 100°C			250	
Primary Input Leads Inductance (Parasitic)	$L_{PRI\_IN\_LEADS}$	Frequency 2.5MHz (double switching frequency), Simulated lead model		7		nH
Secondary Output Leads Inductance (Parasitic)	$L_{SEC\_OUT\_LEADS}$	Frequency 2.5MHz (double switching frequency), Simulated lead model		0.64		nH

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powetrain PRIMARY to SECONDARY Specification (Forward Direction) Cont.						
Effective Primary Capacitance (Internal)	C_{PRI_INT}	Effective Value at 384V_{PRI_DC}		0.37		µF
Effective Secondary Capacitance (Internal)	C_{SEC_INT}	Effective Value at 24V_{SEC_DC}		70		µF
Effective Secondary Output Capacitance (External)	$C_{SEC\_OUT\_EXT}$	Excessive capacitance may drive module into SC protection			**1000**	µF
Effective Secondary Output Capacitance (External)	$C_{SEC\_OUT\_AEXT}$	$C_{SEC\_OUT\_AEXT}$ Max = N * 0.5 * $C_{SEC\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Protection PRIMARY to SECONDARY (Forward Direction)						
Auto Restart Time	$t_{AUTO\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given V_{PRI_DC} > V_{PRI_UVLO+}	**490**		**560**	ms
Primary Overvoltage Lockout Threshold	V_{PRI_OVLO+}		**420**	435	**450**	V
Primary Overvoltage Recovery Threshold	V_{PRI_OVLO-}		**410**	425	**440**	V
Primary Overvoltage Lockout Hysteresis	$V_{PRI\_OVLO\_HYST}$			10		V
Primary Overvoltage Lockout Response Time	t_{PRI_OVLO}			100		µs
Primary Soft-Start Time	$t_{PRI\_SOFT-START}$	From powertrain active. Fast Current limit protection disabled during Soft-Start		1		ms
Secondary Output Overcurrent Trip Threshold	$I_{SEC\_OUT\_OCP}$		**75**	84	**100**	A
Secondary Output Overcurrent Response Time Constant	$t_{SEC\_OUT\_OCP}$	Effective internal RC filter		3		ms
Secondary Output Short Circuit Protection Trip Threshold	$I_{SEC\_OUT\_SCP}$		**94**			A
Secondary Output Short Circuit Protection Response Time	$t_{SEC\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits PRIMARY to SECONDARY (Forward Direction)						
Primary Overvoltage Lockout Threshold	V_{PRI_OVLO+}		**420**	435	**450**	V
Primary Overvoltage Recovery Threshold	V_{PRI_OVLO-}		**410**	425	**440**	V
Primary Overvoltage Lockout Hysteresis	$V_{PRI\_OVLO\_HYST}$			10		V
Primary Overvoltage Lockout Response Time	t_{PRI_OVLO}			100		µs
Primary Undervoltage Lockout Threshold	V_{PRI_UVLO-}		**200**	225	**250**	V
Primary Undervoltage Recovery Threshold	V_{PRI_UVLO+}		**220**	240	**259**	V
Primary Undervoltage Lockout Hysteresis	$V_{PRI\_UVLO\_HYST}$			15		V
Primary Undervoltage Lockout Response Time	t_{PRI_UVLO}			100		µs
Primary Undervoltage Startup Delay	$t_{PRI\_UVLO+\_DELAY}$	From V_{PRI_DC} = V_{PRI_UVLO+} to powertrain active, EN floating, (i.e One time Startup delay from application of V_{PRI_DC} to V_{SEC_DC})		20		ms
Secondary Output Overcurrent Trip Threshold	$I_{SEC\_OUT\_OCP}$		**83**	88	**93**	A
Secondary Output Overcurrent Response Time Constant	$t_{SEC\_OUT\_OCP}$	Effective internal RC filter		3		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C
Overtemperature Recovery Threshold	t_{OTP-}		105	110	115	°C
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC; Protection not available for M-Grade units.			-45	°C
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given V_{PRI_DC} > V_{PRI_UVLO+}		3		s

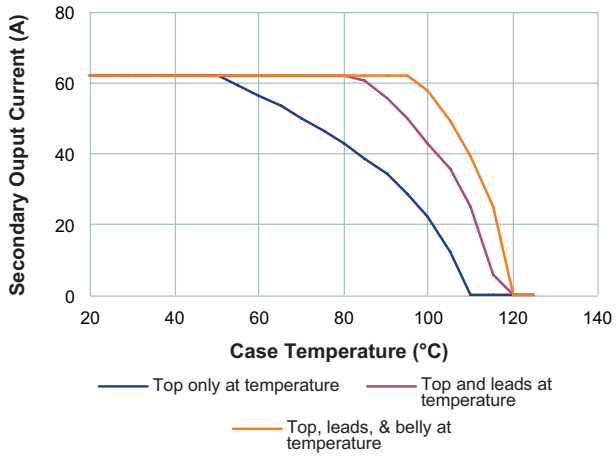


Figure 1 — *Specified thermal operating area*

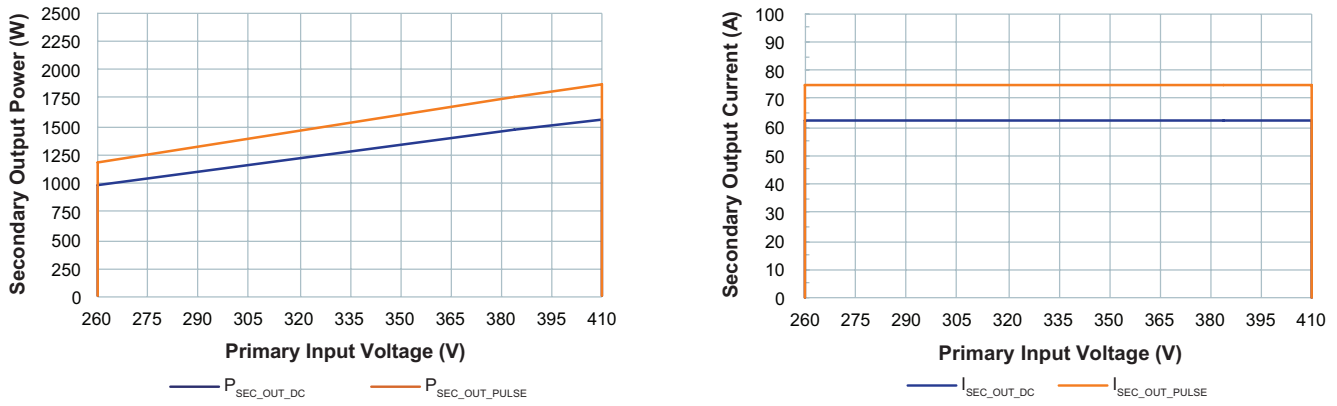


Figure 2 — *Specified electrical operating area using rated R_{SEC_HOT}*

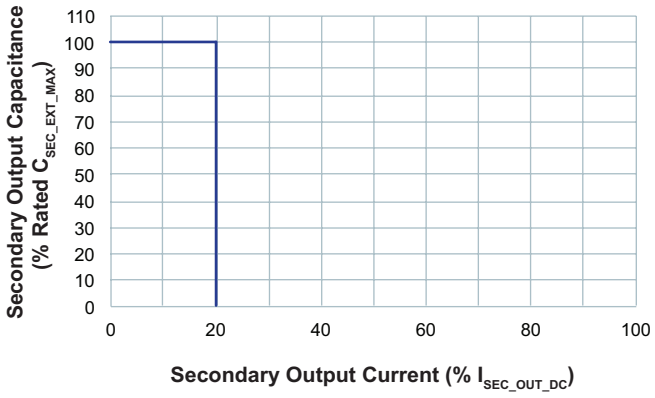


Figure 3 — *Specified Primary start-up into load current and external capacitance*

Analog Control Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Temperature Monitor								
• The TM pin is a standard analog I/O configured as an output from an internal µC. • The TM pin monitors the internal temperature of the controller IC within an accuracy of ±5°C. • µC 250kHz PWM output internally pulled high to 3.3V.								
SIGNAL TYPE	**STATE**	**ATTRIBUTE**	**SYMBOL**	**CONDITIONS / NOTES**	**MIN**	**TYP**	**MAX**	**UNIT**
DIGITAL OUTPUT	Startup	Powertrain active to TM time	t_{TM}			**100**		µs
	Regular Operation	TM Duty Cycle	TM_{PWM}		**18.18**		**68.18**	%
		TM Current	I_{TM}				**4**	mA
		Recommended External filtering						
		TM Capacitance (External)	C_{TM_EXT}	Recommended External filtering		0.01		µF
		TM Resistance (External)	R_{TM_EXT}	Recommended External filtering		1		kΩ
		Specifications using recommended filter						
		TM Gain	A_{TM}			10		mV / °C
		TM Voltage Reference	V_{TM_AMB}			1.27		V
		TM Voltage Ripple	V_{TM_PP}	R_{TM_EXT} = 1K Ohm, C_{TM_EXT} = 0.01µF, V_{PRI_DC} = 384V, I_{SEC_DC} = 62.5A		28		mV
				$T_{INTERNAL}$ ≤ 100°C			40	

Enable / Disable Control								
• The EN pin is a standard analog I/O configured as an input to an internal µC. • It is internally pulled high to 3.3V. • When held low the BCM internal bias will be disabled and the powertrain will be inactive. • In an array of BCMs, EN pins should be interconnected to synchronize startup.								
SIGNAL TYPE	**STATE**	**ATTRIBUTE**	**SYMBOL**	**CONDITIONS / NOTES**	**MIN**	**TYP**	**MAX**	**UNIT**
ANALOG INPUT	Startup	EN to Powertrain active time	t_{EN_START}	V_{PRI_DC} > V_{PRI_UVLO+}, EN held low both conditions satisfied for T > $t_{PRI\_UVLO+\_DELAY}$		**250**		µs
	Regular Operation	EN Voltage Threshold	V_{EN_TH}		**2.3**			V
		EN Resistance (Internal)	R_{EN_INT}	Internal pull up resistor		1.5		kΩ
		EN Disable Threshold	$V_{EN\_DISABLE\_TH}$				**1**	V

Analog Control Signal Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Auxiliary Voltage Source

- The VAUX pin is a standard analog I/O configured as an output from an internal µC.
- VAUX is internally connected to µC output as internally pulled high to a 3.3V regulator with 2% tolerance, a 1% resistor of 1.5kΩ.
- VAUX can be used as a "Ready to process full power" flag. This pin transitions VAUX voltage after a 2ms delay from the start of powertrain activating, signaling the end of softstart.
- VAUX can be used as "Fault flag". This pin is pulled low internally when a fault protection is detected.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Startup	Powertrain active to VAUX time	t_{VAUX}	Powertrain active to VAUX High		**2**		ms
	Regular Operation	VAUX Voltage	V_{VAUX}		**2.8**		**3.3**	V
		VAUX Available Current	I_{VAUX}				**4**	mA
		VAUX Voltage Ripple	V_{VAUX_PP}			50		mV
				$T_{INTERNAL}$ ≤ 100°C			**100**	
		VAUX Capacitance (External)	C_{VAUX_EXT}				0.01	µF
		VAUX Resistance (External)	R_{VAUX_EXT}	$V_{PRI\_DC} < V_{µC\_ACTIVE}$	1.5			kΩ
	Fault	VAUX Fault Response Time	t_{VAUX_FR}	From fault to V_{VAUX} = 2.8V, C_{VAUX} = 0pF		10		µs

PMBus™ Control Signal Characteristics

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UART SER-IN / SER-OUT Pins

- Universal Asynchronous Receiver/Transmitter (UART) pins.
- The BCM communication version is not intended to be used without a Digital Supervisor.
- Isolated I^2C communication and telemetry is available when using Vicor Digital Isolator and Vicor Digital Supervisor. Please see specific product data sheet for more details.
- UART SER-IN pin is internally pulled high using a 1.5kΩ to 3.3V.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
GENERAL I/O	Regular Operation	Baud Rate	BR_{UART}	Rate		**750**		Kbit/s
DIGITAL INPUT		**SER-IN Pin**						
		SER-IN Input Voltage Range	V_{SER-IN_IH}		2.3			V
			V_{SER-IN_IL}				1	V
		SER-IN rise time	t_{SER-IN_RISE}	10% to 90%		400		ns
		SER-IN fall time	t_{SER-IN_FALL}	10% to 90%		25		ns
		SER-IN R_{PULLUP}	R_{SER-IN_PLP}	Pull up to 3.3V		1.5		kΩ
		SER-IN External Capacitance	C_{SER-IN_EXT}				400	pF
DIGITAL OUTPUT		**SER-OUT Pin**						
		SER-OUT Output Voltage Range	$V_{SER-OUT\_OH}$	0mA ≥ I_{OH} ≥ -4mA	2.8			V
			$V_{SER-OUT\_OL}$	0mA ≤ I_{OL} ≤ 4mA			0.5	V
		SER-OUT rise time	$t_{SER-OUT\_RISE}$	10% to 90%		55		ns
		SER-OUT fall time	$t_{SER-OUT\_FALL}$	10% to 90%		45		ns
		SER-OUT source current	$I_{SER-OUT}$	$V_{SER-OUT}$ = 2.8V			6	mA
		SER-OUT output impedance	$Z_{SER-OUT}$			**120**		Ω

Enable / Disable Control

- The EN pin is a standard analog I/O configured as an input to an internal µC.
- It is internally pulled high to 3.3V.
- When held low the BCM internal bias will be disabled and the powertrain will be inactive.
- In an array of BCMs, EN pins should be interconnected to synchronize startup.
- Enable / disable command will have no effect if the EN pin is disabled.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Startup	EN to Powertrain active time	t_{EN_START}	V_{PRI_DC} > V_{PRI_UVLO+}, EN held low both conditions satisfied for t > $t_{PRI\_UVLO+\_DELAY}$		**250**		µs
	Regular Operation	EN Voltage Threshold	V_{ENABLE}		**2.3**			V
		EN Resistance (Internal)	R_{EN_INT}	Internal pull up resistor		1.5		kΩ
		EN Disable Threshold	$V_{EN\_DISABLE\_TH}$				1	V

PMBus™ Reported Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

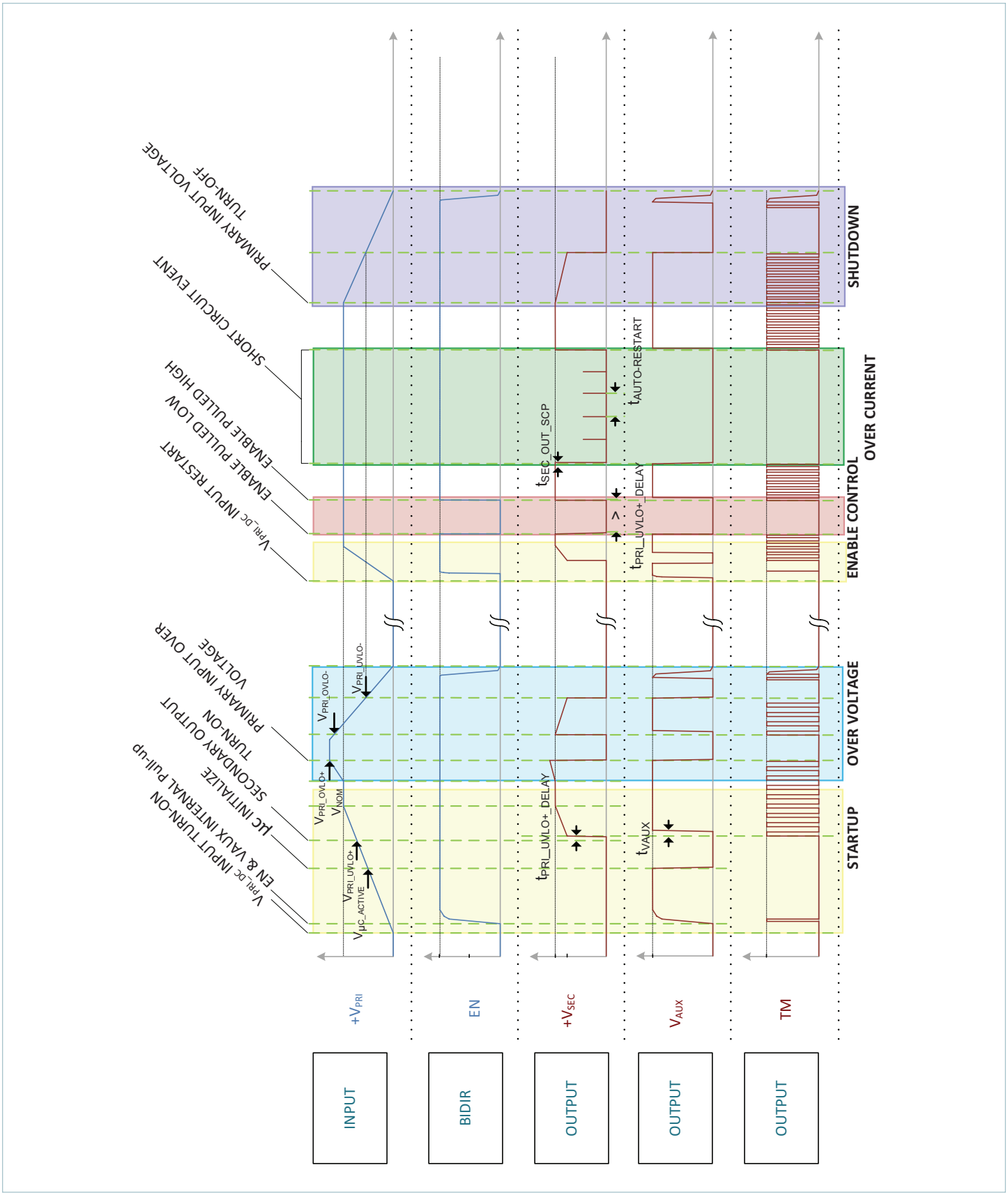
Monitored Telemetry					
• The BCM communication version is not intended to be used without a Digital Supervisor.					
ATTRIBUTE	**DIGITAL SUPERVISOR PMBus™ READ COMMAND**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**UPDATE RATE**	**REPORTED UNITS**
Input voltage	(88h) READ_VIN	± 5% (LL - HL)	130V to 450V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Input current	(89h) READ_IIN	± 5% (10 - 133% of FL)	-5.9A to 5.9A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-3}$
Output voltage[1]	(8Bh) READ_VOUT	± 5% (LL - HL)	8.0V to 28.0V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Output current	(8Ch) READ_IOUT	± 5% (10 - 133% of FL)	-87.5A to 87.5A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
Output resistance	(D4h) READ_ROUT	± 5% (50 - 100% of FL)	500µΩ to 15mΩ	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature[2]	(8Dh) READ_TEMPERATURE_1	± 7°C (Full Range)	- 55°C to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[1] Default READ Output Voltage returned when unit is disabled = -300 V.
[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameter					
• Factory setting of all below Thresholds and Warning limits are 100% of listed protection values. • Variables can be written only when module is disabled either EN pulled low or $V_{IN} < V_{IN\_UVLO-}$. • Module must remain in a disabled mode for 3 ms after any changes to the below variables allowing ample time to commit changes to EEPROM.					
ATTRIBUTE	**DIGITAL SUPERVISOR PMBus™ COMMAND [3]**	**CONDITIONS / NOTES**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**DEFAULT VALUE**
Input / Output Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{IN_OVLO-} is automatically 3% lower than this set point	± 5% (LL - HL)	130V to 435V	100%
Input / Output Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5% (LL - HL)	130V to 435V	100%
Input / Output Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5% (LL - HL)	130V or 260V	100%
Input Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		± 5% (10 - 133% of FL)	0 to 5.5A	100%
Input Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 5% (10 - 133% of FL)	0 to 5.5A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT		± 7°C (Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT		± 7°C (Full Range)	0 to 125°C	100%
Turn on Delay	(60h) TON_DELAY	Additional time delay to the Undervoltage Startup Delay	± 50µs	0 to 100ms	0ms

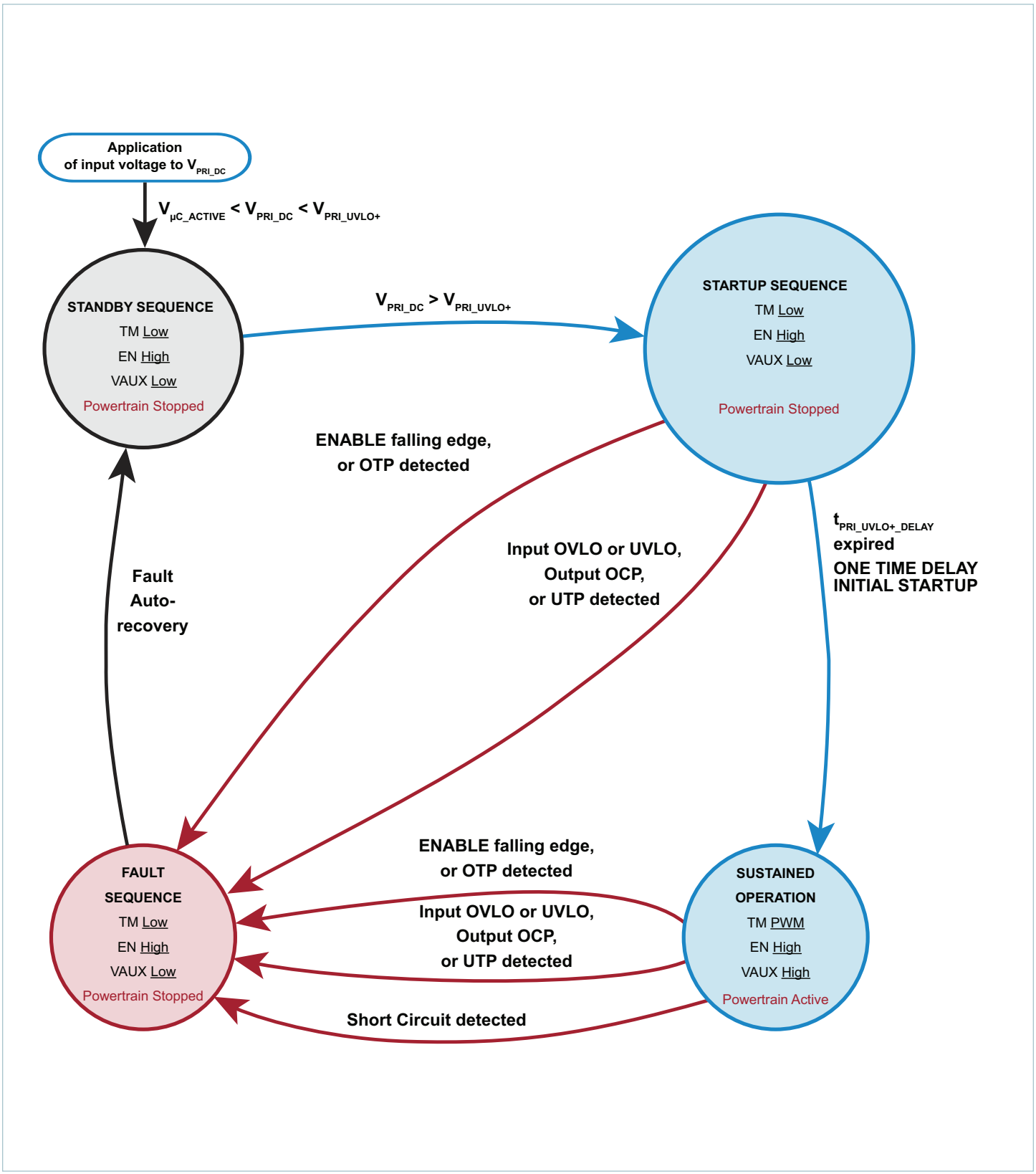
[3] Refer to Digital Supervisor datasheet for complete list of supported commands.

BCM Module Timing Diagram



High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



Application Characteristics

Product is mounted and temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected data from primary sourced units processing power in forward direction.See associated figures for general trend data.

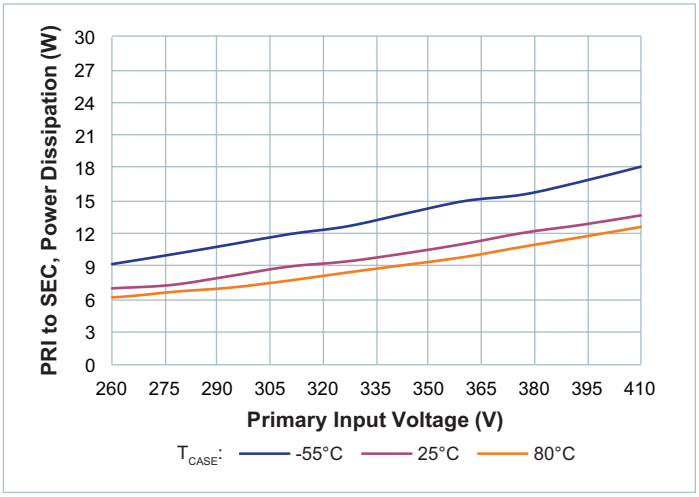


Figure 4 — *No load power dissipation vs. V_{PRI_DC}*

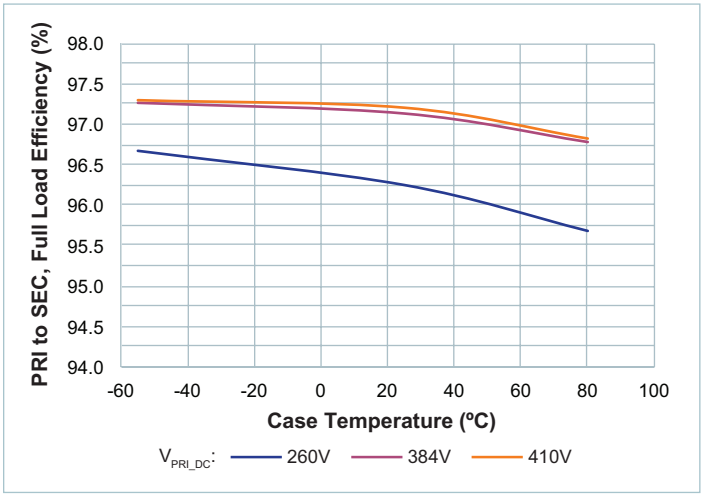


Figure 5 — *Full load efficiency vs. temperature; V_{PRI_DC}*

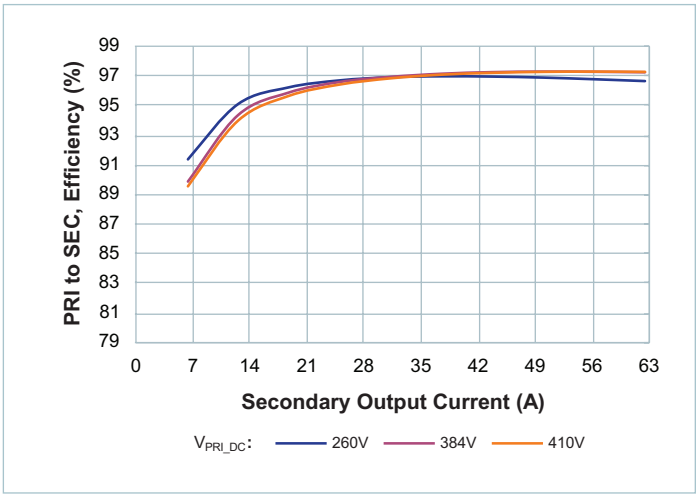


Figure 6 — *Efficiency at T_{CASE} = -55°C*

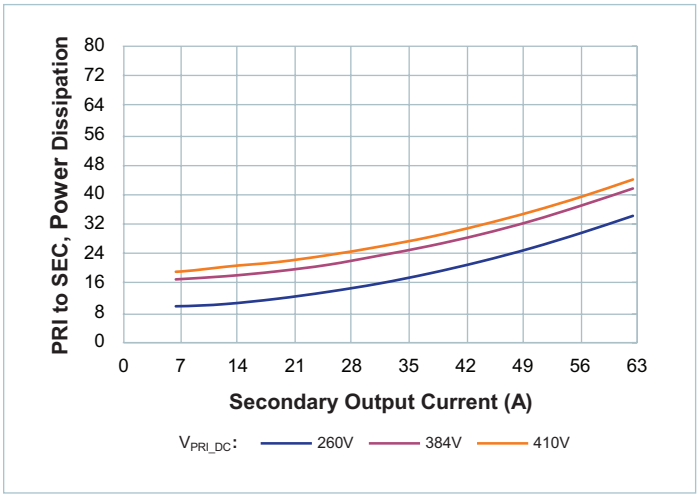


Figure 7 — *Power dissipation at T_{CASE} = -55°C*

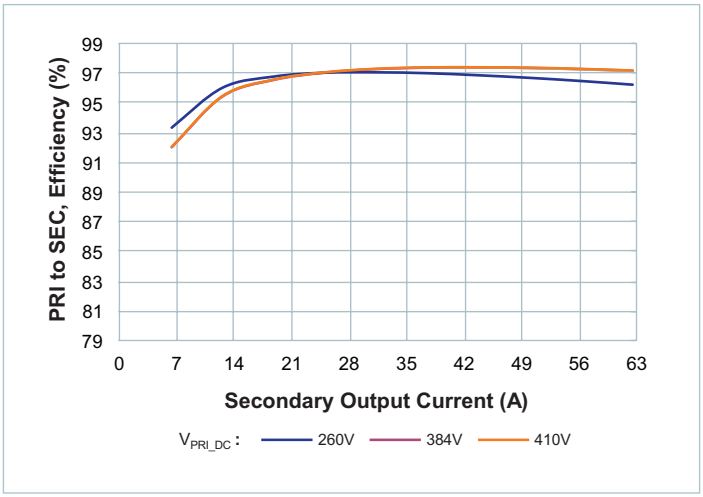


Figure 8 — *Efficiency at T_{CASE} = 25°C*

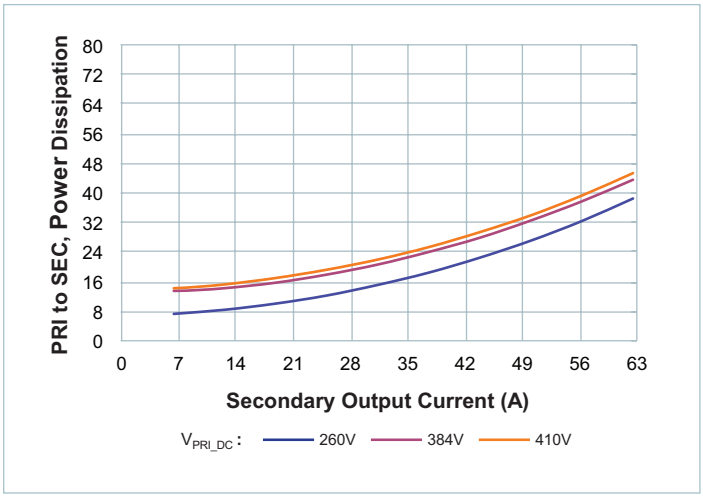


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

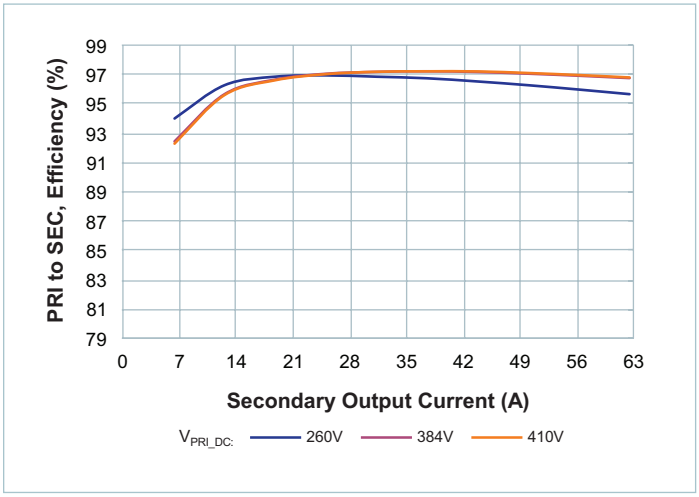


Figure 10 — *Efficiency at T_{CASE} = 80°C*

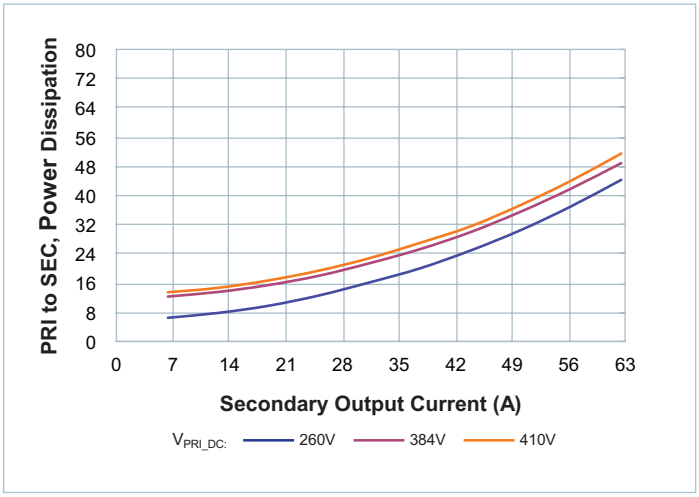


Figure 11 — *Power dissipation at T_{CASE} = 80°C*

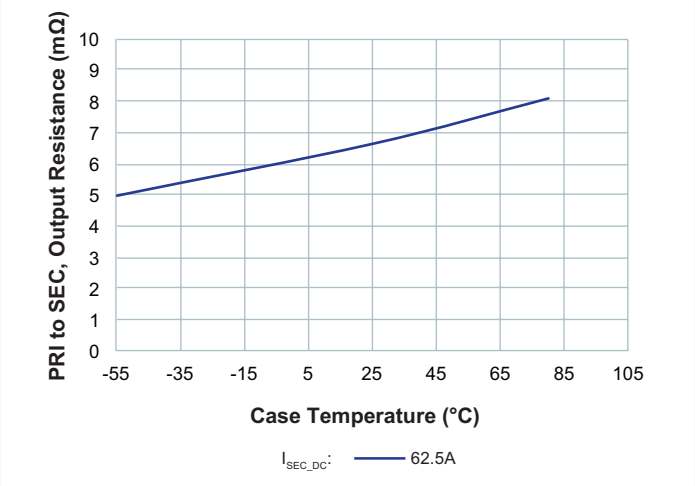


Figure 12 — *R_{SEC} vs. temperature; Nominal V_{PRI_DC} I_{SEC_DC} = 62.5A at T_{CASE} = 80°C*

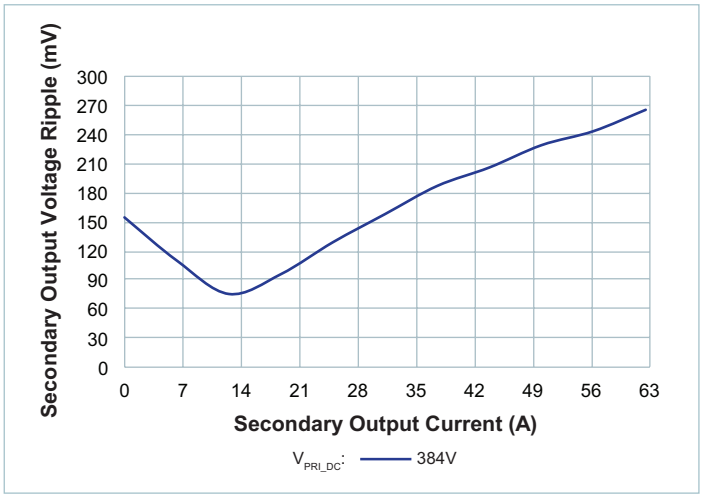


Figure 13 — *$V_{SEC\_OUT\_PP}$ vs. I_{SEC_DC} ; No external $C_{SEC\_OUT\_EXT.}$ Board mounted module, scope setting : 20MHz analog BW*

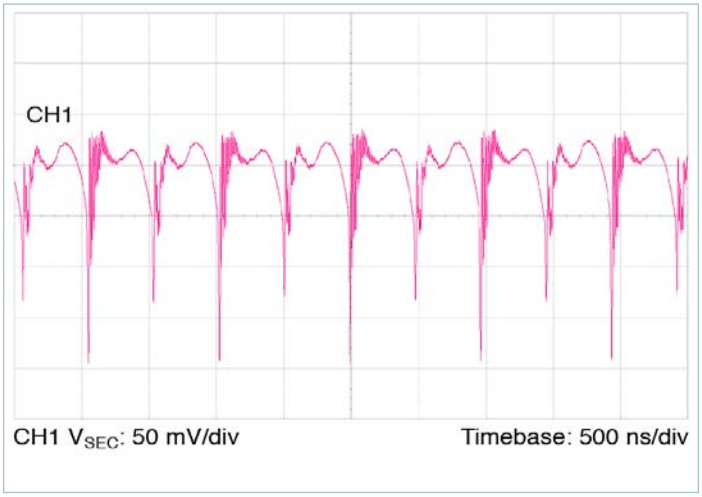


Figure 14 — *Full load ripple, 10µF $C_{PRI\_IN\_EXT}$; No external $C_{SEC\_OUT\_EXT}$. Board mounted module, scope setting: 20MHz analog BW*

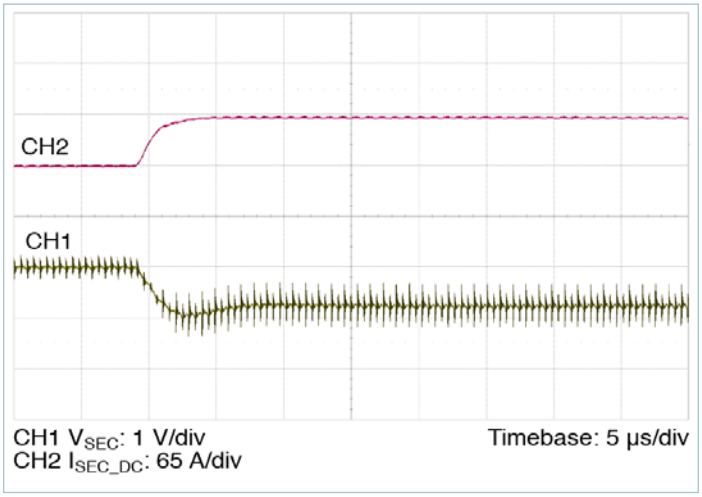


Figure 15 — *0 A– 62.5 A transient response: $C_{PRI\_IN\_EXT}$ = 10 µF, no external $C_{SEC\_OUT\_EXT}$*

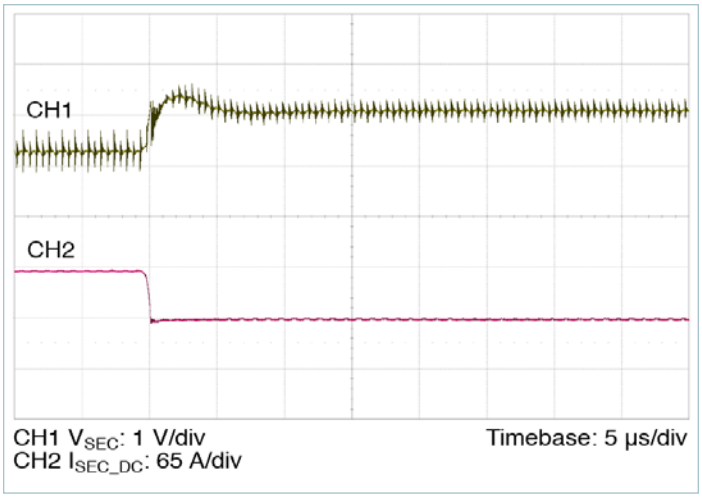


Figure 16 — *62.5A – 0A transient response: $C_{PRI\_IN\_EXT}$ = 10µF, no external $C_{SEC\_OUT\_EXT}$*

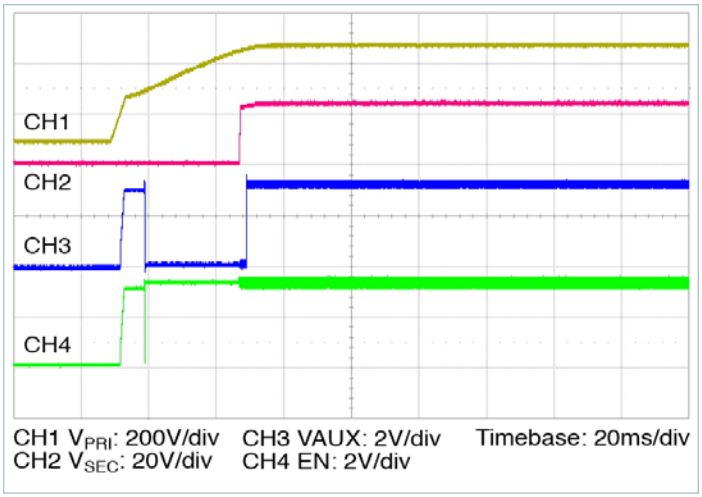


Figure 17 — *Start up from application of V_{PRI_DC}= 384V, 20% I_{SEC_DC}, 100% $C_{SEC\_OUT\_EXT}$*

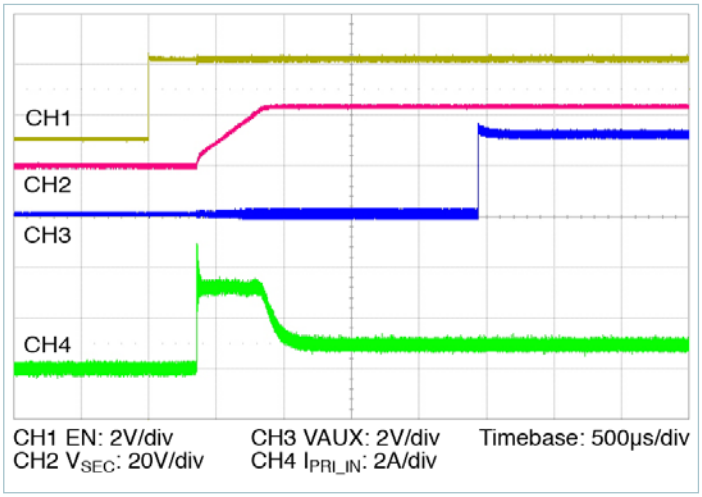


Figure 18 — *Start up from application of EN with pre-applied V_{PRI_DC} = 384V, 20% I_{SEC_DC}, 100% $C_{SEC\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		60.87 / [2.396]	61.00 / [2.402]	61.13 / [2.407]	mm/[in]
Width	W		24.76 / [0.975]	25.14 / [0.990]	25.52 / [1.005]	mm/[in]
Height	H		7.21 / [0.284]	7.26 / [0.286]	7.31 / [0.288]	mm/[in]
Volume	Vol	Without Heatsink		11.13 / [0.679]		cm^3/[in^3]
Weight	W			41 / [1.45]		g/[oz]
Lead finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating Temperature	$T_{INTERNAL}$	BCM6123xD1E2662yzz (T-Grade)	-40		125	°C
		BCM6123xD1E2662yzz (M-Grade)	-55		125	°C
Thermal Resistance Top Side	$\eta_{INT-TOP}$	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.45		°C/W
Thermal Resistance Leads	$\eta_{INT-LEADS}$	Estimated thermal resistance to maximum temperature internal component from isothermal leads		1.77		°C/W
Thermal Resistance Bottom Side	$\eta_{INT-BOTTOM}$	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		1.67		°C/W
Thermal Capacity				34		Ws/°C
Assembly						
Storage temperature		BCM6123xD1E2662yzz (T-Grade)	-55		125	°C
		BCM6123xD1E2662yzz (M-Grade)	-65		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)				
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)				

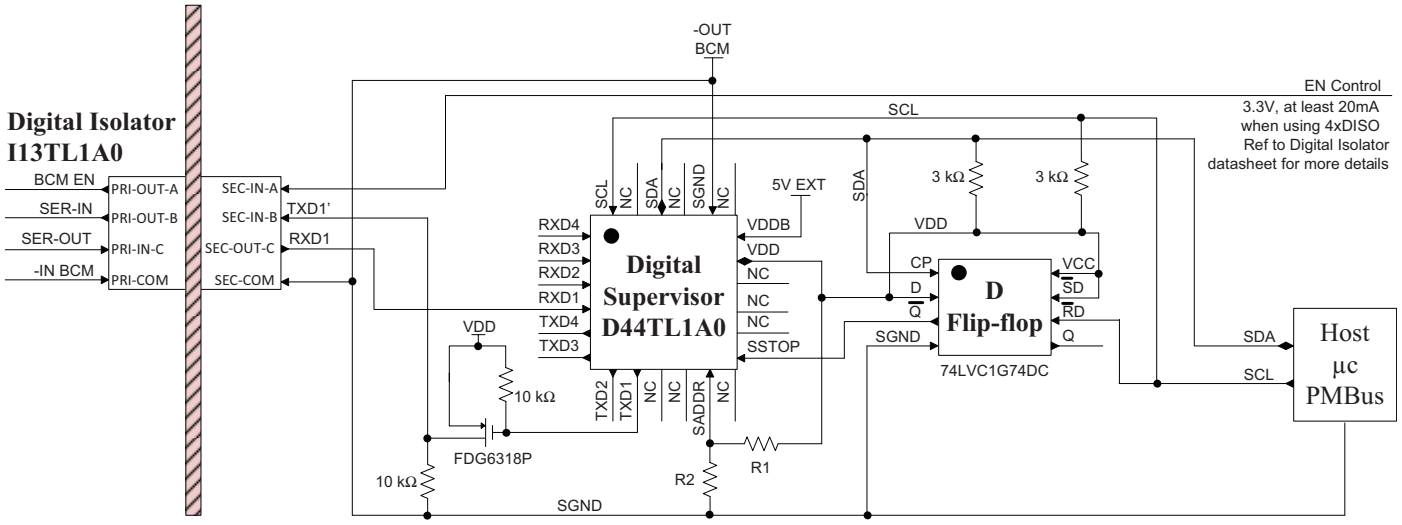
General Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -55°C ≤ $T_{INTERNAL}$ ≤ 125°C (M-Grade); All other specifications are at $T_{INTERNAL}$ = 25ºC unless otherwise noted.

Soldering[1]						
Peak Temperature Top Case					135	°C
Safety						
Isolation voltage / Dielectric test	V_{HIPOT}	PRIMARY to SECONDARY	**4,242**			V_{DC}
		PRIMARY to CASE	**2,121**			
		SECONDARY to CASE	**2,121**			
Isolation Capacitance	C_{PRI_SEC}	Unpowered Unit	**620**	780	**940**	pF
Insulation Resistance	R_{PRI_SEC}	At 500 Vdc	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		2.31		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.41		MHrs
Agency Approvals / Standards		cTUVus "EN 60950-1"				
		60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

[1] Product is not intended for reflow solder attach.

PMBus™ System Diagram



The PMBus communication enabled bus converter provides accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags.

The BCM internal µC is referenced to primary ground. The Digital Isolator allows UART communication interface with the host Digital Supervisor at typical speed of 750KHz across the isolation barrier. One of the advantages of the Digital Isolator is its low power consumption. Each transmission channel is able to draw its internal bias circuitry directly from the input signal being transmitted to the output with minimal to no signal distortion.

The Digital Supervisor provides the host system µC with access to an array of up to 4 BCMs. This array is constantly polled for status by the Digital Supervisor. Direct communication to individual BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the Digital Supervisor data and pages (0x01 – 0x04) prior to a telemetry inquiry points to the array of BCMs connected data. The Digital Supervisor constantly polls the BCM data through the UART interface.

The Digital Supervisor enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The Digital Supervisor follows the PMBus command structure and specification.

Please refer to the Digital Supervisor data sheet for more details.

Sine Amplitude Converter™ Point of Load Conversion

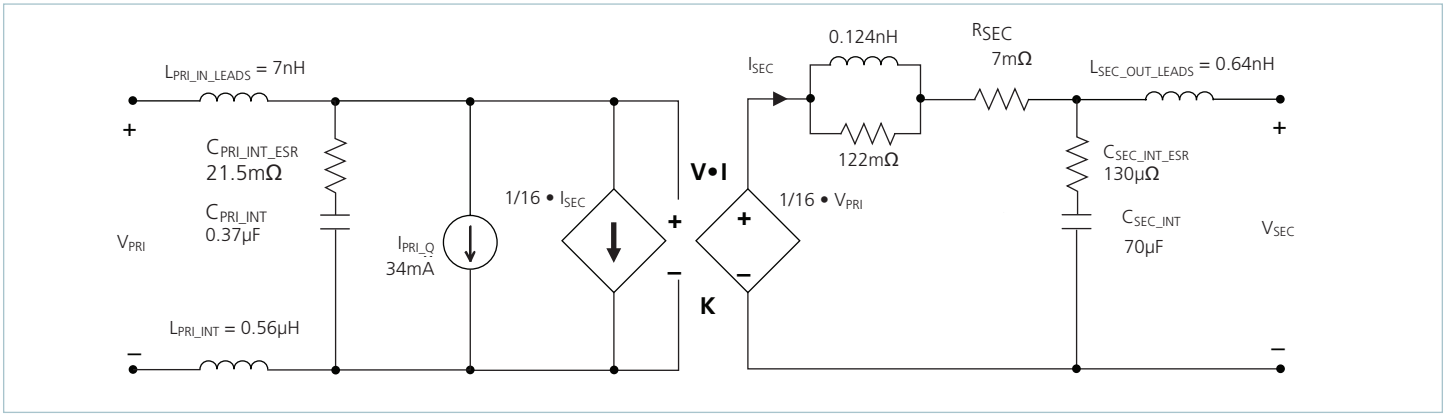


Figure 19 — *BCM module AC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from Primary to secondary and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of primary voltage and secondary current. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM6123xD1E2662yzz SAC can be simplified into the preceeding model.

At no load:

$$V_{SEC} = V_{PRI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC. Rearranging Eq (1):

$$K = \frac{V_{SEC}}{V_{PRI}} \qquad (2)$$

In the presence of load, V_{SEC} is represented by:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R_{SEC} \qquad (3)$$

and I_{SEC} is represented by:

$$I_{SEC} = \frac{I_{PRI} - I_{PRI\_Q}}{K} \qquad (4)$$

R_{SEC} represents the impedance of the SAC, and is a function of the R_{DSON} of the primary and secondary MOSFETs and the winding resistance of the power transformer. I_{PRI_Q} represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that R_{SEC} = 0Ω and I_{PRI_Q} = 0A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{PRI}.

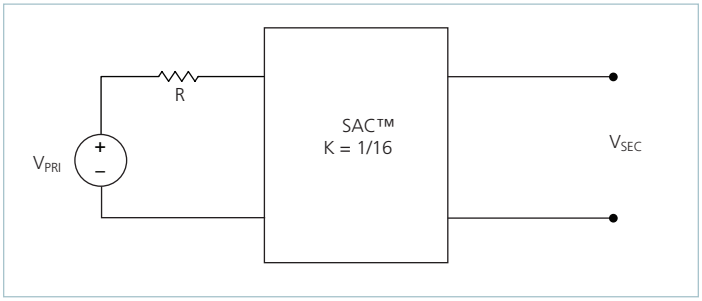


Figure 20 — *K = 1/16 Sine Amplitude Converter with series primary resistor*

The relationship between V_{PRI} and V_{SEC} becomes:

$$V_{SEC} = (V_{PRI} - I_{PRI} \bullet R) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_{PRI_Q} is assumed = 0A) into Eq. (5) yields:

$$V_{SEC} = V_{PRI} \bullet K - I_{SEC} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{SEC} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the primary side of the SAC is effectively scaled by K^2 with respect to the secondary.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 3.91mΩ, with K = 1/16.

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the primary of the SAC. A switch in series with V_{PRI} is added to the circuit. This is depicted in Figure 21.

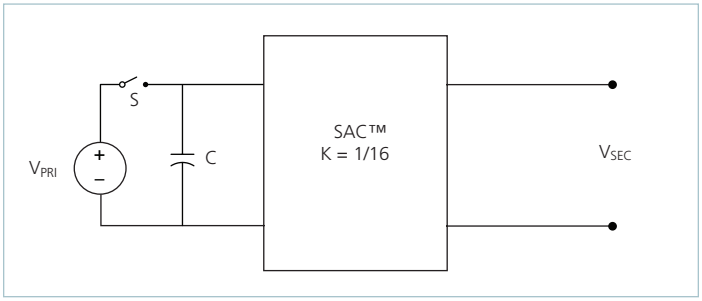


Figure 21 — *Sine Amplitude Converter with primary capacitor*

A change in V_{PRI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{PRI}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{PRI}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{SEC} \bullet K \quad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{SEC} = \frac{C}{K^2} \bullet \frac{dV_{SEC}}{dt} \quad (9)$$

The equation in terms of the secondary has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the secondary when expressed in terms of the primary. With a K= 1/16 as shown in Figure 21, C = 1µF would appear as C = 256µF when viewed from the secondary.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{PRI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{SEC}}$): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{PRI\_NL} + P_{R_{SEC}} \quad (10)$$

Therefore,

$$P_{SEC\_OUT} = P_{PRI\_IN} - P_{DISSIPATED} = P_{PRI\_IN} - P_{PRI\_NL} - P_{R_{SEC}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{SEC\_OUT}}{P_{PRI\_IN}} = \frac{P_{PRI\_IN} - P_{PRI\_NL} - P_{R_{SEC}}}{P_{PRI\_IN}} \quad (12)$$

$$= \frac{V_{PRI} \bullet I_{PRI} - P_{PRI\_NL} - (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}}$$

$$= 1 - \left(\frac{P_{PRI\_NL} + (I_{SEC})^2 \bullet R_{SEC}}{V_{PRI} \bullet I_{PRI}} \right)$$

Input and Output Filter Design

A major advantage of SAC™ systems versus conventional PWM converters is that the transformer based SAC does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of primary voltage and secondary current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the primary and secondary stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:

  To take full advantage of the BCM module's dynamic response, the impedance presented to its primary terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the primary should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- Further reduce primary and/or secondary voltage ripple without sacrificing dynamic response:

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the primary source will appear at the secondary of the module multiplied by its K factor.

- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:

  The module primary/secondary voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating primary range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Total load capacitance at the secondary of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and low secondary impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the primary of the module. At frequencies <500kHz the module appears as an impedance of R_{SEC} between the source and load.

Within this frequency range, capacitance at the primary appears as effective capacitance on the secondary per the relationship defined in Eq. (13).

$$C_{SEC\_EXT} = \frac{C_{PRI\_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum current that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for a VI Chip® BCM module 6123 in an application where the top, bottom, and leads are cooled. In this case, the BCM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP}, T_{CASE_BOTTOM}, and T_{LEADS}. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation would provide an estimate of heat flow through the various pathways as well as internal temperature.

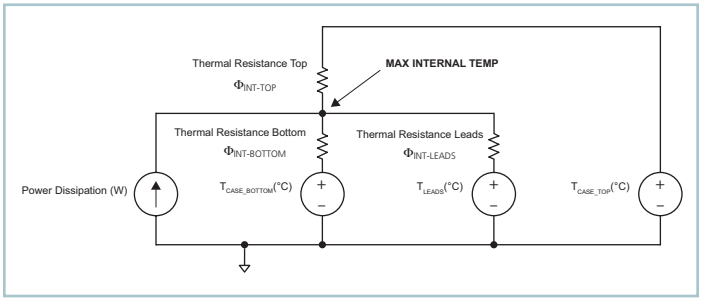


Figure 22 *— Top case, Bottom case and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE\_TOP}$$
$$T_{INT} - PD_2 \bullet \Phi_{INT\text{-}BOTTOM} = T_{CASE\_BOTTOM}$$
$$T_{INT} - PD_3 \bullet \Phi_{INT\text{-}LEADS} = T_{LEADS}$$
$$PD_{TOTAL} = PD_1 + PD_2 + PD_3$$

Where T_{INT} represents the internal temperature and PD_1, PD_2, and PD_3 represent the heat flow through the top side, bottom side, and leads respectively.

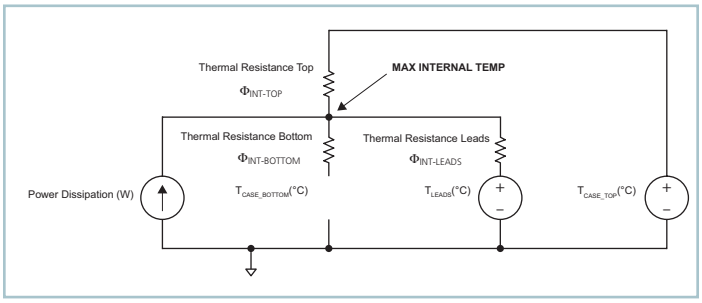


Figure 23 *— Top case and leads thermal model*

Figure 23 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$T_{INT} - PD_3 \bullet \Phi_{INT\text{-}LEADS} = T_{LEADS}$$

$$PD_{TOTAL} = PD_1 + PD_3$$

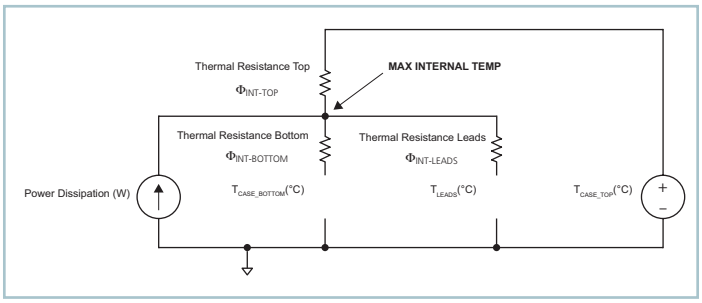


Figure 24 — *Top case thermal model*

Figure 24 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow paths to the bottom and leads are left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE\_TOP}$$

$$PD_{TOTAL} = PD_1$$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a BCM thermal configuration is valid for a given condition. These tools can be found at: http://www.vicorpower.com/powerbench.

Current Sharing

The performance of the SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- An input filter is required for an array of BCMs in order to prevent circulating currents.

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

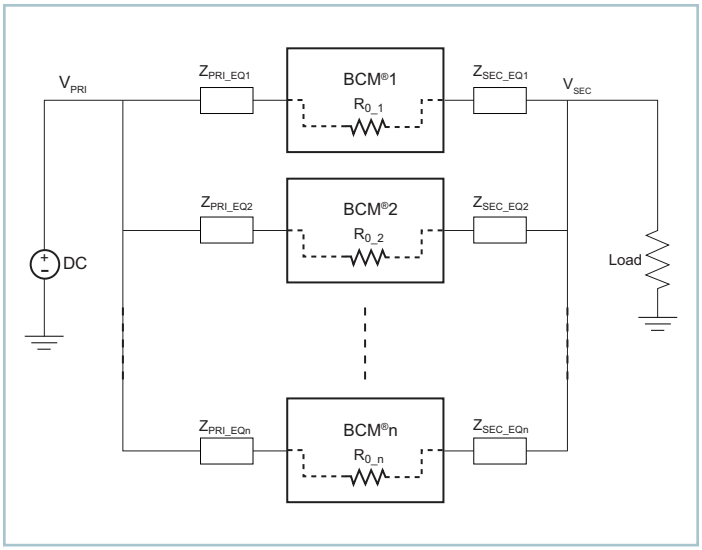


Figure 25 — *BCM module array*

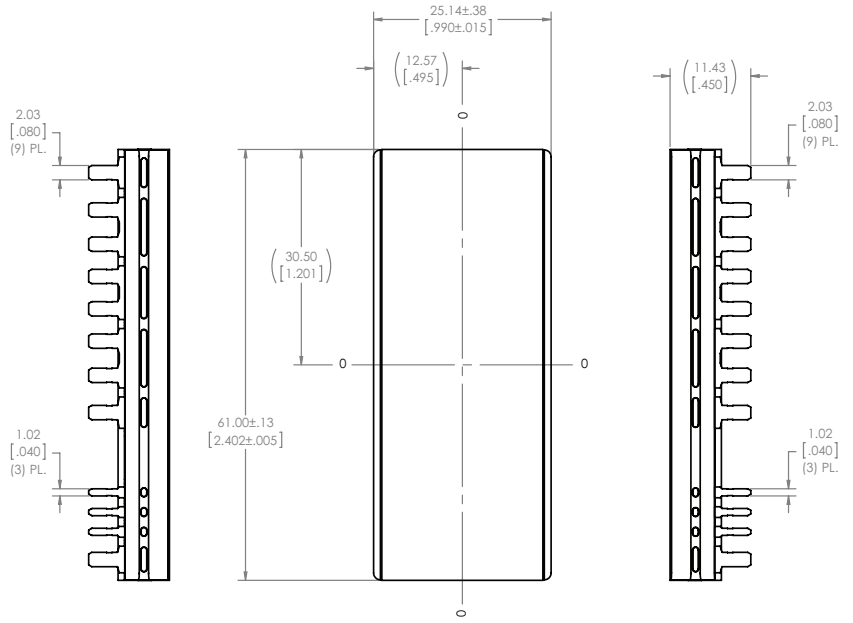
Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

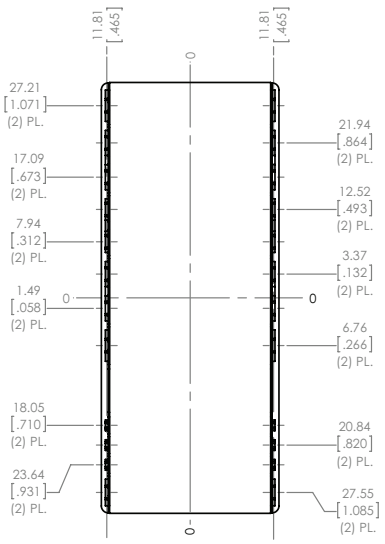
The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤ 5A Bussmann PC-Tron (primary side)

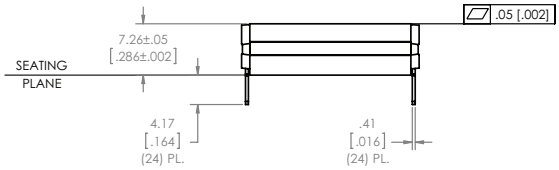
BCM Module Through Hole Package Mechanical Drawing and Recommended Land Pattern



TOP VIEW (COMPONENT SIDE)

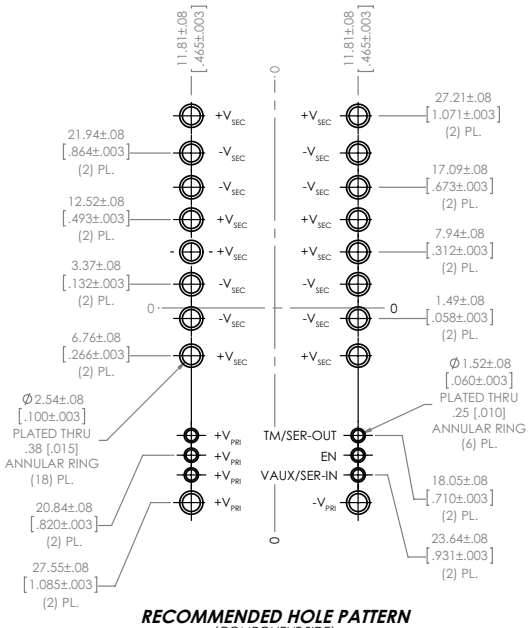


BOTTOM VIEW



NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2- UNLESS SPECIFIED OTHERWISE, DIMENSIONS ARE MM / [INCH], TOLERANCE ± 0.127 / [0.005]



RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)

Revision History

Revision	Date	Description	Page Number(s)
1.0	07/15/16	Initial Release	n/a

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