

LPDDR5X SDRAM

**MT62F1G16D1, MT62F1G32D2, MT62F2G32D4,
MT62F4G32D8, MT62F1G64D4, MT62F2G64D8**

Features

- **Architecture**
 - 17.1 GB/s maximum bandwidth per channel
 - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mb/s with WCK:CK = 4:1)
 - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X/LPDDR5 data interface**
 - Single x16 channel/die
 - Double-data-rate command/address entry
 - Differential command clocks (CK_t/CK_c) for high-speed operation
 - Differential data clocks (WCK_t/WCK_c)
 - Optional differential read strobe (RDQS_t/RDQS_c)
 - 16n-bit or 32n-bit prefetch architecture
 - Bank Architecture: 8-bank (8B) mode, bank group (BG) mode, and 16-bank (16B) mode supported
 - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
 - Background ZQ calibration/command-based ZQ calibration
 - Optional link protection (link ECC)
 - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
 - V_{DD1} = 1.70–1.95V; 1.80V TYP
 - V_{DD2H} = 1.01–1.12V; 1.05V TYP
 - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.90V TYP
 - V_{DDQ} = 0.50V or 0.45V¹ TYP; 0.30V TYP (ODT off only)
- **I/O characteristics**
 - Interface-LVSTL 0.5/0.3
 - I/O type: Low-swing single-ended, V_{SS} terminated
 - V_{OH}-compensated output drive
 - Programmable V_{SS} on-die termination (ODT)
 - Non target ODT support
 - DVFSQ support
- **Low power features**
 - DVFSC: Dynamic voltage frequency scaling core
 - Single-ended CK, single-ended WCK, and single-ended RDQS
 - Data copy
 - Write X

Options

- **Operating Voltage**
 - V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}/V_{DDQ} (ODT off only): 1.80V/1.05V/V_{DD2H} or 0.90V/0.50V or 0.45V¹/0.30V
- **Array Configuration**
 - 1Gb x 16 (1Gb16 x 1 Die x 1Ch x 1R)
 - 1Gb x 32 (1Gb16 x 1 Die x 2Ch x 1R)
 - 2Gb x 32 (1Gb16 x 1 Die x 2Ch x 2R)
 - 4Gb x 32 (2Gb8 x 2 Die x 2Ch x 2R)
 - 1Gb x 64 (1Gb16 x 1 Die x 4Ch x 1R)
 - 2Gb x 64 (1Gb16 x 1 Die x 4Ch x 2R)
- **Device configuration**
 - 1 die in package (1Gb16 x 1 die)
 - 2 die in package (1Gb16 x 2 die)
 - 4 die in package (1Gb16 x 4 die)
 - 8 die in package (2Gb8 x 8 die)
 - 8 die in package (1Gb16 x 8 die)
- **FBGA RoHS-compliant “green” package**
 - 315-ball TFBGA
 - 315-ball LFBGA
 - 441-ball TFBGA
 - 563-ball WFBGA
 - 563-ball VFBGA
- **Speed grade, cycle time (^tWCK)**
 - 8533 Mb/s
 - 7500 Mb/s
- **Operating Temperature:**
 - -25°C ≤ T_C ≤ +85°C
 - -40°C ≤ T_C ≤ +95°C
- **Revision**

Marking

F

1G16
1G32
2G32
4G32
1G64
2G64

D1
D2
D4
D8
D8
DS
DV
EK
AH
AJ

-023
-026

WT
IT
:B

Note: 1. V_{DDQ} = 0.45V (TYP) support on all packages up to 7500 Mb/s.

Part Number Ordering Information

Figure 1: Part Number Chart

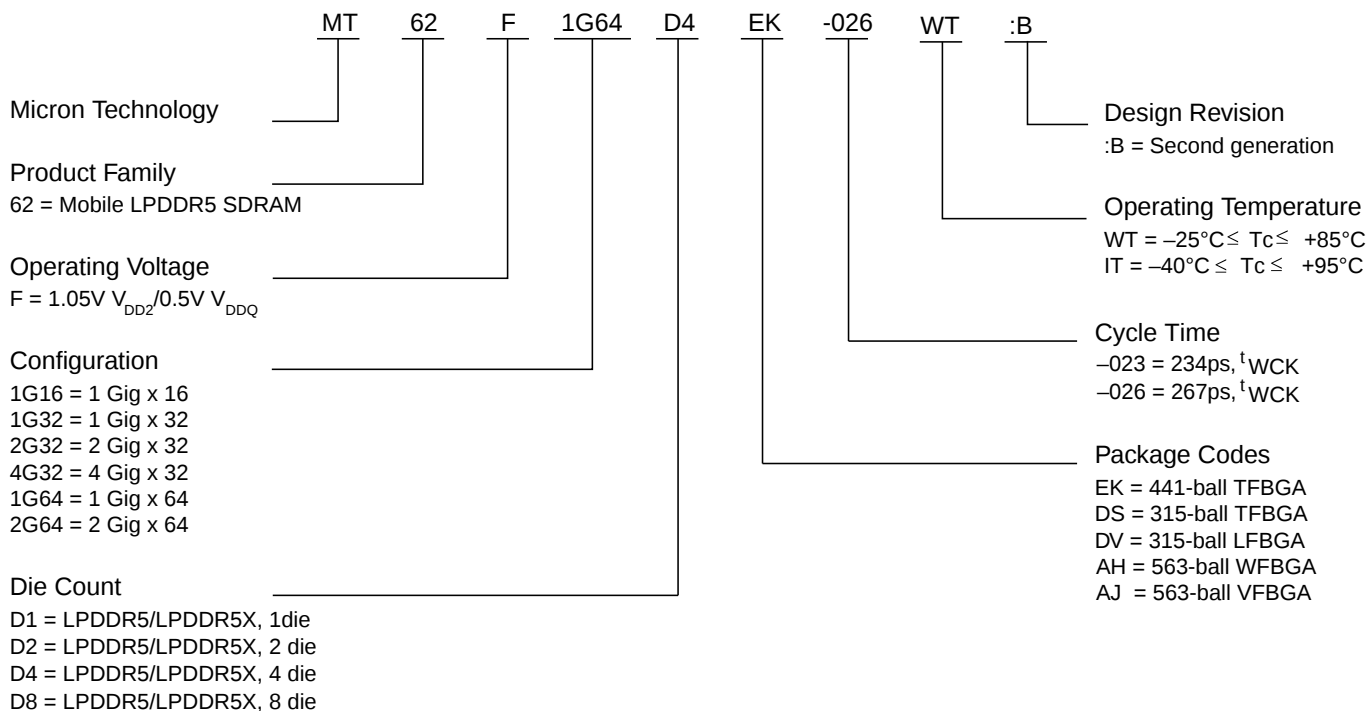


Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F1G16D1DS-023 IT:B	2GB (16Gb)	8533 Mb/s
MT62F1G32D2DS-023 IT:B	4GB (32Gb)	
MT62F1G32D2DS-023 WT:B		
MT62F2G32D4DS-023 IT:B	8GB (64Gb)	
MT62F2G32D4DS-023 WT:B		
MT62F4G32D8DV-023 IT:B	16GB (128Gb)	
MT62F4G32D8DV-023 WT:B		
MT62F1G64D4EK-023 WT:B	8GB (64Gb)	
MT62F2G64D8EK-023 WT:B	16GB (128Gb)	
MT62F1G64D4AH-023 WT:B	8GB (64Gb)	
MT62F2G64D8AJ-023 WT:B	16GB (128Gb)	

Table 1: Part Number List (Continued)

Part Number	Total Density	Data Rate per Pin
MT62F1G32D2DS-026 WT:B	4GB (32Gb)	7500 Mb/s
MT62F2G32D4DS-026 WT:B	8GB (64Gb)	
MT62F4G32D8DV-026 WT:B	16GB (128Gb)	
MT62F1G64D4EK-026 WT:B	8GB (64Gb)	
MT62F2G64D8EK-026 WT:B	16GB (128Gb)	
MT62F1G64D4AH-026 WT:B	8GB (64Gb)	
MT62F2G64D8AJ-026 WT:B	16GB (128Gb)	

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

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Important Notes and Warnings

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any content defined in this device ID specific data sheet document takes precedence over similar content defined in the general core LPDDR5/LPDDR5X SDRAM data sheet document(s).

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 2: Die Organization in the Package (x16)

Die Organization	1G16 (16 Gb/package)
Channel A	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Organization in the Package (x32)

Die Organization	1G32 (32 Gb/package)	2G32 (64 Gb/package)	4G32 (128 Gb/package)
Channel A	x16 mode × 1 die	–	–
Channel B	x16 mode × 1 die	–	–
Channel A, rank 0	–	x16 mode × 1 die	–
Channel B, rank 0	–	x16 mode × 1 die	–
Channel A, rank 1	–	x16 mode × 1 die	–
Channel B, rank 1	–	x16 mode × 1 die	–
Channel A, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[15:8]	–	–	x8 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 4: Die Organization in the Package (x64)

Die Organization	1G64 (64 Gb/package)	2G64 (128 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel C, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel D, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die
Channel C, rank 1	–	x16 mode × 1 die
Channel D, rank 1	–	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 5: Die Addressing

Description	1G16 (16 Gb/package), 1G32 (32 Gb/package), 2G32 (64 Gb/package), 1G64 (64 Gb/package), 2G64 (128 Gb/package)			4G32 (128 Gb/package)		
	BG mode	16B mode	8B mode	BG mode	16B mode	8B mode
Density per die	16Gb			16Gb		
Bits	17,179,869,184			17,179,869,184		
Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 16 DQ × 8 Banks	128Mb × 8 DQ × 4 Banks × 4BG	128Mb × 8 DQ × 16 Banks	256Mb × 8 DQ × 8 Banks
Number of banks	4	16	8	4	16	8
Number of bank groups	4	1	1	4	1	1
Array prefetch bits	256	256	512	128	128	256
Rows per bank	65,536			131,072		
Columns	64			64		
Page size (bytes)	2048	2048	4096	1024	1024	2048
Native burst length	16	16	32	16	16	32
Number of I/Os	16			8		
Bank address	BA[1:0]	BA[3:0]	BA[2:0]	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–	BG[1:0]	–	–
Row address	R[15:0]			R[16:0]		
Column address	C[5:0]			C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit			128-bit		

Note: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.

Refresh Requirement Parameters

Table 6: Refresh Requirement Parameters

Parameter	Symbol	16Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	^t RFCab	280	280	ns
REFRESH cycle time (per bank)	^t RFCpb	140	140	ns
Per bank refresh to per bank refresh time (different bank)	^t PBR2PBR	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^t PBR2ACT	7.5	10	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

CS Rx Relaxed Specification

Table 7: CS Rx Specifications

Item	Symbol	Min/ Max	CK Frequency (MHz)														Unit	Note
			67 ⁶	133	200	266	344	400	467	533	600	688	750	800	937.5	1066.5		
Rx mask																		
CS Rx mask height	vCSIVW	Min	155														mV	2, 7
CS Rx mask width at V _{REF} CS	^t CSIVW1	Min	0.3														UI	1
CS Rx mask width at vCSIVW	^t CSIVW2	Min	0.22														UI	1
Rx single pulse																		
CS Rx pulse amplitude	vCSIHL_AC	Min	240														mV	3
CS reference voltage	vREFCS		V _{DD2H} /3														mV	
CS Rx pulse width	^t CSIPW	Min	0.6														UI	
Power down																		
CS V _{IL} during power down/deep sleep	V _{ILPD}	Max	130														mV	4
CS V _{IH} during power down/deep sleep	V _{IHPD}	Min	550														mV	5
		Max	V _{DD2H} + 200															

- Notes: 1. CS Rx mask voltage and timing parameters at the pin include temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component min/max DC operating conditions.
2. CS single-pulse signal amplitude into the receiver must meet or exceed vCSIHL_AC at any point over the total UI; No timing requirement above a certain level. vCSIHL_AC is the peak-to-peak voltage centered around V_{REF} CS such that vCSIHL_AC/2 min has to be met both above and below V_{REF} CS.
3. vCSIHL_AC does not have to be met when no transitions are occurring.
4. The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.
5. V_{IHPD} is only applied for POWER DOWN and DEEP SLEEP EXIT operations.
6. The Rx voltage and absolute timing requirements apply for all CS operating frequencies at or below 67 for all speed bins. For example, ^tCSIVW1 (ns) = 4.477ns at or below 67 MHz CK frequency.
7. Measured at die pad.

DQ Rx Mask and Single Input Pulse Relaxed Specifications

Table 8: DQ Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/ Max	WCK Frequency (MHz)		Unit	Notes
			3750	4266		
DQ Rx mask height	vDIVW	Min	70		mV	1, 2, 3
DQ Rx mask width at V _{REF} (DQ)	^t DIVW1	Min	0.35		UI	1, 3
DQ Rx mask width at vDIVW	^t DIVW2	Min	0.18		UI	1, 3
DQ Rx pulse width at V _{REF} (DQ)	^t DIPW1	Min	0.51		UI	4
DQ Rx pulse reference	^t DIPW2	Min	0.26		UI	4
DQ Rx pulse width at V _{REF} (DQ) ± vDIVW/2	^t DIHL	Min	0.24		UI	4
DQ Rx pulse amplitude from programmed V _{REF} (DQ)	vDIHP1	Min	70		mV	
	vDILP1	Max	-70		mV	

Table 8: DQ Rx Mask and Single Input Pulse Specifications (Continued)

Item	Symbol	Min/ Max	WCK Frequency (MHz)		Unit	Notes
			3750	4266		
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55		mV	
	vDILP2	Max	-55		mV	

- Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (t_{DIVW1} , t_{DIVW2} , and vDIVW) are the same regardless DFE enabled or disabled. DFE coefficient can be included as part of input waveform amplitude when DFE is enabled.
4. $UI = t_{WCK}/2$, programmed V_{REF} , is defined as a percentage of MR14/15 code x V_{DDQ} .

Figure 2: DQ Rx Mask Definition

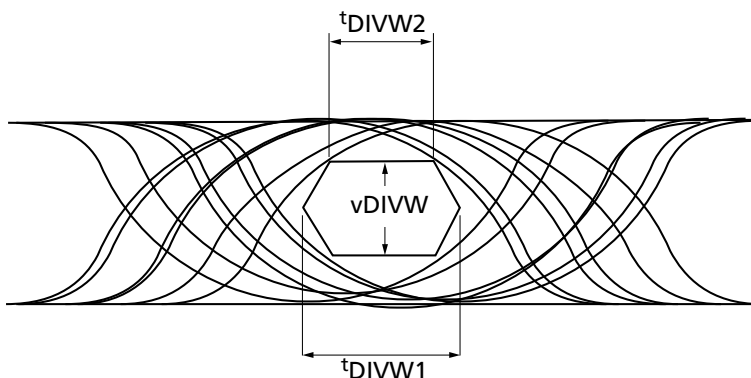
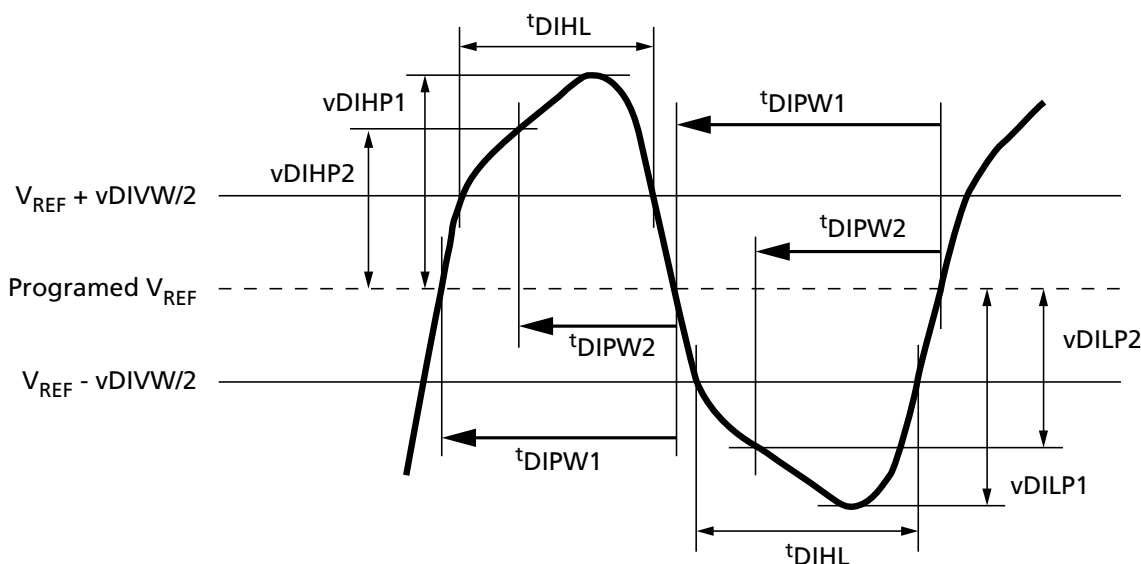


Figure 3: LPDDR5X DQ Single Pulse Definition



Note: 1. $vDIHL_AC/2 = vDIHP1 = vDILP1$. Programmed $V_{REF(DQ)}$ is defined as percentage of MR14/15 code * V_{DDQ} .

DQ Rx Mask and Single Input Pulse Relaxed Specifications 3200 MHz

Table 9: DQ, DMI, Parity and DBI Rx Mask and Single Input Pulse Specifications

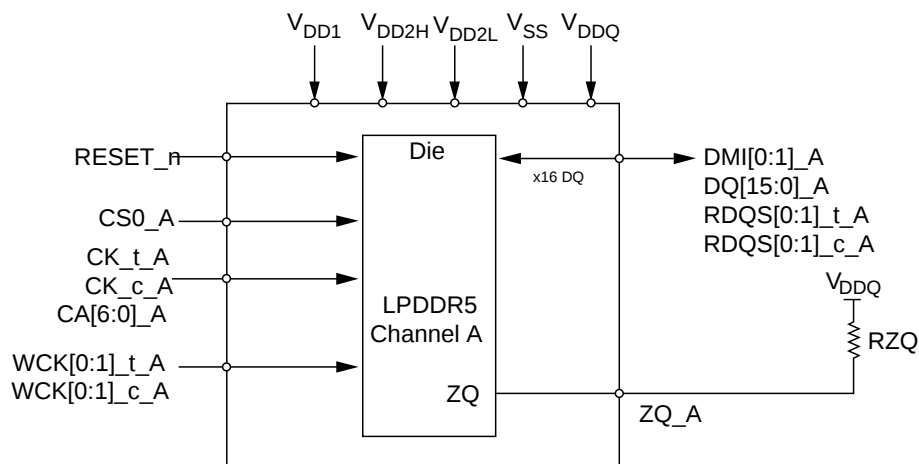
Item	Symbol	Min/Max	WCK Frequency (MHz)	Unit	Notes
			3200		
DQ Rx mask height	vDIVW	Min	70	mV	1, 2, 3, 6
DQ Rx mask width at $V_{REF(DQ)}$	t^{DIVW1}	Min	0.35	UI	1, 3
DQ Rx mask width at vDIVW	t^{DIVW2}	Min	0.18	UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	t^{DIPW1}	Min	0.51	UI	4, 6
DQ Rx pulse reference	t^{DIPW2}	Min	0.26	UI	4
DQ Rx pulse width at $V_{REF(DQ)} \pm vDIVW/2$	t^{DIHL}	Min	0.24	UI	4, 6
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70	mV	
	vDILP1	Max	-70	mV	
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55	mV	
	vDILP2	Max	-55	mV	
DQ V_{REF}	VREF(DQ)	Min	75	mV	6
		Max	180	mV	6
DQ to DQ offset	t^{DQ2DQ}	Max	30	ps	5

- Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (t^{DIVW1} , t^{DIVW2} , and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = $t^{WCK}/2$, programed V_{REF} , is defined as a percentage of MR14/15 code x V_{DDQ} .
5. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
6. When vDIVW is 70mV or more and less than 80mV.

Package Block Diagrams

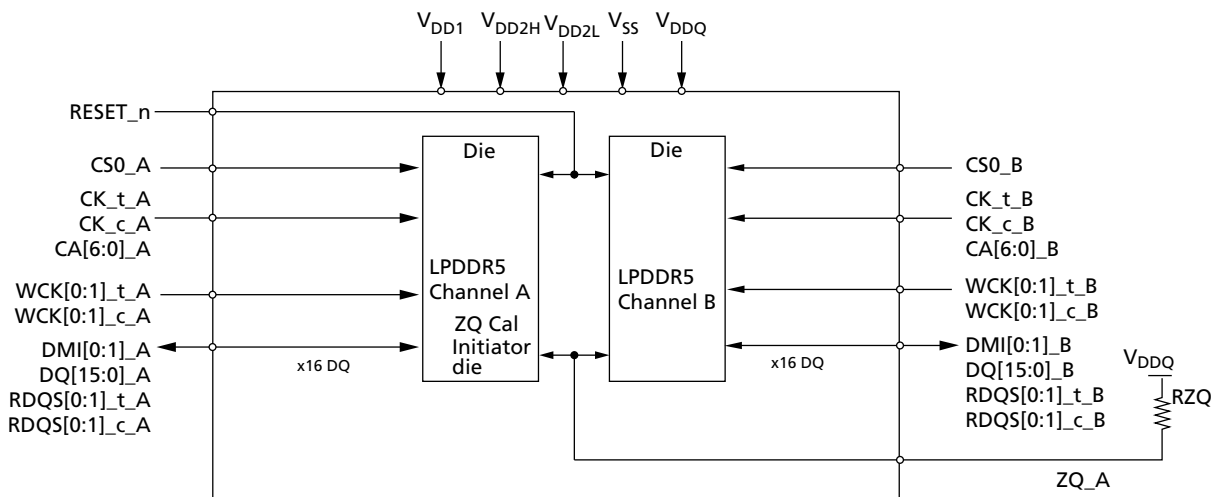
Single Die, Single Channel, Single Rank

Figure 4: Single-Die, Single-Channel, Single-Rank Package Block Diagram



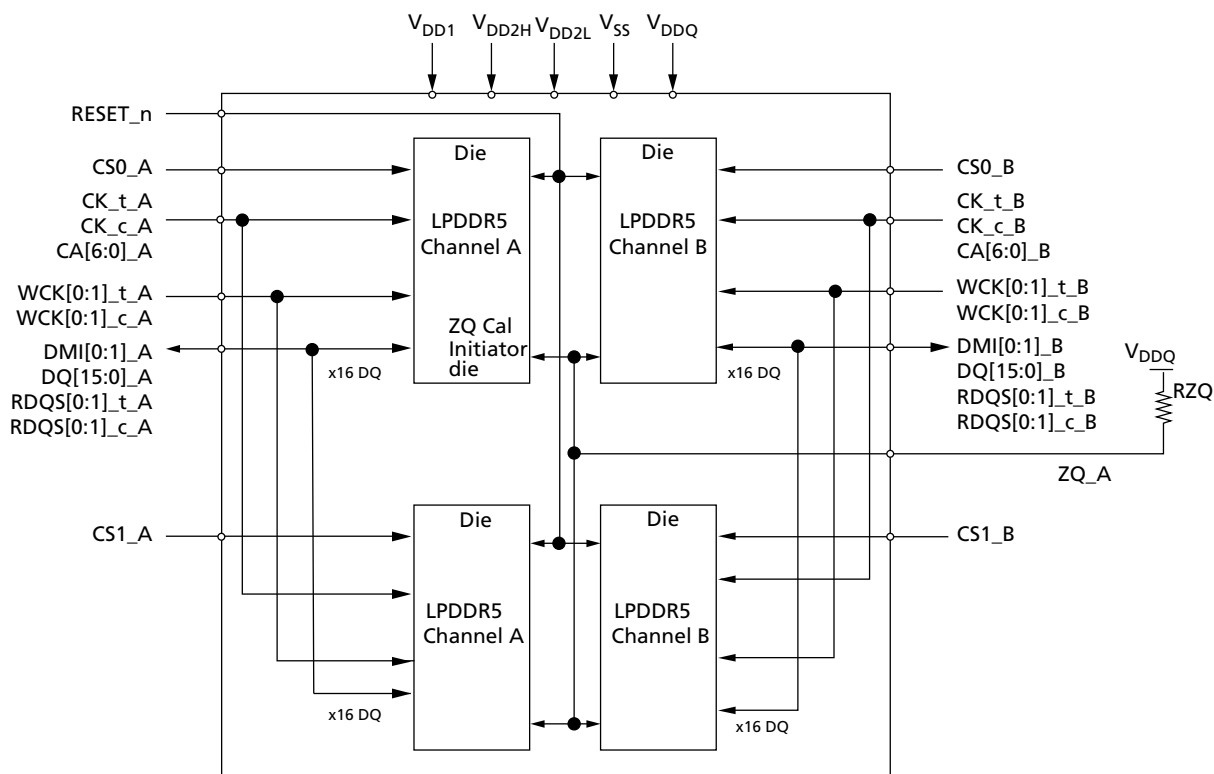
Dual Die, Dual Channel, Single Rank

Figure 5: Dual-Die, Dual-Channel, Single-Rank Package Block Diagram



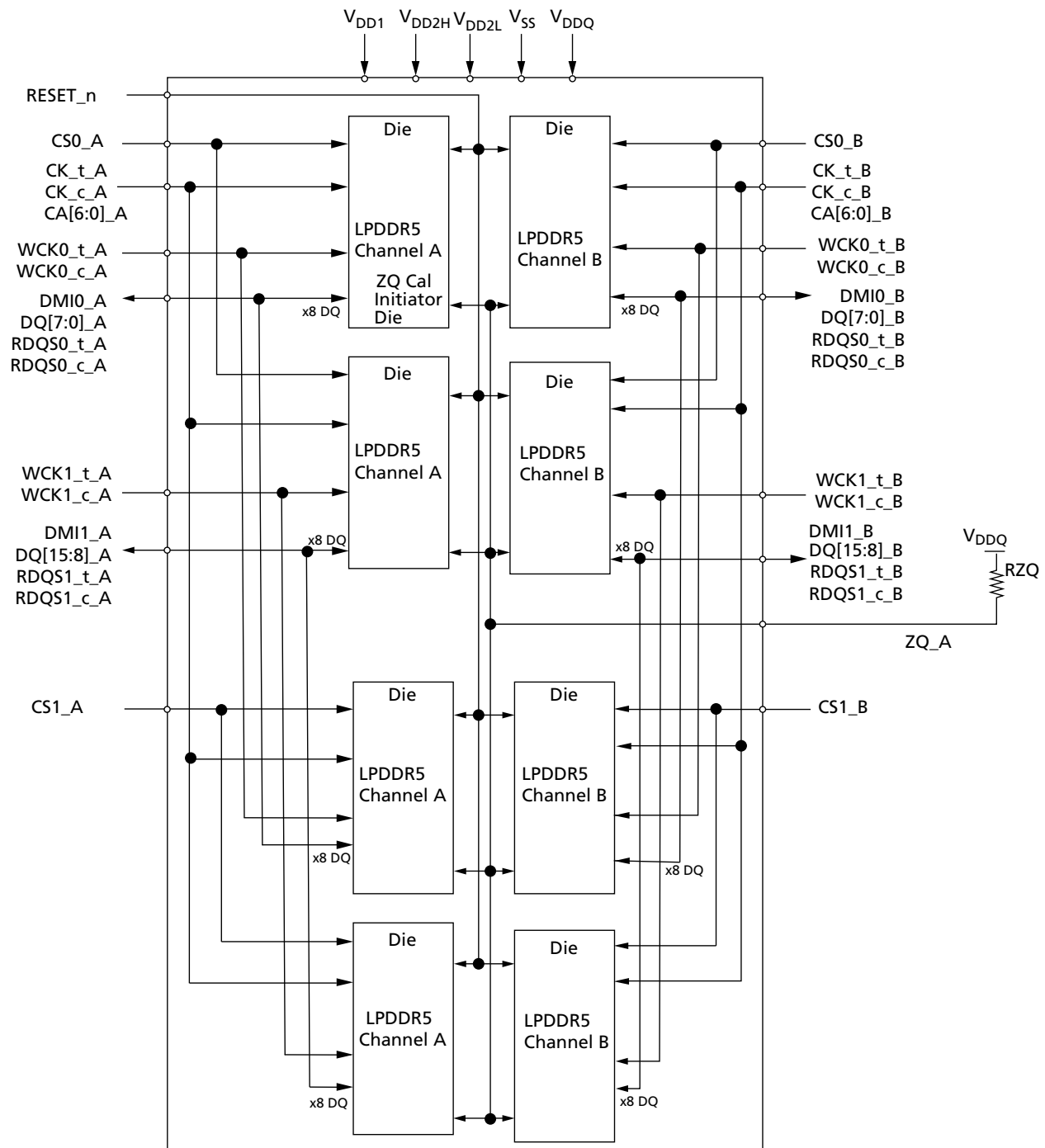
Quad Die, Dual Channel, Dual Rank

Figure 6: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram



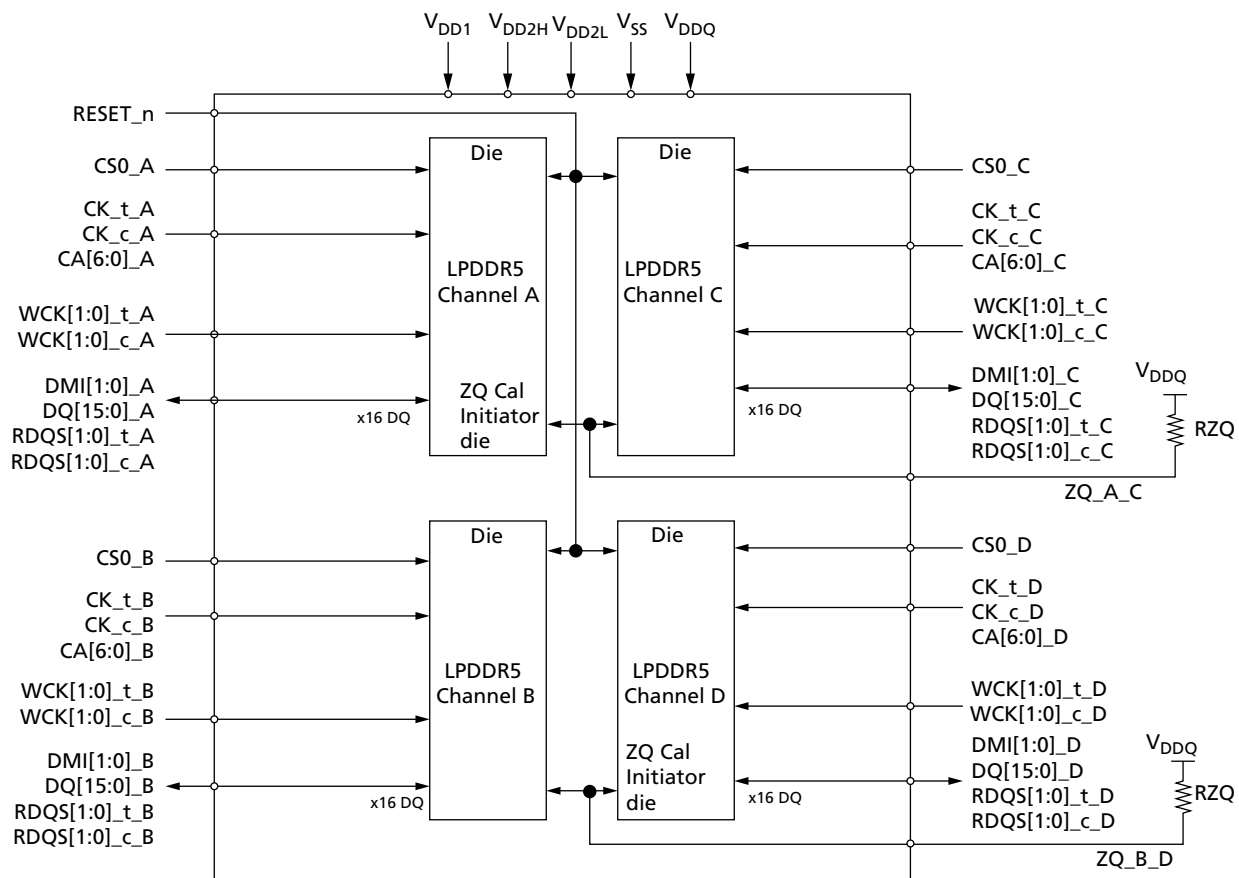
Eight Die, Dual Channel, Dual Rank

Figure 7: Eight-Die, Dual-Channel, Dual-Rank Package Block Diagram



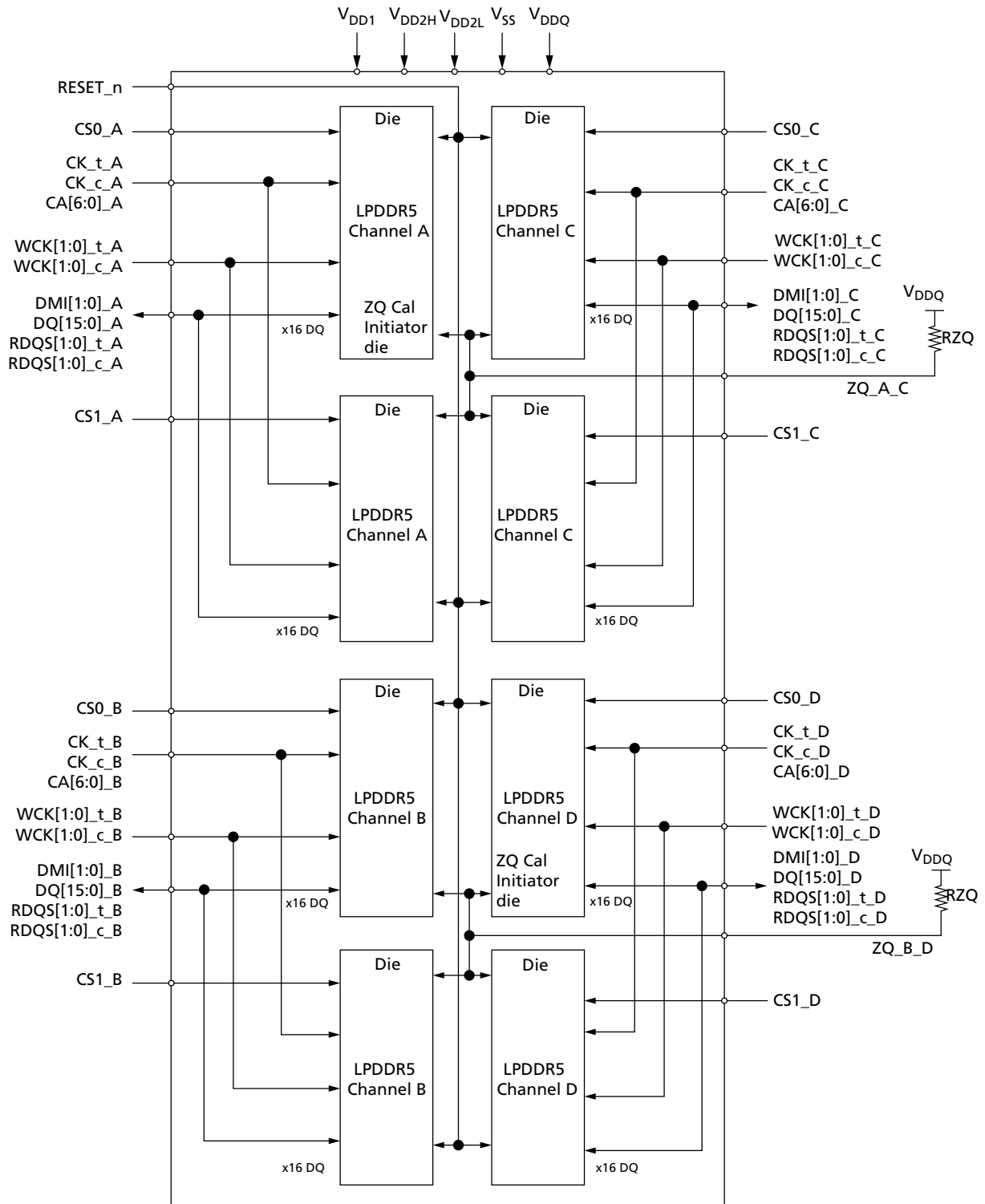
Quad-Die, Quad-Channel, Single-Rank

Figure 8: Quad-Die, Quad-Channel, Single-Rank Package Block Diagram



Eight-Die, Quad-Channel, Dual-Rank

Figure 9: Eight-Die, Quad-Channel, Dual-Rank Package Block Diagram



Ball Assignments and Descriptions

315b Single Die, Single Channel, 1 Rank, 2 Rank

Table 10: Single Channel 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A], CK_c_[A]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A], CS1_[A]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A], WCK[1:0]_c_[A]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A], RDQS[1:0]_c_[A]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.
RFU	–	Reserved Future Use: Not internally connected

Figure 10: 315-Ball Single-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V _{DDQ}	DMI0_A	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI1_A	V _{DDQ}	NC	NC	A
B	NC	V _{DDQ}	RDQS0_t_A	V _{SS}	DQ4_A	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ12_A	V _{SS}	RDQS1_t_A	V _{DDQ}	NC	B
C	V _{DD1}	DQ1_A	V _{DDQ}	RDQS0_c_A	V _{SS}	DQ5_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ13_A	V _{SS}	RDQS1_c_A	V _{DDQ}	DQ9_A	V _{DD1}	C
D	DQ0_A	V _{SS}	DQ3_A	V _{DDQ}	WCK0_c_A	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK1_c_A	V _{DDQ}	DQ11_A	V _{SS}	DQ8_A	D
E	V _{SS}	DQ2_A	V _{SS}	WCK0_t_A	V _{DDQ}	DQ6_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ14_A	V _{DDQ}	WCK1_t_A	V _{SS}	DQ10_A	V _{SS}	E
F	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ7_A	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ15_A	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	F
G	V _{DDQ}	V _{DDQ}	V _{SS}	CA0_A	V _{SS}	CS1_A	V _{SS}	CA2_A	V _{SS}	CA4_A	V _{SS}	CA6_A	V _{SS}	V _{DDQ}	V _{DDQ}	G
H	RESET_N	V _{DD2L}	V _{SS}	V _{SS}	CA1_A	V _{SS}	CS0_A	V _{SS}	CK_t_A	V _{SS}	CA3_A	V _{SS}	CA5_A	V _{DD2L}	ZQ_A	H
J	V _{SS}	V _{DD2L}	V _{SS}	RFU	V _{DD2H}	RFU	V _{SS}	V _{SS}	CK_c_A	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	J
K	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	K
L	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	L
M	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	M
N	V _{SS}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	NC	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	N
P	RFU	V _{DD2L}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	V _{SS}	V _{DD2L}	RFU	P
R	V _{DDQ}	V _{DDQ}	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	V _{DDQ}	V _{DDQ}	R
T	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	NC	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	NC	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	T
U	V _{SS}	NC	V _{SS}	NC	V _{DDQ}	NC	V _{DD2H}	V _{SS}	V _{DD2H}	NC	V _{DDQ}	NC	V _{SS}	NC	V _{SS}	U
V	NC	V _{SS}	NC	V _{DDQ}	NC	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	NC	V _{DDQ}	NC	V _{SS}	NC	V
W	V _{DD1}	NC	V _{DDQ}	NC	V _{SS}	NC	V _{DD2H}	V _{SS}	V _{DD2H}	NC	V _{SS}	NC	V _{DDQ}	NC	V _{DD1}	W
Y	NC	V _{DDQ}	NC	V _{SS}	NC	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	NC	V _{SS}	NC	V _{DDQ}	NC	Y
AA	NC	NC	V _{DDQ}	NC	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	NC	V _{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Top View (ball down)

V_{SS}
V_{DD1}
V_{DD2H}
V_{DD2L}
V_{DDQ}
CK
RDQS
WCK
DQ, DMI
CA, CS, ZQ, RESET
NC, RFU

315b Dual Channel, 1 Rank, 2 Rank

Table 11: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.
RFU	–	Reserved Future Use: Not internally connected.

Figure 11: 315-Ball Dual-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V _{DDQ}	DMI0_A	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI1_A	V _{DDQ}	NC	NC	A
B	NC	V _{DDQ}	RDQS0_t_A	V _{SS}	DQ4_A	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ12_A	V _{SS}	RDQS1_t_A	V _{DDQ}	NC	B
C	V _{DD1}	DQ1_A	V _{DDQ}	RDQS0_c_A	V _{SS}	DQ5_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ13_A	V _{SS}	RDQS1_c_A	V _{DDQ}	DQ9_A	V _{DD1}	C
D	DQ0_A	V _{SS}	DQ3_A	V _{DDQ}	WCK0_c_A	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK1_c_A	V _{DDQ}	DQ11_A	V _{SS}	DQ8_A	D
E	V _{SS}	DQ2_A	V _{SS}	WCK0_t_A	V _{DDQ}	DQ6_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ14_A	V _{DDQ}	WCK1_t_A	V _{SS}	DQ10_A	V _{SS}	E
F	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ7_A	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ15_A	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	F
G	V _{DDQ}	V _{DDQ}	V _{SS}	CA0_A	V _{SS}	CS1_A	V _{SS}	CA2_A	V _{SS}	CA4_A	V _{SS}	CA6_A	V _{SS}	V _{DDQ}	V _{DDQ}	G
H	RESET_N	V _{DD2L}	V _{SS}	V _{SS}	CA1_A	V _{SS}	CS0_A	V _{SS}	CK_t_A	V _{SS}	CA3_A	V _{SS}	CA5_A	V _{DD2L}	ZQ_A	H
J	V _{SS}	V _{DD2L}	V _{SS}	RFU	V _{DD2H}	RFU	V _{SS}	V _{SS}	CK_c_A	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	J
K	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	K
L	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	L
M	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	M
N	V _{SS}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	CK_c_B	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	N
P	RFU	V _{DD2L}	CA5_B	V _{SS}	CA3_B	V _{SS}	CK_t_B	V _{SS}	CS0_B	V _{SS}	CA1_B	V _{SS}	V _{SS}	V _{DD2L}	RFU	P
R	V _{DDQ}	V _{DDQ}	V _{SS}	CA6_B	V _{SS}	CA4_B	V _{SS}	CA2_B	V _{SS}	CS1_B	V _{SS}	CA0_B	V _{SS}	V _{DDQ}	V _{DDQ}	R
T	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ15_B	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ7_B	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	T
U	V _{SS}	DQ10_B	V _{SS}	WCK1_t_B	V _{DDQ}	DQ14_B	V _{DD2H}	V _{SS}	V _{DD2H}	DQ6_B	V _{DDQ}	WCK0_t_B	V _{SS}	DQ2_B	V _{SS}	U
V	DQ8_B	V _{SS}	DQ11_B	V _{DDQ}	WCK1_c_B	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK0_c_B	V _{DDQ}	DQ3_B	V _{SS}	DQ0_B	V
W	V _{DD1}	DQ9_B	V _{DDQ}	RDQS1_c_B	V _{SS}	DQ13_B	V _{DD2H}	V _{SS}	V _{DD2H}	DQ5_B	V _{SS}	RDQS1_c_B	V _{DDQ}	DQ1_B	V _{DD1}	W
Y	NC	V _{DDQ}	RDQS1_t_B	V _{SS}	DQ12_B	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ4_B	V _{SS}	RDQS0_t_B	V _{DDQ}	NC	Y
AA	NC	NC	V _{DDQ}	DMI1_B	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI0_B	V _{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Top View (ball down)

V_{SS}
V_{DD1}
V_{DD2H}
V_{DD2L}
V_{DDQ}
CK
RDQS
WCK
DQ, DMI
CA, CS, ZQ, RESET
NC, RFU

441-Ball Quad-Channel, 1-Rank, 2-Rank

Table 12: 441-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D], CK_c_[A:D]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D], WCK[1:0]_c_[A:D]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A:D], RDQS[1:0]_c_[A:D]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.
RFU	–	Reserved Future Use: Not internally connected

Figure 12: 441-Ball Quad-Channel FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	V _{SS}	V _{SS}	V _{DD1}	V _{DD2L}	V _{SS}	V _{DD2H}	V _{DD1}	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD1}	V _{DD2L}	V _{SS}	V _{DD2H}	V _{DD1}	V _{SS}	V _{DD2L}	V _{SS}	V _{SS}	A
B	V _{SS}	DQ0_A	V _{SS}	DQ3_A	V _{DD2H}	V _{SS}	DQ11_A	DQ9_A	DQ8_A	V _{SS}	V _{DD2H}	DQ0_C	V _{SS}	DQ3_C	V _{DD2H}	V _{SS}	DQ11_C	DQ9_C	DQ8_C	RFU	V _{SS}	B
C	V _{DD2H}	V _{SS}	DQ2_A	V _{DDQ}	CA0_A	V _{DD2H}	V _{SS}	DQ10_A	V _{DDQ}	V _{DD2H}	V _{SS}	V _{SS}	DQ2_C	V _{DDQ}	CA0_C	V _{DD2H}	V _{SS}	DQ10_C	V _{DDQ}	V _{DD2H}	V _{DD2H}	C
D	V _{SS}	DQ1_A	WCK0_c_A	V _{SS}	CA1_A	CS0_A	V _{DDQ}	V _{SS}	WCK1_t_A	V _{DD2H}	V _{DDQ}	DQ1_C	WCK0_c_C	V _{SS}	CA1_C	CS0_C	V _{DDQ}	V _{SS}	WCK1_t_C	V _{DDQ}	V _{SS}	D
E	V _{DDQ}	RDQS0_c_A	V _{SS}	WCK0_t_A	V _{SS}	CS1_A	V _{SS}	WCK1_c_A	DMI1_A	V _{SS}	V _{DDQ}	RDQS0_c_C	V _{SS}	WCK0_t_C	V _{SS}	CS1_C	V _{SS}	WCK1_c_C	DMI1_C	V _{SS}	V _{DD2H}	E
F	V _{DDQ}	RDQS0_t_A	V _{SS}	V _{DDQ}	V _{SS}	CA2_A	V _{SS}	RDQS1_t_A	V _{SS}	V _{DDQ}	V _{SS}	RDQS0_t_C	V _{SS}	V _{DDQ}	V _{SS}	CA2_C	V _{SS}	RDQS1_t_C	V _{SS}	V _{DDQ}	V _{DD2H}	F
G	V _{SS}	DQ4_A	V _{DDQ}	DMI0_A	RFU	RFU	CA6_A	V _{SS}	RDQS1_c_A	V _{SS}	V _{DDQ}	DMI0_C	V _{DDQ}	DQ4_C	RFU	RFU	CA6_C	V _{SS}	RDQS1_c_C	V _{SS}	V _{SS}	G
H	V _{DD2L}	V _{SS}	DQ5_A	V _{SS}	CK_t_A	V _{SS}	CA5_A	V _{DDQ}	V _{SS}	DQ12_A	V _{SS}	V _{SS}	DQ5_C	V _{SS}	CK_t_C	V _{SS}	CA5_C	V _{DDQ}	V _{SS}	DQ12_C	V _{DD2L}	H
J	V _{DD2H}	DQ6_A	DQ7_A	V _{DD2H}	V _{SS}	CK_c_A	V _{SS}	DQ14_A	DQ13_A	V _{SS}	V _{DD2L}	DQ6_C	DQ7_C	V _{DD2L}	ZQ_A_C	CK_c_C	V _{SS}	DQ14_C	DQ13_C	V _{SS}	V _{DD2H}	J
K	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	CA3_A	CA4_A	V _{DD2L}	V _{SS}	DQ15_A	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	CA3_C	CA4_C	V _{DD2H}	V _{SS}	DQ15_C	V _{SS}	K
L	V _{DD2H}	V _{DD2L}	V _{DD2L}	V _{DD2H}	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	V _{DD2H}	V _{DD2L}	V _{DD2L}	V _{DD2H}	L
M	V _{SS}	DQ15_B	V _{SS}	V _{DD2H}	CA4_B	CA3_B	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	DQ15_D	V _{SS}	V _{DD2L}	CA4_D	CA3_D	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	M
N	V _{DD2H}	V _{SS}	DQ13_B	DQ14_B	V _{SS}	CK_c_B	ZQ_B_D	V _{DD2L}	DQ7_B	DQ6_B	V _{DD2L}	V _{SS}	DQ13_D	DQ14_D	V _{SS}	CK_c_D	V _{SS}	V _{DD2H}	DQ7_D	DQ6_D	V _{DD2H}	N
P	V _{DD2L}	DQ12_B	V _{SS}	V _{DDQ}	CA5_B	V _{SS}	CK_t_B	V _{SS}	DQ5_B	V _{SS}	V _{SS}	DQ12_D	V _{SS}	V _{DDQ}	CA5_D	V _{SS}	CK_t_D	V _{SS}	DQ5_D	V _{SS}	V _{DD2L}	P
R	V _{SS}	V _{SS}	RDQS1_c_B	V _{SS}	CA6_B	RFU	RFU	DQ4_B	V _{DDQ}	DMI0_B	V _{DDQ}	V _{SS}	RDQS1_c_D	V _{SS}	CA6_D	RFU	RFU	DMI0_D	V _{DDQ}	DQ4_D	V _{SS}	R
T	V _{DD2H}	V _{DDQ}	V _{SS}	RDQS1_t_B	V _{SS}	CA2_B	V _{SS}	V _{DDQ}	V _{SS}	RDQS0_t_B	V _{SS}	V _{DDQ}	V _{SS}	RDQS1_t_D	V _{SS}	CA2_D	V _{SS}	V _{DDQ}	V _{SS}	RDQS0_t_D	V _{DDQ}	T
U	V _{DD2H}	V _{SS}	DMI1_B	WCK1_c_B	V _{SS}	CS1_B	V _{SS}	WCK0_t_B	V _{SS}	RDQS0_c_B	V _{DDQ}	V _{SS}	DMI1_D	WCK1_c_D	V _{SS}	CS1_D	V _{SS}	WCK0_t_D	V _{SS}	RDQS0_c_D	V _{DDQ}	U
V	V _{SS}	V _{DDQ}	WCK1_t_B	V _{SS}	V _{DDQ}	CS0_B	CA1_B	V _{SS}	WCK0_c_B	DQ1_B	V _{DDQ}	V _{DD2H}	WCK1_t_D	V _{SS}	V _{DDQ}	CS0_D	CA1_D	V _{SS}	WCK0_c_D	DQ1_D	V _{SS}	V
W	V _{DD2H}	V _{DD2H}	V _{DDQ}	DQ10_B	V _{SS}	V _{DD2H}	CA0_B	V _{DDQ}	DQ2_B	V _{SS}	V _{SS}	V _{DD2H}	V _{DDQ}	DQ10_D	V _{SS}	V _{DD2H}	CA0_D	V _{DDQ}	DQ2_D	V _{SS}	V _{DD2H}	W
Y	V _{SS}	RESET_N	DQ8_B	DQ9_B	DQ11_B	V _{SS}	V _{DD2H}	DQ3_B	V _{SS}	DQ0_B	V _{DD2H}	V _{SS}	DQ8_D	DQ9_D	DQ11_D	V _{SS}	V _{DD2H}	DQ3_D	V _{SS}	DQ0_D	V _{SS}	Y
AA	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	V _{DD1}	V _{DD2H}	V _{SS}	V _{DD2L}	V _{DD1}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	V _{DD1}	V _{DD2H}	V _{SS}	V _{DD2L}	V _{DD1}	V _{SS}	V _{SS}	AA

Top View (ball down)

V _{SS}	V _{DD1}	V _{DD2H}	V _{DD2L}	V _{DDQ}	CK	RDQS	WCK	DQ, DMI	CA, CS, ZQ, RESET	NC
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563b Quad Channel, 1 Rank, 2 Rank

Table 13: 563-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D] WCK[1:0]_c_[A:D]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A:D] RDQS[1:0]_c_[A:D]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.

Figure 13: 563-Ball Quad-Channel FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A		NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	A
B	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	B
C	V _{SS}	V _{SS}	DQ0_A	V _{DDQ}	V _{SS}	DMI0_A	DQ5_A	V _{SS}	CS0_A	CS1_A	CA3_A	V _{SS}	DQ13_A	DMI1_A	V _{SS}	V _{DDQ}	DQ8_A	V _{SS}	V _{SS}	C
D	V _{SS}	V _{DD1}	V _{SS}	DQ3_A	WCK0_C_A	V _{DDQ}	V _{SS}	CA0_A	V _{SS}	V _{SS}	V _{SS}	CA6_A	V _{SS}	V _{DDQ}	WCK1_C_A	DQ11_A	V _{SS}	V _{DD1}	V _{SS}	D
E	V _{SS}	V _{DD2H}	DQ1_A	V _{SS}	WCK0_T_A	V _{SS}	DQ6_A	V _{DDQ}	CA1_A	CK_T_A	CA4_A	V _{DDQ}	DQ14_A	V _{SS}	WCK1_T_A	V _{SS}	DQ9_A	V _{DD2H}	V _{SS}	E
F	V _{SS}	V _{SS}	V _{DDQ}	RDQS0_T_A	V _{DD2H}	DQ4_A	V _{DDQ}	V _{SS}	V _{SS}	CK_C_A	V _{SS}	V _{SS}	V _{DDQ}	DQ12_A	V _{DD2H}	RDQS1_T_A	V _{DDQ}	V _{SS}	V _{SS}	F
G	V _{SS}	V _{DD2L}	DQ2_A	RDQS0_C_A	V _{SS}	V _{DD2H}	DQ7_A	V _{DD2H}	CA2_A	V _{DD2L}	CA5_A	V _{DD2H}	DQ15_A	V _{DD2H}	V _{SS}	RDQS1_C_A	DQ10_A	ZQ_A_C	V _{SS}	G
H	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2L}	H
J	V _{SS}	V _{DD2L}	DQ2_C	RDQS0_C_C	V _{SS}	V _{DD2H}	DQ7_C	V _{DD2H}	CA2_C	V _{DD2L}	CA5_C	V _{DD2H}	DQ15_C	V _{DD2H}	V _{SS}	RDQS1_C_C	DQ10_C	RESET_N	V _{SS}	J
K	V _{SS}	V _{SS}	V _{DDQ}	RDQS0_T_C	V _{DD2H}	DQ4_C	V _{DDQ}	V _{SS}	V _{SS}	CK_C_C	V _{SS}	V _{SS}	V _{DDQ}	DQ12_C	V _{DD2H}	RDQS1_T_C	V _{DDQ}	V _{SS}	V _{SS}	K
L	V _{SS}	V _{DD2H}	DQ1_C	V _{SS}	WCK0_T_C	V _{SS}	DQ6_C	V _{DDQ}	CA1_C	CK_T_C	CA4_C	V _{DDQ}	DQ14_C	V _{SS}	WCK1_T_C	V _{SS}	DQ9_C	V _{DD2H}	V _{SS}	L
M	V _{SS}	V _{SS}	V _{SS}	DQ3_C	WCK0_C_C	V _{DDQ}	V _{SS}	CA0_C	V _{SS}	V _{SS}	V _{SS}	CA6_C	V _{SS}	V _{DDQ}	WCK1_C_C	DQ11_C	V _{SS}	V _{SS}	V _{SS}	M
N	V _{SS}	V _{DD1}	DQ0_C	V _{DDQ}	V _{SS}	DMI0_C	DQ5_C	V _{SS}	CS0_C	CS1_C	CA3_C	V _{SS}	DQ13_C	DMI1_C	V _{SS}	V _{DDQ}	DQ8_C	V _{DD1}	V _{SS}	N
P	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	P
R	V _{SS}	V _{SS}					V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	R
T	V _{SS}	V _{SS}					V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	T
U	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	U
V	V _{SS}	V _{DD1}	DQ8_D	V _{DDQ}	V _{SS}	DMI1_D	DQ13_D	V _{SS}	CA3_D	CS1_D	CS0_D	V _{SS}	DQ5_D	DMI0_D	V _{SS}	V _{DDQ}	DQ0_D	V _{DD1}	V _{SS}	V
W	V _{SS}	V _{SS}	V _{SS}	DQ11_D	WCK1_C_D	V _{DDQ}	V _{SS}	CA6_D	V _{SS}	V _{SS}	V _{SS}	CA0_D	V _{SS}	V _{DDQ}	WCK0_C_D	DQ3_D	V _{SS}	V _{SS}	V _{SS}	W
Y	V _{SS}	V _{DD2H}	DQ9_D	V _{SS}	WCK1_T_D	V _{SS}	DQ14_D	V _{DDQ}	CA4_D	CK_T_D	CA1_D	V _{DDQ}	DQ6_D	V _{SS}	WCK0_T_D	V _{SS}	DQ1_D	V _{DD2H}	V _{SS}	Y
AA	V _{SS}	V _{SS}	V _{DDQ}	RDQS1_T_D	V _{DD2H}	DQ12_D	V _{DDQ}	V _{SS}	V _{SS}	CK_C_D	V _{SS}	V _{SS}	V _{DDQ}	DQ4_D	V _{DD2H}	RDQS0_T_D	V _{DDQ}	V _{SS}	V _{SS}	AA
AB	V _{SS}	V _{DD2L}	DQ10_D	RDQS1_C_D	V _{SS}	V _{DD2H}	DQ15_D	V _{DD2H}	CA5_D	V _{DD2L}	CA2_D	V _{DD2H}	DQ7_D	V _{DD2H}	V _{SS}	RDQS0_C_D	DQ2_D	V _{SS}	V _{SS}	AB
AC	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	AC
AD	V _{SS}	V _{DD2L}	DQ10_B	RDQS1_C_B	V _{SS}	V _{DD2H}	DQ15_B	V _{DD2H}	CA5_B	V _{DD2L}	CA2_B	V _{DD2H}	DQ7_B	V _{DD2H}	V _{SS}	RDQS0_C_B	DQ2_B	ZQ_B_D	V _{SS}	AD
AE	V _{SS}	V _{SS}	V _{DDQ}	RDQS1_T_B	V _{DD2H}	DQ12_B	V _{DDQ}	V _{SS}	V _{SS}	CK_C_B	V _{SS}	V _{SS}	V _{DDQ}	DQ4_B	V _{DD2H}	RDQS0_T_B	V _{DDQ}	V _{SS}	V _{SS}	AE
AF	V _{SS}	V _{DD2H}	DQ9_B	V _{SS}	WCK1_T_B	V _{SS}	DQ14_B	V _{DDQ}	CA4_B	CK_T_B	CA1_B	V _{DDQ}	DQ6_B	V _{SS}	WCK0_T_B	V _{SS}	DQ1_B	V _{DD2H}	V _{SS}	AF
AG	V _{SS}	V _{DD1}	V _{SS}	DQ11_B	WCK1_C_B	V _{DDQ}	V _{SS}	CA6_B	V _{SS}	V _{SS}	V _{SS}	CA0_B	V _{SS}	V _{DDQ}	WCK0_C_B	DQ3_B	V _{SS}	V _{DD1}	V _{SS}	AG
AH	V _{SS}	V _{SS}	DQ8_B	V _{DDQ}	V _{SS}	DMI1_B	DQ13_B	V _{SS}	CA3_B	CS1_B	CS0_B	V _{SS}	DQ5_B	DMI0_B	V _{SS}	V _{DDQ}	DQ0_B	V _{SS}	V _{SS}	AH
AJ	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	AJ
AK	NC	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	AK

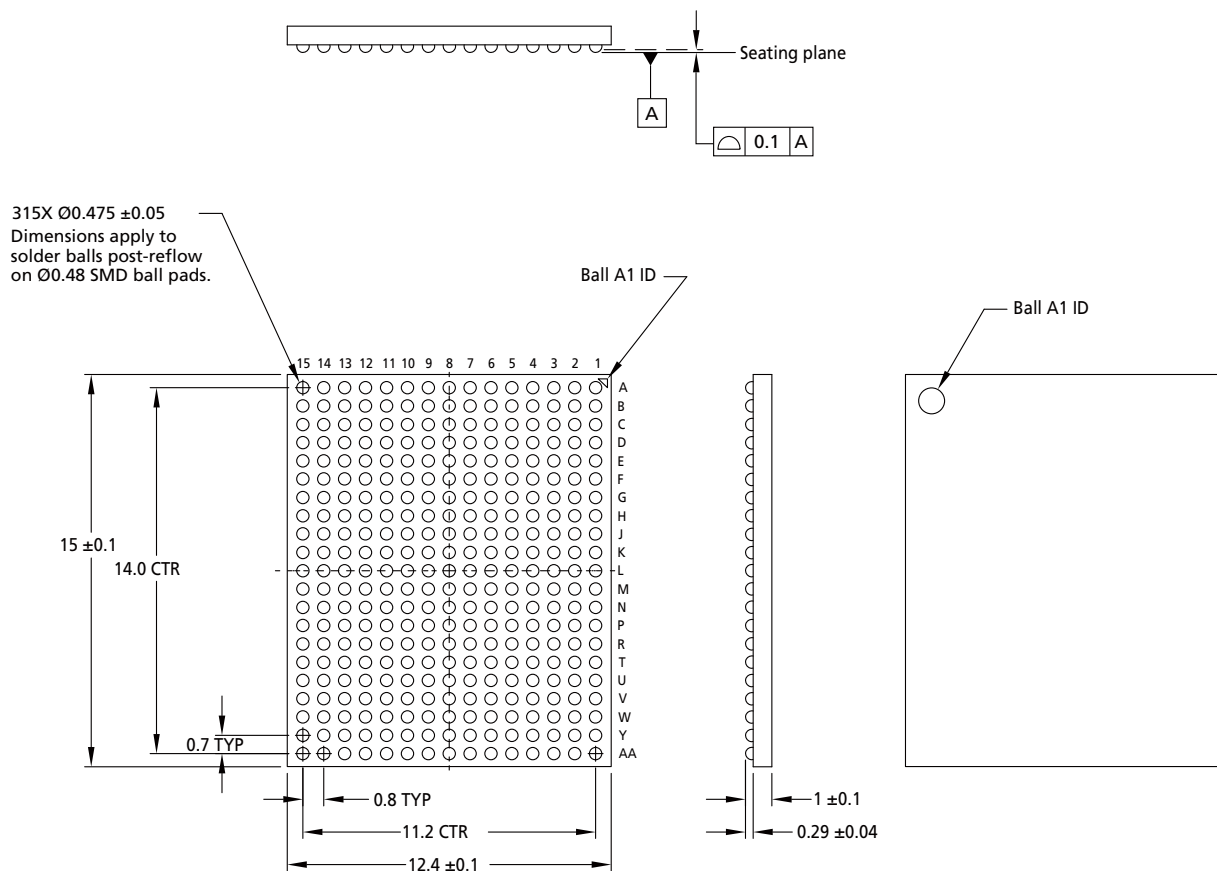
Top View (ball down)

V_{SS}
V_{DD1}
V_{DD2H}
V_{DD2HQ}
V_{DD2L}
V_{DDQ}
CK
DQS, RDQS
DQ, DMI
WCK
CA, CS, ZQ, RESET
NC, RFU, DNU

Package Dimensions

315-Ball Package (Package Code: DS)

Figure 14: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)

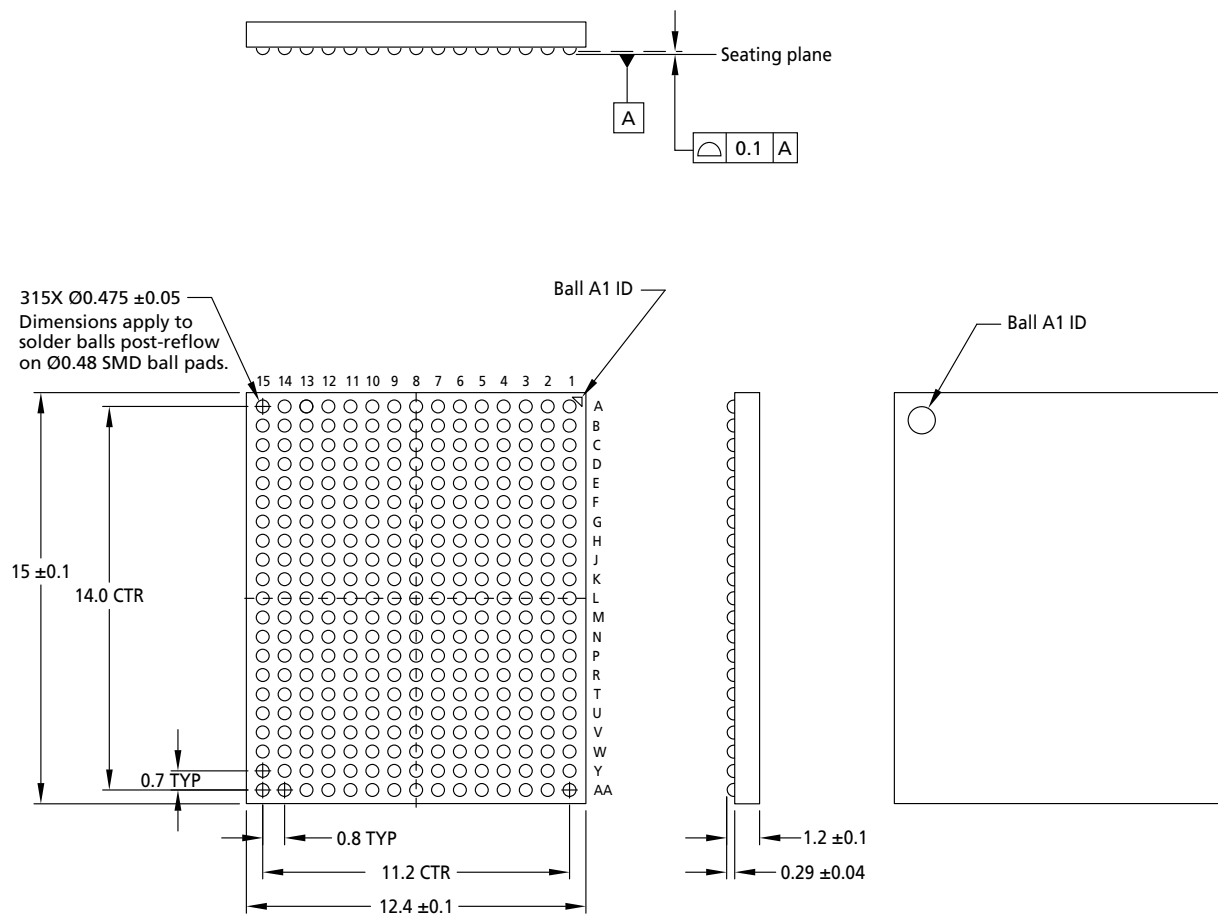


Notes: 1. All dimensions are in millimeters.

2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

315-Ball Package (Package Code: DV)

Figure 15: 315-Ball LFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.3mm (MAX) (Package Code: DV)

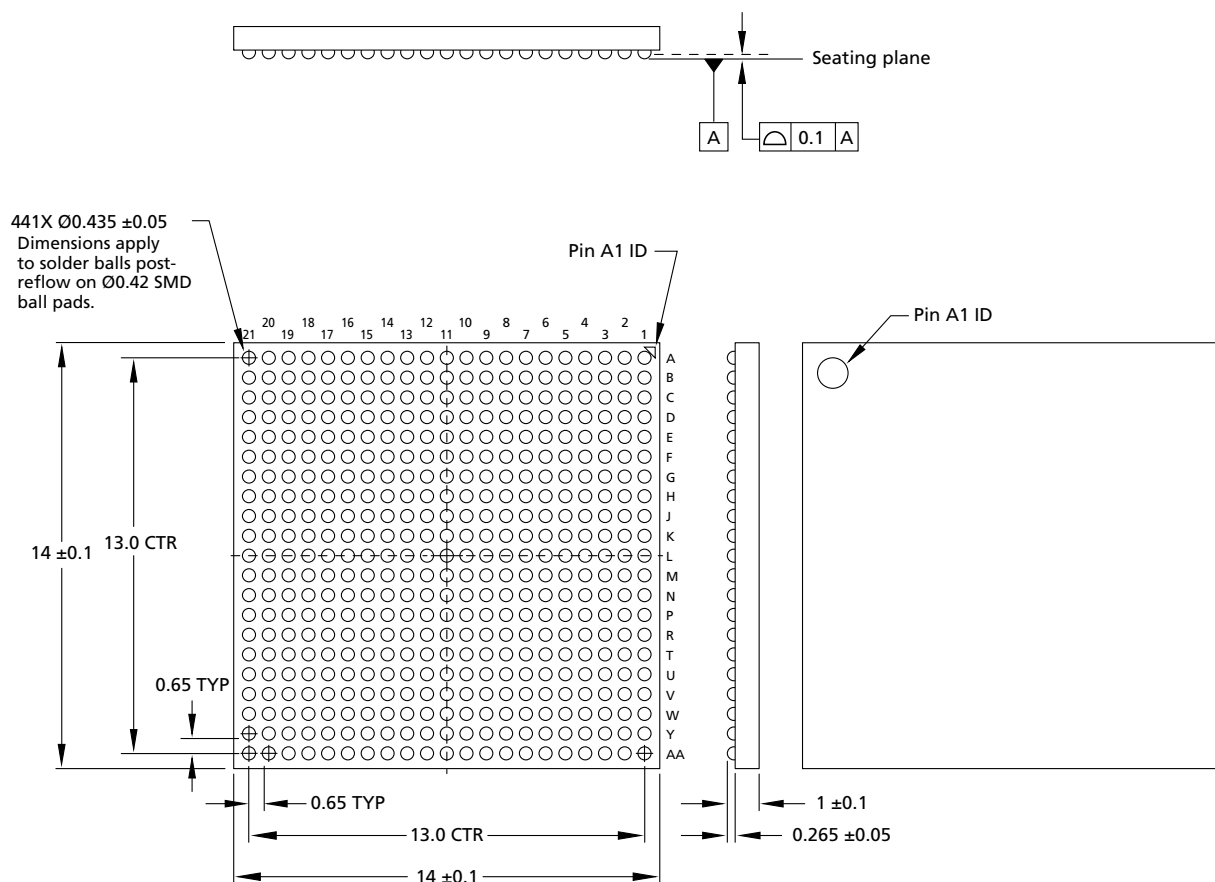


Notes: 1. All dimensions are in millimeters.

2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

441-Ball Package (Package Code: EK)

Figure 16: 441-Ball TFBGA – 14.0mm (TYP) x 14.0mm (TYP) x 1.1mm (MAX) (Package Code: EK)

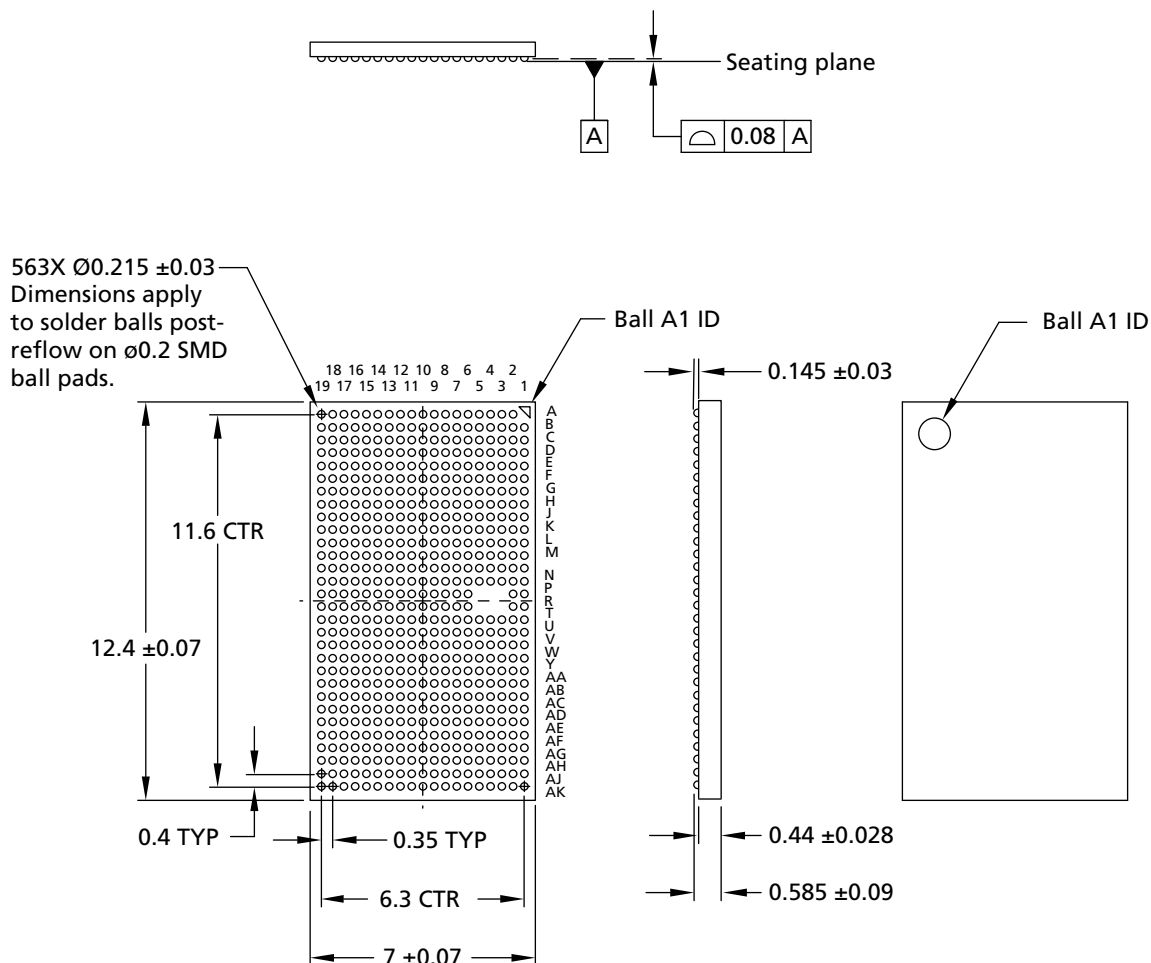


Notes: 1. All dimensions are in millimeters.

2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni).

563-Ball Package (Package Code: AH)

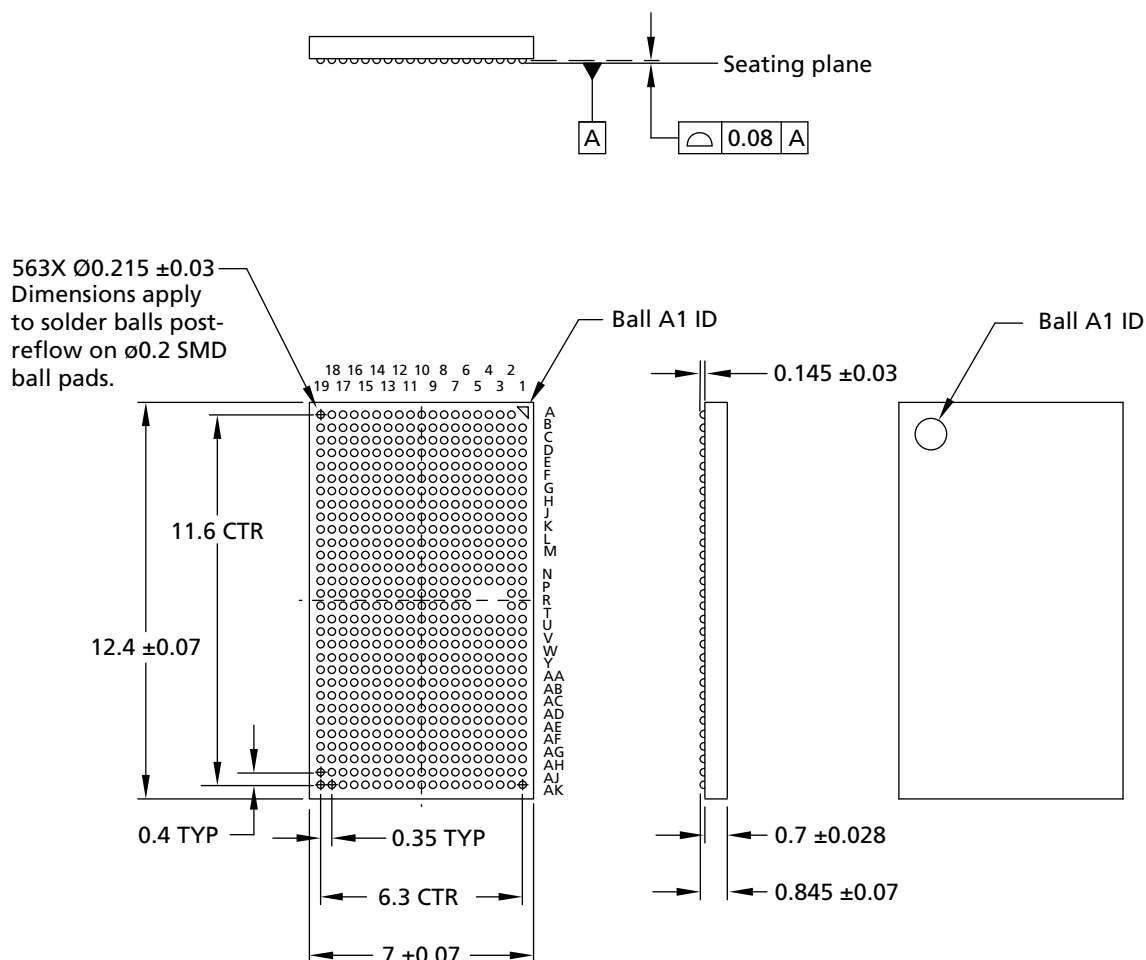
Figure 17: 563-Ball WFBGA – 7.0mm (TYP) x 12.4mm (TYP) x 0.675mm (MAX) (Package Code: AH)



- Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC302 with Ni/Au pads (Sn-3Ag-0.2Cu).

563-Ball Package (Package Code: AJ)

Figure 18: 563-Ball VFBGA – 7.0mm (TYP) x 12.4mm (TYP) x 0.915mm (MAX) (Package Code: AJ)



Notes: 1. All dimensions are in millimeters.

2. Solder ball composition: SAC302 with Ni/Au pads (Sn-3Ag-0.2Cu).

Package Thermal Impedance

Table 14: Package Thermal Impedance Characteristics

Die Revision	Package	Parameter	Symbol	Value	Unit
Rev B	315-ball, SDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	3.5	°C/W
		Junction-to-board	Θ_{JB}	11.6	°C/W
	315-ball, DDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	3.4	°C/W
		Junction-to-board	Θ_{JB}	11.1	°C/W
	315-ball, QDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	2.7	°C/W
		Junction-to-board	Θ_{JB}	11.7	°C/W
	315-ball, 8DP, package code DV	Junction-to-case (TOP)	Θ_{JC}	2.3	°C/W
		Junction-to-board	Θ_{JB}	12.4	°C/W
	441-ball, QDP, package code EK	Junction-to-case (TOP)	Θ_{JC}	2.1	°C/W
		Junction-to-board	Θ_{JB}	7.8	°C/W
	441-ball, 8DP, package code EK	Junction-to-case (TOP)	Θ_{JC}	1.6	°C/W
		Junction-to-board	Θ_{JB}	7.5	°C/W
	563-ball, QDP, package code AH	Junction-to-case (TOP)	Θ_{JC}	3.3	°C/W
		Junction-to-board	Θ_{JB}	9.1	°C/W
	563-ball, 8DP, package code AJ	Junction-to-case (TOP)	Θ_{JC}	4.1	°C/W
		Junction-to-board	Θ_{JB}	10.1	°C/W

Product-Specific Mode Register Definition

Table 15: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	Per-pin DFE	Pre Emphasis	Unified NT ODT behavior mode	DMI output behavior mode	Optimized refresh mode	Enhanced WCK always-on mode	Latency mode	NT ODT timing mode
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 1G16, 1G32, 2G32, 1G64, 2G64 OP[1] = 1b: Device supports x8 mode latency for 4G32							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 0b: Device does not support Per Pin DFE							
MR1						DRFM support ³	ARFM support ³	CS ODT OP support
	OP[0] = 1b: Device supports CS ODT behavior OP							
	OP[1] = 1b: Device supports ARFM							
	OP[2] = 0b: Device does not supports DRFM							
MR3				BK/BG Org				
	OP[4:3] = 00b: BG, 01b: 8B, 10b: 16B Mode Supported							
MR4				Refresh Multiplier (Note 6)				
	OP[4:0]: Refer to General LPDDR5/LPDDR5X Specification 1 for mode register definitions.							
MR5	Manufacturer ID							
	1111 1111b: Micron							
MR6	Revision ID1							
	0000 0111b							
MR8	I/O width		Density				Type	
	OP[7:6] = 00b: x16 for 1G16, 1G32, 2G32, 1G64, 2G64 OP[7:6] = 01b: x8 for 4G32		OP[5:2] = 0110b: 16Gb				OP[1:0] = 01b: LPDDR5X SDRAM	
MR13						VRO		
	OP[2] = 0b: Normal operation (default) 1b: Output the V _{REF(CA)} value on DQ7 and V _{REF(DQ)} value on DQ6							
MR19			WCK2DQ OSC FM					
	OP[5] = 1b: WCK2DQ OSC FM supported							

Table 15: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR21	WXS				ODTD-CSFS	WXFS	RDCFS	WDCFS
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	RECC		WECC					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	DFES				Read DCA			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE (See Note 5)							
MR26		RDQSTFS						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	RAAMULT		RAAIMT					RFM
	OP[0] = 1b: RFM is required							
	OP[5:1] = 01110b: 112							
	OP[7:6] = 01b: 4X							
MR41					E-DVFSC ODT OP support	DVFSC/E-DVFSC Support		
	OP[2:1] = 00b: Only Legacy DVFSC Mode supported							
	OP[3] = 0b: Enhanced DVFSC ODT OP not supported							
MR43		SBEC rule						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	ARFM ³				RFMSB		RAADEC	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: 1 = Does not support single-bank mode							
	OP[7:6] = 00b: default (01110b: 112), 01b: Level A = 01101b: 104, Level B = 01100b: 96, Level C = 01011: 88							
MR63 - MR164	Reserved MR bits MR63 through MR164 are RFU by JEDEC standard and should not be accessed by user unless directed by supplier.							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.

2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.

3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.

4. Write link ECC and read link ECC are supported.

5. Device supports 3-step DFE.

6. MR4:OP[4:0] output from each die in a defined package shall be used to determine the required package level refresh rate. Any other method used to determine a valid refresh rate, places ownership and responsibility of the correct refresh rate on the system developer or end user. T_{OPER} (case surface temperature) shall be used to determine whether operating temperature requirements are being met. Any other method used to determine



operating temperature, places ownership and responsibility of the correct operating temperature on the system developer or end user.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 16: WT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I _{DD01}	V _{DD1}	3.20	3.20	3.20	3.20	mA	
I _{DD02H}	V _{DD2H}	28.50	28.50	29.00	29.00		
I _{DD02L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD0Q}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2P1}	V _{DD1}	1.50	1.50	1.50	1.50	mA	
I _{DD2P2H}	V _{DD2H}	2.50	2.50	2.50	2.50		
I _{DD2P2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2PQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2PS1}	V _{DD1}	1.50	1.50	1.50	1.50	mA	
I _{DD2PS2H}	V _{DD2H}	2.50	2.50	2.50	2.50		
I _{DD2PS2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2PSQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2N1}	V _{DD1}	1.50	1.50	1.50	1.50	mA	
I _{DD2N2H}	V _{DD2H}	16.50	16.50	17.00	17.00		
I _{DD2N2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2NQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2NS1}	V _{DD1}	1.50	1.50	1.50	1.50	mA	
I _{DD2NS2H}	V _{DD2H}	16.50	16.50	17.00	17.00		
I _{DD2NS2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2NSQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD3P1}	V _{DD1}	1.50	1.50	1.50	1.50	mA	
I _{DD3P2H}	V _{DD2H}	6.50	6.50	6.50	6.50		
I _{DD3P2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD3PQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD3PS1}	V _{DD1}	1.50	1.50	1.50	1.50	mA	
I _{DD3PS2H}	V _{DD2H}	6.50	6.50	6.50	6.50		
I _{DD3PS2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD3PSQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD3N1}	V _{DD1}	1.80	1.80	1.80	1.80	mA	
I _{DD3N2H}	V _{DD2H}	20.50	20.50	21.00	21.00		
I _{DD3N2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD3NQ}	V _{DDQ}	0.60	0.60	0.60	0.60		

Table 16: WT I_{DD} Parameters – Single Die (Continued)

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I _{DD4R1}	V _{DD1}	9.00	9.00	11.00	12.00	mA	3, 4
I _{DD4R2H}	V _{DD2H}	295.00	325.00	435.00	485.00		
I _{DD4R2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD4RQ}	V _{DDQ}	58.00	63.00	116.00	126.00		
I _{DD4W1}	V _{DD1}	8.00	9.00	10.00	11.00	mA	3
I _{DD4W2H}	V _{DD2H}	225.00	245.00	305.00	335.00		
I _{DD4W2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD4WQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD51}	V _{DD1}	23.00	23.00	23.00	23.00	mA	
I _{DD52H}	V _{DD2H}	165.00	165.00	165.00	165.00		
I _{DD52L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD5Q}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD5AB1}	V _{DD1}	3.20	3.20	3.20	3.20	mA	
I _{DD5AB2H}	V _{DD2H}	26.50	26.50	27.00	27.00		
I _{DD5AB2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD5ABQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD5PB1}	V _{DD1}	3.20	3.20	3.20	3.20	mA	
I _{DD5PB2H}	V _{DD2H}	26.50	26.50	27.00	27.00		
I _{DD5PB2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD5PBQ}	V _{DDQ}	0.60	0.60	0.60	0.60		

- Notes: 1. Applies to entire table: Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27–0.37V (DVFSQ enabled); T_C = –25°C to +85°C
6. Notes 1, 2, and 5 apply to entire table.

Table 17: WT I_{DD} Parameters – With DVFSC Enabled - Single Die

Symbol	Supply	Speed Grade		Unit	Note
		x8 Mode	x16 Mode		
		1600 Mb/s	1600 Mb/s		
I _{DD4R-DVFSC1}	V _{DD1}	–	–	mA	4
I _{DD4R-DVFSC2H}	V _{DD2H}	–	–		
I _{DD4R-DVFSC2L}	V _{DD2L}	–	–		
I _{DD4R-DVFSCQ}	V _{DDQ}	–	–		
I _{DD4W-DVFSC1}	V _{DD1}	–	–	mA	
I _{DD4W-DVFSC2H}	V _{DD2H}	–	–		
I _{DD4W-DVFSC2L}	V _{DD2L}	–	–		
I _{DD4W-DVFSCQ}	V _{DDQ}	–	–		

- Notes: 1. Applies to entire table: Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC enabled, DVFSQ enabled, 1600 Mb/s, 16B mode.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSC disabled)/0.27–0.37V (DVFSC enabled); T_C = –25°C to +85°C
6. Notes 1, 2, 3, and 5 apply to entire table.

Table 18: WT Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit	Notes
25°C	I _{DD61}	V _{DD1}	0.27	mA	
	I _{DD62H}	V _{DD2H}	0.60		
	I _{DD62L}	V _{DD2L}	2.00	uA	4
	I _{DD6Q}	V _{DDQ}	30.00		
	I _{DD6DS1}	V _{DD1}	0.27	mA	
	I _{DD6DS2H}	V _{DD2H}	0.60		
	I _{DD6DS2L}	V _{DD2L}	2.00	uA	4
	I _{DD6DSQ}	V _{DDQ}	30.00		
45°C	I _{DD61}	V _{DD1}	TBD	mA	
	I _{DD62H}	V _{DD2H}	TBD		
	I _{DD62L}	V _{DD2L}	TBD	uA	4
	I _{DD6Q}	V _{DDQ}	TBD		
	I _{DD6DS1}	V _{DD1}	TBD	mA	
	I _{DD6DS2H}	V _{DD2H}	TBD		
	I _{DD6DS2L}	V _{DD2L}	TBD	uA	4
	I _{DD6DSQ}	V _{DDQ}	TBD		
65°C	I _{DD61}	V _{DD1}	TBD	mA	
	I _{DD62H}	V _{DD2H}	TBD		
	I _{DD62L}	V _{DD2L}	TBD	uA	4
	I _{DD6Q}	V _{DDQ}	TBD		
	I _{DD6DS1}	V _{DD1}	TBD	mA	
	I _{DD6DS2H}	V _{DD2H}	TBD		
	I _{DD6DS2L}	V _{DD2L}	TBD	uA	4
	I _{DD6DSQ}	V _{DDQ}	TBD		
85°C	I _{DD61}	V _{DD1}	3.30	mA	
	I _{DD62H}	V _{DD2H}	13.00		
	I _{DD62L}	V _{DD2L}	0.20	mA	4
	I _{DD6Q}	V _{DDQ}	0.60		
	I _{DD6DS1}	V _{DD1}	3.30	mA	
	I _{DD6DS2H}	V _{DD2H}	13.00		
	I _{DD6DS2L}	V _{DD2L}	0.20	mA	4
	I _{DD6DSQ}	V _{DDQ}	0.60		

- Notes: 1. I_{DD625/45/65°C} is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD685°C} is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
4. While entering and exiting self-refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the self-refresh with power down mode entrance commands are completed and t_{ESPD} timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.

Table 19: IT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I _{DD01}	V _{DD1}	3.30	3.30	3.30	3.30	mA	
I _{DD02H}	V _{DD2H}	30.50	30.50	31.00	31.00		
I _{DD02L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD0Q}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2P1}	V _{DD1}	1.60	1.60	1.60	1.60	mA	
I _{DD2P2H}	V _{DD2H}	2.70	2.70	2.70	2.70		
I _{DD2P2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2PQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2PS1}	V _{DD1}	1.60	1.60	1.60	1.60	mA	
I _{DD2PS2H}	V _{DD2H}	2.70	2.70	2.70	2.70		
I _{DD2PS2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2PSQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2N1}	V _{DD1}	1.60	1.60	1.60	1.60	mA	
I _{DD2N2H}	V _{DD2H}	17.50	17.50	18.00	18.00		
I _{DD2N2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2NQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD2NS1}	V _{DD1}	1.60	1.60	1.60	1.60	mA	
I _{DD2NS2H}	V _{DD2H}	17.50	17.50	18.00	18.00		
I _{DD2NS2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD2NSQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD3P1}	V _{DD1}	1.60	1.60	1.60	1.60	mA	
I _{DD3P2H}	V _{DD2H}	7.00	7.00	7.00	7.00		
I _{DD3P2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD3PQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD3PS1}	V _{DD1}	1.60	1.60	1.60	1.60	mA	
I _{DD3PS2H}	V _{DD2H}	7.00	7.00	7.00	7.00		
I _{DD3PS2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD3PSQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD3N1}	V _{DD1}	1.90	1.90	1.90	1.90	mA	
I _{DD3N2H}	V _{DD2H}	22.50	22.50	23.00	23.00		
I _{DD3N2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD3NQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD4R1}	V _{DD1}	9.00	10.00	11.00	12.00	mA	3, 4
I _{DD4R2H}	V _{DD2H}	300.00	330.00	440.00	490.00		
I _{DD4R2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD4RQ}	V _{DDQ}	58.00	63.00	116.00	126.00		

Table 19: IT I_{DD} Parameters – Single Die (Continued)

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I _{DD4W1}	V _{DD1}	8.00	9.00	10.00	11.00	mA	3
I _{DD4W2H}	V _{DD2H}	230.00	250.00	310.00	340.00		
I _{DD4W2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD4WQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD51}	V _{DD1}	23.00	23.00	23.00	23.00	mA	
I _{DD52H}	V _{DD2H}	165.00	165.00	165.00	165.00		
I _{DD52L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD5Q}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD5AB1}	V _{DD1}	3.20	3.20	3.20	3.20	mA	
I _{DD5AB2H}	V _{DD2H}	26.50	26.50	27.00	27.00		
I _{DD5AB2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD5ABQ}	V _{DDQ}	0.60	0.60	0.60	0.60		
I _{DD5PB1}	V _{DD1}	3.20	3.20	3.20	3.20	mA	
I _{DD5PB2H}	V _{DD2H}	26.50	26.50	27.00	27.00		
I _{DD5PB2L}	V _{DD2L}	0.20	0.20	0.20	0.20		
I _{DD5PBQ}	V _{DDQ}	0.60	0.60	0.60	0.60		

- Notes: 1. Applies to entire table: Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27–0.37V (DVFSQ enabled); T_C = –40°C to +95°C
6. Notes 1, 2, and 5 apply to entire table.

Table 20: IT I_{DD} Parameters – With DVFSC Enable - Single Die

Symbol	Supply	Speed Grade		Unit	Note
		x8 Mode	x16 Mode		
		1600 Mb/s	1600 Mb/s		
I _{DD4R-DVFSC1}	V _{DD1}	–	–	mA	4
I _{DD4R-DVFSC2H}	V _{DD2H}	–	–		
I _{DD4R-DVFSC2L}	V _{DD2L}	–	–		
I _{DD4R-DVFSCQ}	V _{DDQ}	–	–		
I _{DD4W-DVFSC1}	V _{DD1}	–	–	mA	
I _{DD4W-DVFSC2H}	V _{DD2H}	–	–		
I _{DD4W-DVFSC2L}	V _{DD2L}	–	–		
I _{DD4W-DVFSCQ}	V _{DDQ}	–	–		

- Notes: 1. Applies to entire table: Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC enabled, DVFSQ enabled, 1600 Mb/s, 16B mode
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27–0.37V (DVFSQ enabled); T_C = –40°C to +95°C
6. Notes 1, 2, 3, and 5 apply to entire table.

Table 21: IT Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit	Notes
25°C	I _{DD61}	V _{DD1}	0.27	mA	
	I _{DD62H}	V _{DD2H}	0.60		
	I _{DD62L}	V _{DD2L}	2.00	uA	4
	I _{DD6Q}	V _{DDQ}	30.00		
	I _{DD6DS1}	V _{DD1}	0.27	mA	
	I _{DD6DS2H}	V _{DD2H}	0.60		
	I _{DD6DS2L}	V _{DD2L}	2.00	uA	4
	I _{DD6DSQ}	V _{DDQ}	30.00		
45°C	I _{DD61}	V _{DD1}	–	mA	
	I _{DD62H}	V _{DD2H}	–		
	I _{DD62L}	V _{DD2L}	–	uA	4
	I _{DD6Q}	V _{DDQ}	–		
	I _{DD6DS1}	V _{DD1}	–	mA	
	I _{DD6DS2H}	V _{DD2H}	–		
	I _{DD6DS2L}	V _{DD2L}	–	uA	4
	I _{DD6DSQ}	V _{DDQ}	–		
65°C	I _{DD61}	V _{DD1}	–	mA	
	I _{DD62H}	V _{DD2H}	–		
	I _{DD62L}	V _{DD2L}	–	uA	4
	I _{DD6Q}	V _{DDQ}	–		
	I _{DD6DS1}	V _{DD1}	–	mA	
	I _{DD6DS2H}	V _{DD2H}	–		
	I _{DD6DS2L}	V _{DD2L}	–	uA	4
	I _{DD6DSQ}	V _{DDQ}	–		
85°C	I _{DD61}	V _{DD1}	3.30	mA	
	I _{DD62H}	V _{DD2H}	13.00		
	I _{DD62L}	V _{DD2L}	0.20	mA	4
	I _{DD6Q}	V _{DDQ}	0.60		
	I _{DD6DS1}	V _{DD1}	3.30	mA	
	I _{DD6DS2H}	V _{DD2H}	13.00		
	I _{DD6DS2L}	V _{DD2L}	0.20	mA	4
	I _{DD6DSQ}	V _{DDQ}	0.60		

Notes: 1. I_{DD625/45/65°C} is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD685°C} is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.

2. DVFSC and DVFSQ disabled.

3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –40°C to +95°C

4. While entering and exiting self-refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the self-refresh with power down mode entrance commands are completed and t_{ESPD} timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.

Revision History

Rev. F – 05/2024

- Updated Note #1 on features page
- Changed Package Thermal Resistance to Package Thermal Impedance

Rev. E – 11/2023

- Added 563-ball package details to feature description page
- Updated important notes and warnings section
- Updated General Notes to highlight precedence between core data sheet and specific data sheet
- Added adjustments to CS Rx and DQ Rx mask parameters
- Added table for DQ Rx adjustments at 3200 MHz
- Added 563-ball AJ and AH package descriptions and mechanical drawings
- Added Package Thermal Resistance Characteristics details
- Updated MR1: Added DRFM support bit definition
- Added MR4 to the register definition section along with Note 7 to highlight how refresh rate is defined
- Updated MR24: Added DFE support bit setting
- Updated MR41: Added E-DVFS ODT OP support setting
- Added DVFS enabled I_{DD} parameters to I_{DD} tables. Parameters affected = I_{DD4R} , I_{DD4W}
- Updated I_{DD6} Note 4 to align with core data sheet description
- Added I_{DD6} table entries for 45°C and 65°C, adjusted I_{DD6} IT limits to align with WT
- Removed I_{DD3NS} from I_{DD} tables

Rev. D – 11/2022

- Updated legal status to Production
- Updated general clarifications, namely on page #1
- Updated Mode Register Contents table: Corrected values
- Updated IT I_{DD} Parameters – Single Die table
- Fixed typo's in images

Rev. C – 06/2022

- Updated I_{DD} Parameters
- Updated details on Features page in options column to improve description

Rev. B – 04/2022

- Corrected MR settings and added a note to highlight the 3 step DFE support.
- Added Part Number Table
- Added I_{DD} max data for WT/IT temps, 7500/8533 data rates
- Updated package description to include RoHS -compliant as well as already having the “green” notation

Rev. A – 02/2022

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.