



ZHEJIANG UNIU-NE Technology CO., LTD

浙江宇力微新能源科技有限公司



U3406 Data Sheet

V0.4

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■ General Description

The U3406 400V synchronous buck controller regulates from a high input voltage source or from an input rail subject to high voltage transients, minimizing the need for external surge suppression components. A high-side switch minimum on-time of 60 ns gives large step-down ratios, enabling the direct step-down conversion from a 100V nominal input to low-voltage rails for reduced system complexity and solution cost. The U3406 continues to operate during input voltage dips as low as 8.5V, at nearly 100% duty cycle if needed, making it an excellent choice for high-performance 100V battery automotive applications, ADAS (surround view ECU) and HEV/EV systems.

Forced-PWM (FPWM) operation eliminates switching frequency variation to minimize EMI, while user-selectable diode emulation lowers current consumption at light-load conditions. Measuring the voltage drop across the low-side MOSFET or with an optional current sense resistor gives cycle-by-cycle overcurrent protection. The adjustable switching frequency as high as 0.5MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

■ Applications

- High-Power Automotive DC/DC Regulator
- Automotive Motor Drives, ADAS
- HEV/EV Power Compliant to LV-148

■ Key Features

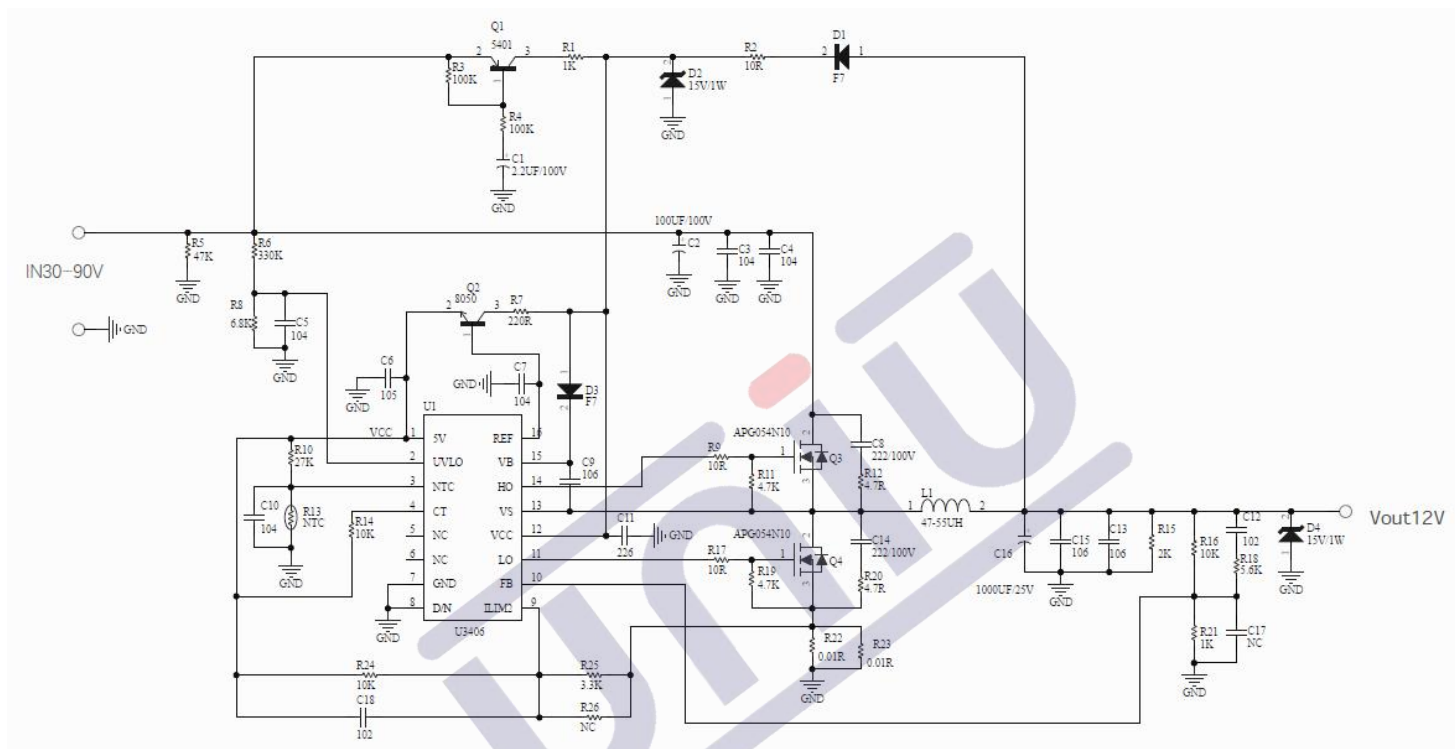
- Device Temperature Grade 1: -40°C to +80°C Ambient Temperature Range
- Versatile Synchronous Buck DC/DC Controller
 - Wide Input Voltage Range of 9.5V to 400V
 - Adjustable Output Voltage From 1.25V to 280V
 - Voltage-mode Control With Line Feedforward
- Three-stage frequency conversion
- 60ns Minimum On-Time for High V_{IN} / V_{OUT} Ratio
- 180ns Minimum Off-Time for Low Dropout
- 1.1V Reference With $\pm 1\%$ Feedback Accuracy
- 8.5V Gate Drivers for Standard V_{TH} MOSFETs
 - 220ns Adaptive Dead-Time Control
 - 2A Source and 2.5A Sink Capability
- Inherent Protection Features for Robust Design
 - Hiccup-Mode Overcurrent Protection
 - Input UVLO With Hysteresis
 - VCC and Gate-Drive UVLO Protection
 - Thermal Shutdown Protection With Hysteresis
- 16-Pin SOP Package With Wettable Flanks
- Create a Custom Design Using the U3406 With UNI-SEMI[®] Power Designer

■ Device Information⁽¹⁾

Part Number	Package	Body Size (Nom)
U3406	SOP(16)	10mm × 6.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet

■ Simple application diagram



■ Output Power Table

Part Number	Package	VIN	IO+/IO-	OUT
U3406	SOP-16	9.5~400V	2A/2.5A	ADJ

Note:

- 1.Default for Buck Converter Application
- 2.The practical output power is determined by the output voltage and thermal condition

■ Description (continued)

The U3406 voltage-mode controller with line feedforward drives external high-side and low-side N-channel power switches with robust 8.5V gate drivers suitable for standard-threshold MOSFETs. Adaptively-timed gate drivers with 2A source and 2.5A sink capability minimize body diode conduction during switching transitions, reducing switching losses and improving thermal performance when driving

MOSFETs at high input voltage and high frequency. The U3406 can be powered from the output of the switching regulator or another available source, further improving efficiency.

Additional features of the U3406 include a configurable soft start, an open-drain power-good monitor for fault reporting and output- monitoring, monotonic start-up into prebiased loads, integrated VCC bias supply regulator and bootstrap diode, external power supply tracking, precision enable input with hysteresis for adjustable line undervoltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The U3406 controller is offered in a 10mm × 6.3mm thermally enhanced, 16-pin SOP package with additional spacing for high-voltage pins and wettable flanks for optical inspection of solder joint fillets.

■ Pin Configuration and Functions

RGY Package 16-Pin SOP With Wettable Flanks

Top View

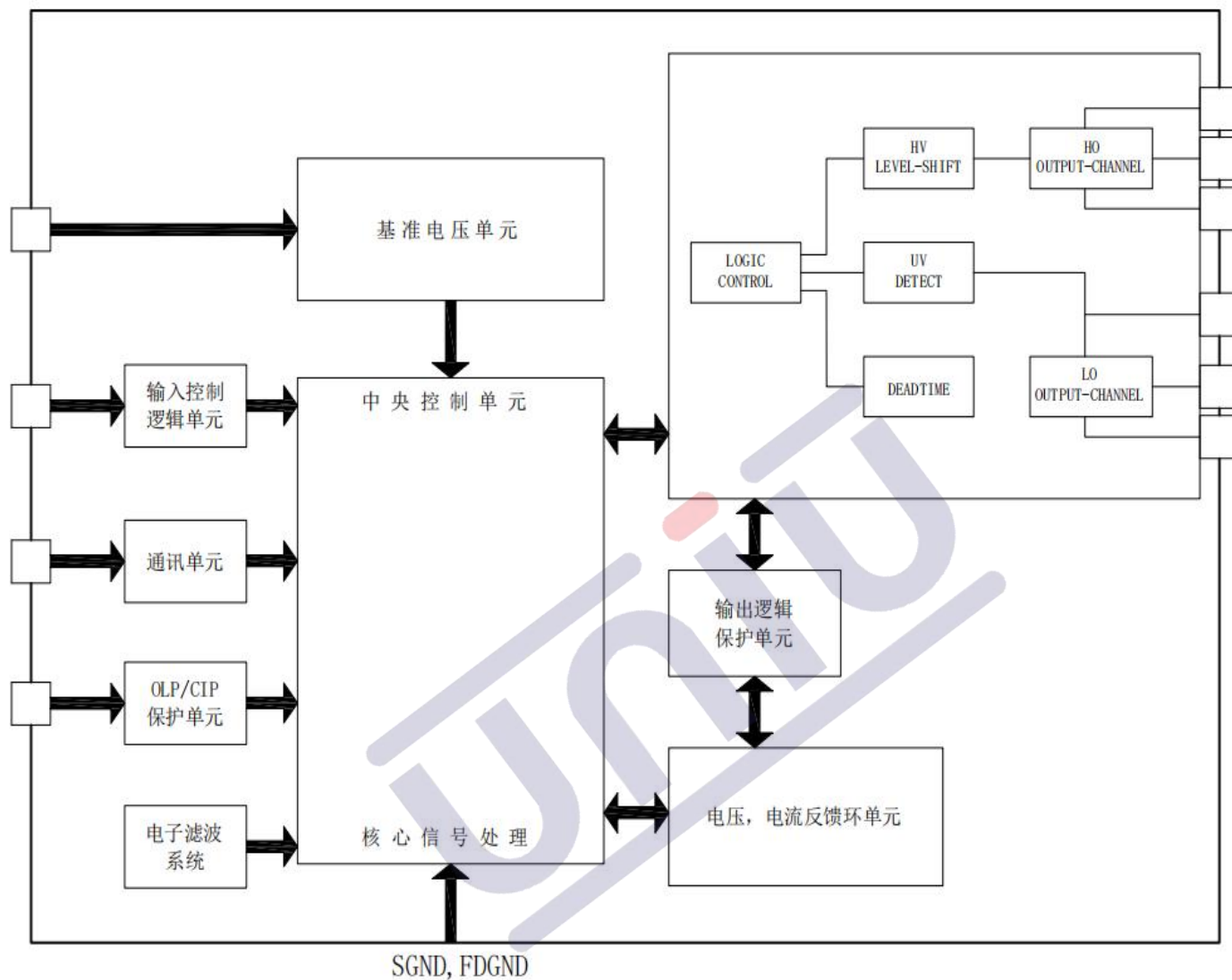


■ Pin Functions

Pin		I/O ⁽¹⁾	Description
NO.	Name		
1	5V	O	The Pin is VCC 5V
2	UVLO	I	Voltage detection
3	NTC	P	Enable input and under voltage lockout programming pin. If the EN/UVLO voltage is below 1V, Power on again after temperature protection
4	EN	I	Test PIN& Standby IO port
5	NC	I	NC
6	NC	I	NC
7	GND	P	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low- side MOSFET or the ground side of a shunt resistor.
8	D/N	I	Shutdown delay selection function (Low level real-time shutdown, high level delay 8 seconds shutdown)
9	ILIM2	I	Current detection in three-wire connection. Ultra-low overload protection below 1V, short circuit protection below 0.7V
10	FB	I	Feedback input. The regulation threshold at the FB pin is nominally 1.1V.
11	LO	P	Low-side MOSFET gate drive output.
12	VCC	O	Power input
13	VS	P	Switching node of the buck controller.
14	HO	P	High-side MOSFET gate drive output.
15	VB	O	Bootstrap supply for the high-side gate driver. Connect to the bootstrap (boot) capacitor.
16	REF	O	the reference for VCC5V.

(1) P = Power, G = Ground, I = Input, O = Output.

■ Functional Block Diagram



■ Specifications

● Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted)⁽¹⁾.

Item		Min	Max	Unit
Input voltages	VS	-1	VB-25	V
	VS (20ns transient)	-5	400	
	LIMT2	0	7	
	UVLO/NTC/(D/N)	-0.3	7	
	VCC	-0.3	20	
	FB	-0.3	6	
Output voltages	VB	-0.3	400	V
	VB to VCC	—	400	
	VB to SW	-0.3	20	
	VCC to VB (20ns transient)	—	7	
	LO (20ns transient)	-3	—	
	REF	-0.3	7	
Operating junction temperature, T_J		—	150	$^{\circ}\text{C}$
Storage temperature, T_{stg}		-55	150	$^{\circ}\text{C}$

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

● ESD Ratings

Item		Description	Value	Unit
V_{ESD}	Electrostatic discharge	HBM ESD Classification Level 2	± 2000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

● Recommended Operating Conditions

Over the recommended operating junction temperature range of -20°C to 80°C (unless otherwise noted)⁽¹⁾.

Item				Min	Nom	Max	Unit
V _I	Input voltages	VIN	U3406	10	—	25	V
		SW		-1	—	400	
		LIMT2		0	—	5	
		UVLO\(\overline{D}/N\)		-0.3	—	5	
V _O	Output voltages	BST		-0.3	—	412	V
		BST to VCC		-0.3	—	400	
		BST to SW		22	—	13	
		REF		—	—	5	
I _{SINK} , I _{SRC}	Sink/source currents	EN/UVLO		-1	—	1	mA
T _J	Operating junction temperature			-20	—	80	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

● Thermal Information

Item	Thermal Metric ⁽¹⁾	U3406	Unit
		RGY (SOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.8	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	$^{\circ}\text{C}/\text{W}$
ψ_{JT}	Junction-to-top characterization parameter	1.4	$^{\circ}\text{C}/\text{W}$
ψ_{JB}	Junction-to-board characterization parameter	21.7	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	$^{\circ}\text{C}/\text{W}$

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

● Electrical Characteristics

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over the -20°C to 80°C junction temperature range unless otherwise stated. $V_{IN}=48\text{V}$, $V_{CC}=12\text{V}$, $V_{EN}/UVLO=5\text{V}$, unless otherwise stated⁽¹⁾⁽²⁾

Item	Parameter	Test Conditions	Min	Typ	Max	Unit
Input Supply						
V_{CC}	Operating input voltage range	$I_{VCC} \leq 10\text{mA}$ at $V_{VIN} = 12\text{V}$	10	—	18	V
I_{Q-RUN}	Operating input current, not switching	$V_{EN}/UVLO = 5\text{V}$,	—	1.8	2.1	mA
I_{Q-STBY}	Standby input current	$V_{EN}/UVLO = 5\text{V}$	—	1.75	2	mA
I_{Q-SDN}	Shutdown input current	$V_{EN}/UVLO = 0\text{V}$, $V_{VCC} < 1\text{V}$	—	13.5	30	μA
REF/VCC Regulator						
V_{REF}	REF regulation voltage	$V_{CT1} = 0\text{V}$, $24\text{V} \leq V_{VIN} \leq 100\text{V}$, $0\text{mA} < I_{VCC} \leq 20\text{mA}$	—	5	—	V
I_{SC-LDO}	REF short-circuit current	$V_{REF} = 0\text{V}$ $V_{CC}=12\text{V}$	—	50	—	mA
V_{VCC-UV}	VCC undervoltage threshold	V_{VCC} rising	—	8.5	—	V
Enable And Input UVLO						
V_{EN}	Standby to operating threshold	$V_{EN}/UVLO}$ rising	—	1	—	V
I_{EN-HYS}	Standby to operating hysteresis	$V_{EN}/UVLO} = 1.5\text{V}$	9	10	11	μA
FB Reference						
V_{REF}	FB reference voltage		—	1200	—	mV
AVOL	DC gain		—	94	—	dB
GBW	Unity gain bandwidth		—	5	—	MHz
Current renferance						
V_{lim1}	I limit1 Reference Voltage	$V_{CC}=12\text{V}$	—	60	—	mV
V_{lim2}	I limit2 Reference Voltage	$V_{CC}=12\text{V}$	—	1	—	V
Oscillator						
F_{SW1}	Oscillator Frequency – 1	$V_{IN}=50\text{V}$	—	55	—	kHz
PWM Control						
$t_{ON(MIN)}$	Minimum controllable on-time	$V_{BST} - V_{SW} = 7\text{V}$, HO 50% to 50%	—	160	—	ns
$t_{OFF(MIN)}$	Minimum off-time	$V_{BST} - V_{SW} = 7\text{V}$, HO 50% to 50%	—	132	—	ns
DC _{80kHz}	Maximum duty cycle	$F_{SW} = 55\text{kHz}$, $6\text{V} \leq V_{VIN} \leq 60\text{V}$	—	70%	—	—
Gate Drivers						
I_{HOH} , I_{LOH}	HO, LO source current	$V_{BST} - V_{SW} = 7\text{V}$, HO=SW, LO=AGND	—	2.0	—	A
I_{HOL} , I_{LOL}	HO, LO sink current	$V_{BST} - V_{SW} = 7\text{V}$, HO=BST, LO=VCC	—	2.5	—	A
Thermal Shutdown						
T_{SD}	Thermal shutdown threshold	T_J rising	—	175	—	$^\circ\text{C}$
T_{SD-HYS}	Thermal shutdown hysteresis		—	20	—	$^\circ\text{C}$

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) The junction temperature (T_J in $^\circ\text{C}$) is calculated from the ambient temperature (T_A in $^\circ\text{C}$) and power dissipation (P_D in Watts) as follows:
 $T_J = T_A + (P_D \cdot R_{\theta JA})$ where $R_{\theta JA}$ (in $^\circ\text{C/W}$) is the package thermal impedance provided in Thermal Information.

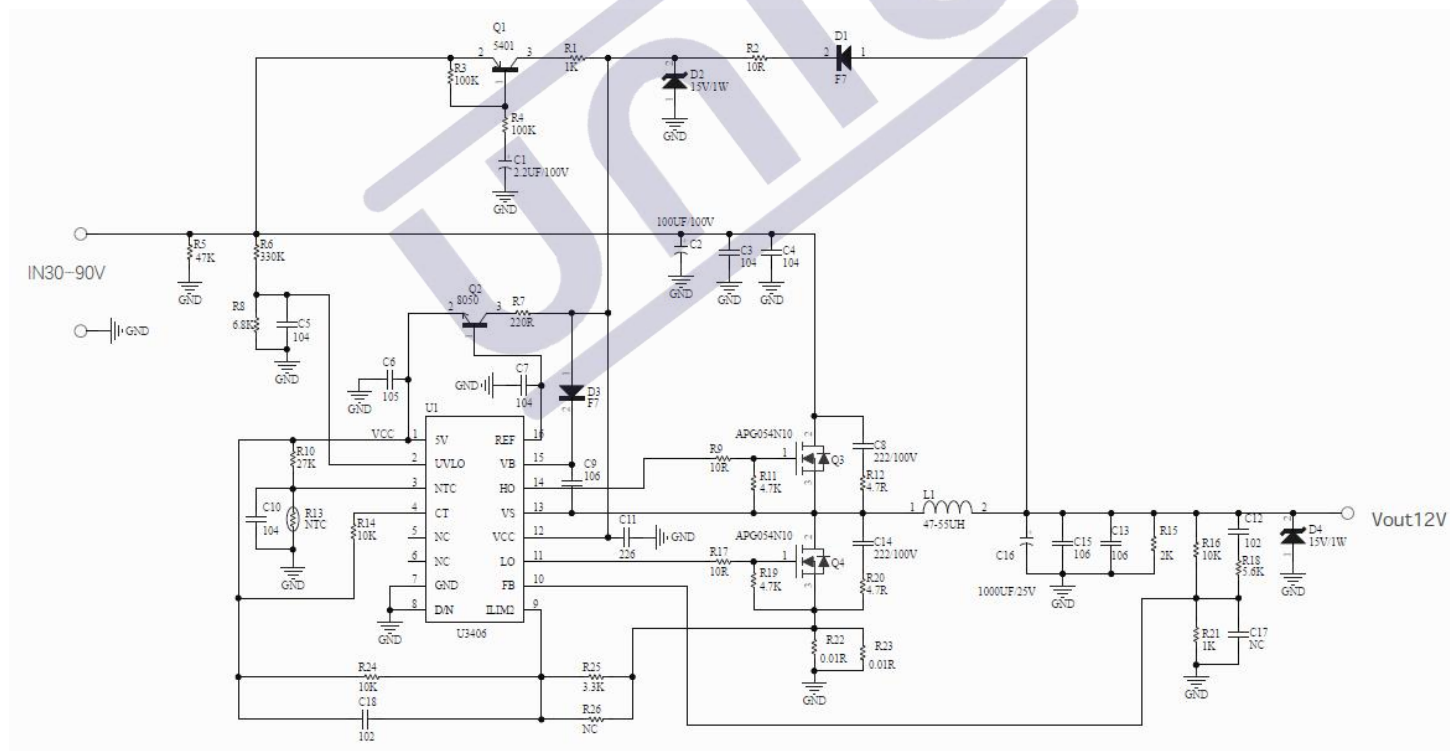
● Switching Characteristics

Typical values correspond to $T_J = 25^{\circ}\text{C}$

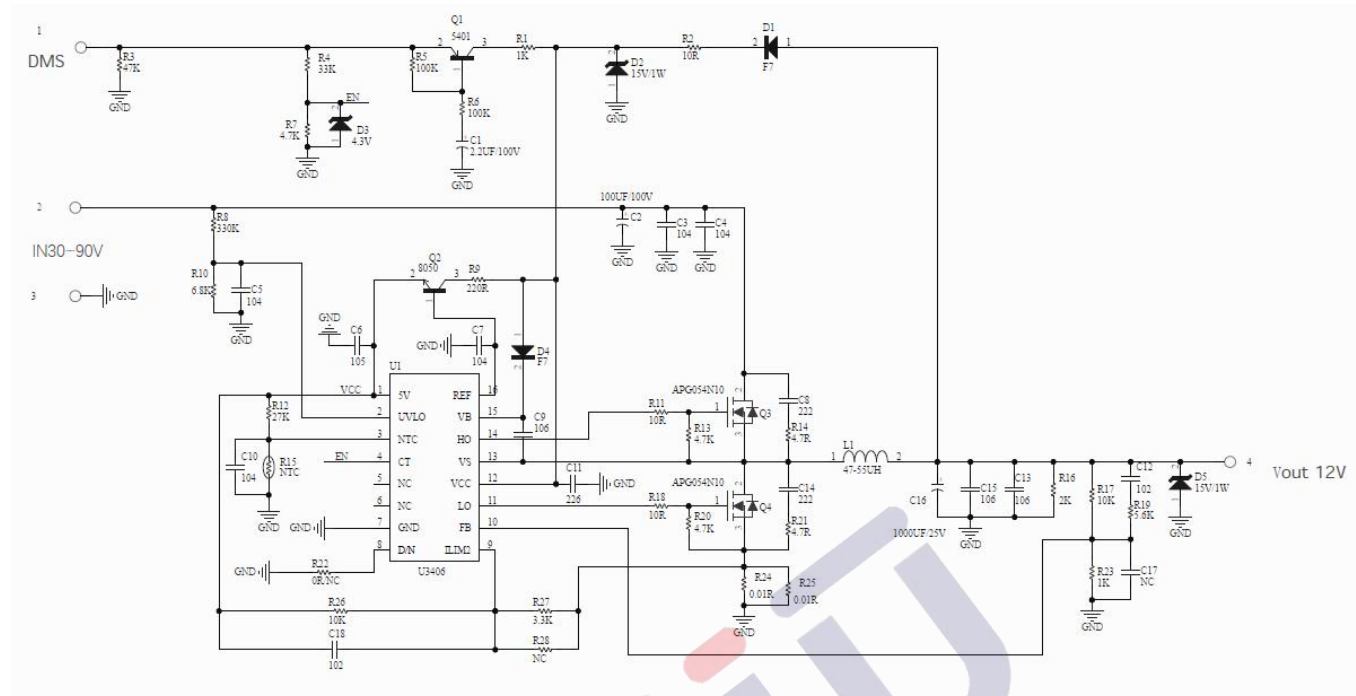
Item	Parameter	Test Conditions	Min	Typ	Max	Unit
T _{HO-TR} T _{LO-TR}	HO, LO rise times	V _{BST} – V _{SW} = 7 V, C _{LOAD} = 1 nF, 20% to 80%	—	25	35	ns
T _{HO-TF} T _{LO-TF}	HO, LO fall times	V _{BST} – V _{SW} = 7 V, C _{LOAD} = 1 nF, 80% to 20%	—	—	25	ns
T _{HO-DT}	HO turn-on dead time	V _{BST} – V _{SW} = 7 V, LO off to HO on, 50% to 50%	—	300	—	ns
T _{LO-DT}	LO turn-on dead time	V _{BST} – V _{SW} = 7 V, HO off to LO on, 50% to 50%	—	300	—	ns

■ Typical Application

APP1:Three-wire circuit diagram ((no electric door lock)



APP2: Four-wire circuit diagram (electric door lock)

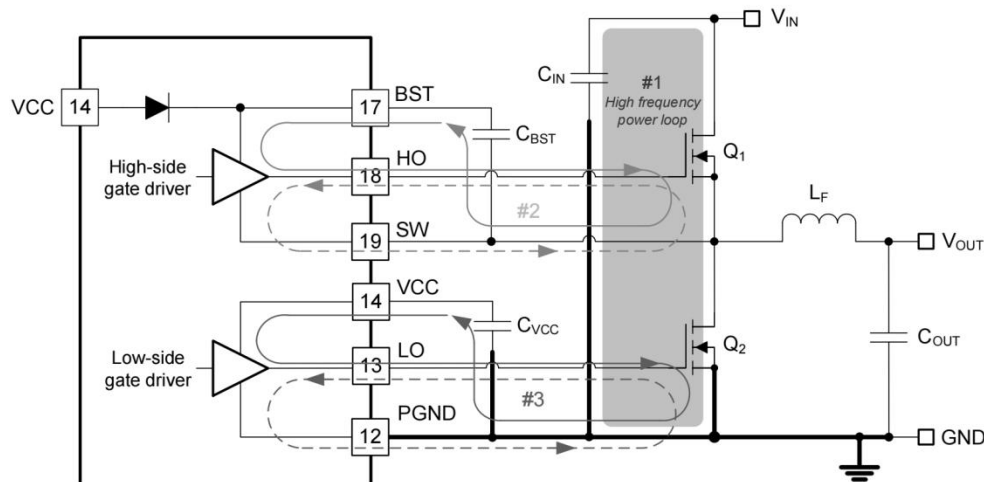


■ Layout

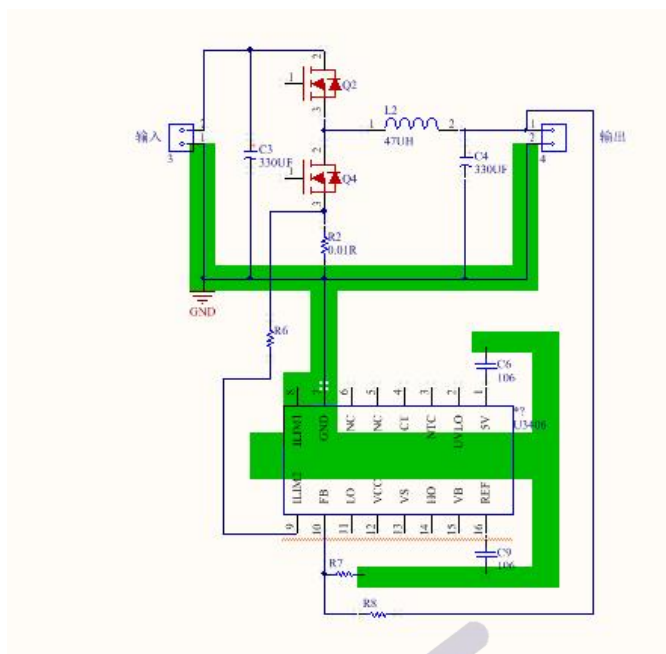
● Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the U3406. The high-frequency power loop of the buck converter power stage is denoted by #1 in the shaded area of Figure 70. The topological architecture of a buck converter means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3.

DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops



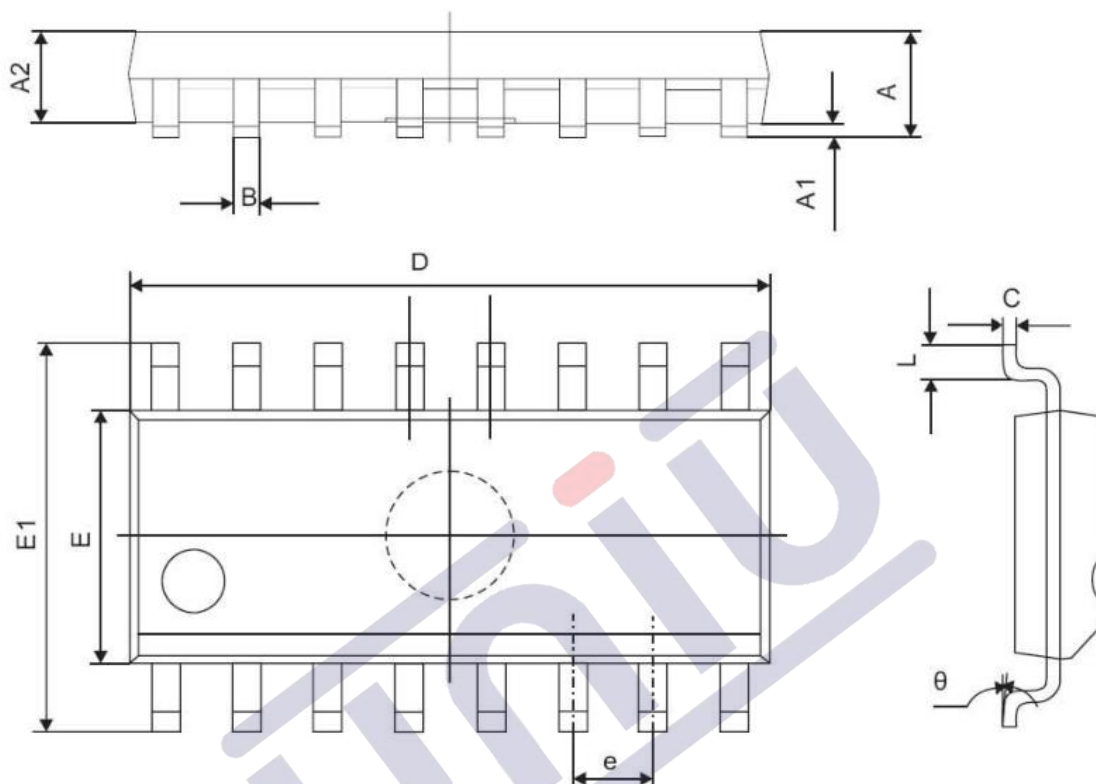
Three wire step-down circuit ground Layout reference.



■ Mechanical Packaging and Orderable

● Mechanical Packaging

SOP-16



(mm)

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.300
e	1.270(TYP)	
L	0.400	1.270
θ	0°	8°

1、版本记录

DATE	REV.	DESCRIPTION
2022/09/28	0.1	首次发布
2023/10/08	0.2	更新应用原理图
2023/11/12	0.3	优化参数及应用原理图

2、免责声明

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