

1. Product profile

1.1 General description

550 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2100 MHz to 2200 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25^\circ\text{C}$ in an asymmetrical Doherty demo circuit. $V_{DS} = 29/32\text{ V}$; $I_{Dq} = 900\text{ mA}$ (main); $V_{GS(amp)peak} = 1.2\text{ V}$, unless otherwise specified.

Test signal	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
1-carrier W-CDMA	2110 to 2170	29	90	15.9	50.5	-28.5 [1]
	2110 to 2170	32	115	16.3	49.8	-29.1 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2100 MHz to 2200 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description	Version	
BLC10G22XS-551AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage		-	65	V	
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+9	V	
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+9	V	
T_{stg}	storage temperature		-65	+150	°C	
T_j	junction temperature	[1]	-	225	°C	
T_{case}	case temperature	operating	[1]	-40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 32$ V; $I_{Dq} = 900$ mA (main); $V_{GS(amp)peak} = 1.024$ V; $T_{case} = 80$ °C		
		$P_L = 87$ W	0.24	k/W
		$P_L = 110$ W	0.22	k/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$; $I_D = 1.8\text{ mA}$	65	-	-	V
$V_{\text{GS}(\text{th})}$	gate-source threshold voltage	$V_{\text{DS}} = 10\text{ V}$; $I_D = 180\text{ mA}$	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{\text{DS}} = 32\text{ V}$; $I_D = 800\text{ mA}$	-	2.2	-	V
I_{DSS}	drain leakage current	$V_{\text{GS}} = 0\text{ V}$; $V_{\text{DS}} = 32\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{\text{GS}} = V_{\text{GS}(\text{th})} + 2.37\text{ V}$; $V_{\text{DS}} = 10\text{ V}$	-	34	-	A
I_{GSS}	gate leakage current	$V_{\text{GS}} = 9\text{ V}$; $V_{\text{DS}} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{\text{DS}} = 10\text{ V}$; $I_D = 9.0\text{ A}$	-	20.5	-	S
$R_{\text{DS}(\text{on})}$	drain-source on-state resistance	$V_{\text{GS}} = V_{\text{GS}(\text{th})} + 2.37\text{ V}$; $I_D = 6.3\text{ A}$	-	72	108	$\text{m}\Omega$
Peak device						
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$; $I_D = 3.8\text{ mA}$	65	-	-	V
$V_{\text{GS}(\text{th})}$	gate-source threshold voltage	$V_{\text{DS}} = 10\text{ V}$; $I_D = 380\text{ mA}$	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{\text{DS}} = 32\text{ V}$; $I_D = 1900\text{ mA}$	-	2.2	-	V
I_{DSS}	drain leakage current	$V_{\text{GS}} = 0\text{ V}$; $V_{\text{DS}} = 32\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{\text{GS}} = V_{\text{GS}(\text{th})} + 2.37\text{ V}$; $V_{\text{DS}} = 10\text{ V}$	-	57	-	A
I_{GSS}	gate leakage current	$V_{\text{GS}} = 9\text{ V}$; $V_{\text{DS}} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{\text{DS}} = 10\text{ V}$; $I_D = 19.0\text{ A}$	-	39.0	-	S
$R_{\text{DS}(\text{on})}$	drain-source on-state resistance	$V_{\text{GS}} = V_{\text{GS}(\text{th})} + 2.37\text{ V}$; $I_D = 13.3\text{ A}$	-	37	62	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; $f_1 = 2112.5\text{ MHz}$; $f_2 = 2167.5\text{ MHz}$; RF performance at $V_{\text{DS}} = 32\text{ V}$; $I_{\text{Dq}} = 1000\text{ mA}$ (main); $V_{\text{GS}(\text{amp})\text{peak}} = 1.2\text{ V}$; $T_{\text{case}} = 25^\circ\text{C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2110 MHz to 2170 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{\text{L}(\text{AV})} = 115\text{ W}$	15.0	16.0	-	dB
RL_{in}	input return loss	$P_{\text{L}(\text{AV})} = 115\text{ W}$	-	-15	-10	dB
η_{D}	drain efficiency	$P_{\text{L}(\text{AV})} = 115\text{ W}$	46	50	-	%
ACPR	adjacent channel power ratio	$P_{\text{L}(\text{AV})} = 115\text{ W}$	-	-29	-24	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; $f = 2167.5\text{ MHz}$; RF performance at $V_{\text{DS}} = 32\text{ V}$; $I_{\text{Dq}} = 1000\text{ mA}$ (main); $V_{\text{GS}(\text{amp})\text{peak}} = 1.2\text{ V}$; $T_{\text{case}} = 25^\circ\text{C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 2170 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_{O}	output peak-to-average ratio	$P_{\text{L}(\text{AV})} = 145\text{ W}$	6.0	6.5	-	dB
$P_{\text{L}(\text{M})}$	peak output power	$P_{\text{L}(\text{AV})} = 145\text{ W}$	566	650	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G22XS-551AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 32$ V; $I_{Dq} = 1000$ mA; $V_{GS(\text{amp})\text{peak}} = 1.15$ V; $f = 2110$ MHz; $P_L = 235$ W (5 dB OBO); 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; $I_{Dq} = 900$ mA (main); $V_{DS} = 32$ V; pulsed CW ($t_p = 100$ μs ; $\delta = 10$ %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [2] (dB)
Maximum power load					
2110	2.8 – j6.5	1.6 – j4.0	298	58.2	15.2
2140	3.3 – j7.0	1.8 – j3.5	298	60.2	15.8
2170	4.1 – j7.2	1.6 – j3.5	295	57.6	15.6
Maximum drain efficiency load					
2110	3.2 – j6.9	4.0 – j2.4	198	69.5	17.9
2140	3.8 – j7.2	3.3 – j2.5	222	68.9	17.7
2170	4.7 – j7.4	2.9 – j2.3	222	68.6	17.8

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; $I_{Dq} = 1900$ mA (peak); $V_{DS} = 32$ V; pulsed CW ($t_p = 100$ μs ; $\delta = 10$ %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [2] (dB)
Maximum power load					
2110	1.9 – j6.0	2.0 – j3.7	596	62.2	14.8
2140	2.3 – j6.3	1.7 – j3.8	592	57.4	14.3
2170	2.8 – j6.6	1.6 – j3.5	583	59.6	14.8
Maximum drain efficiency load					
2110	2.0 – j6.0	2.7 – j2.8	502	67.4	15.9
2140	2.5 – j6.3	2.9 – j2.7	468	66.4	16.0
2170	3.0 – j6.7	2.3 – j2.5	471	66.6	16.2

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At 3 dB gain compression.

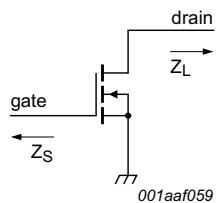


Fig 1. Definition of transistor impedance

7.3 Test circuit

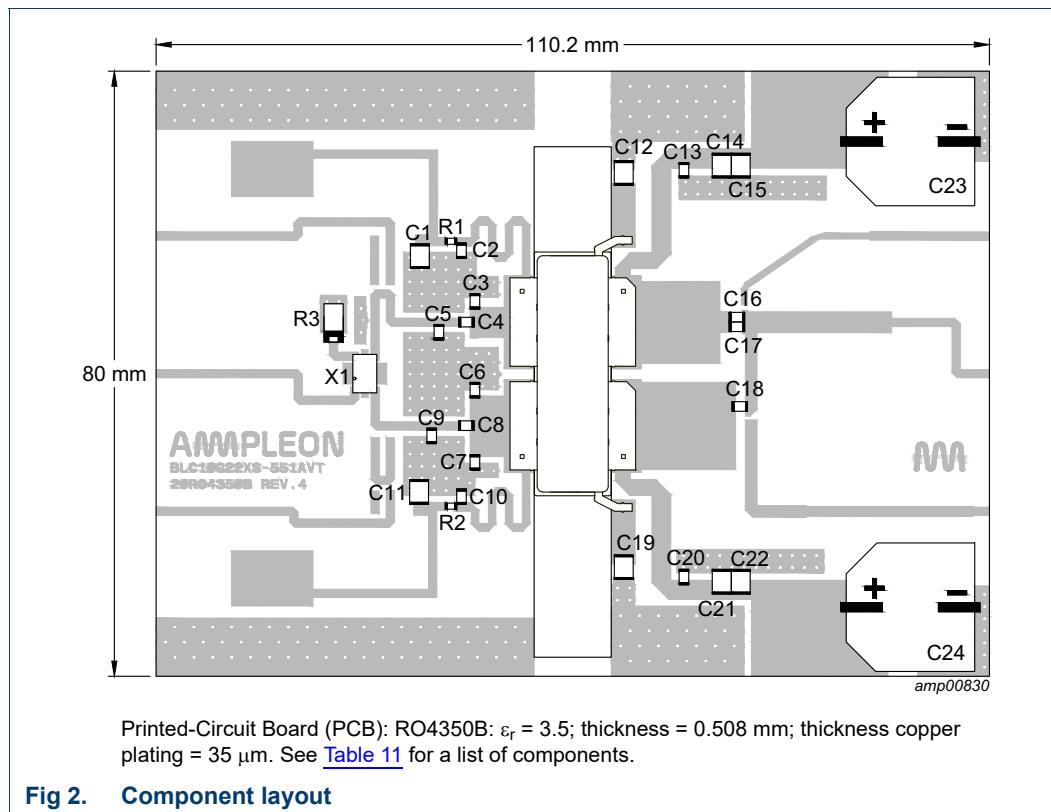


Table 11. List of components

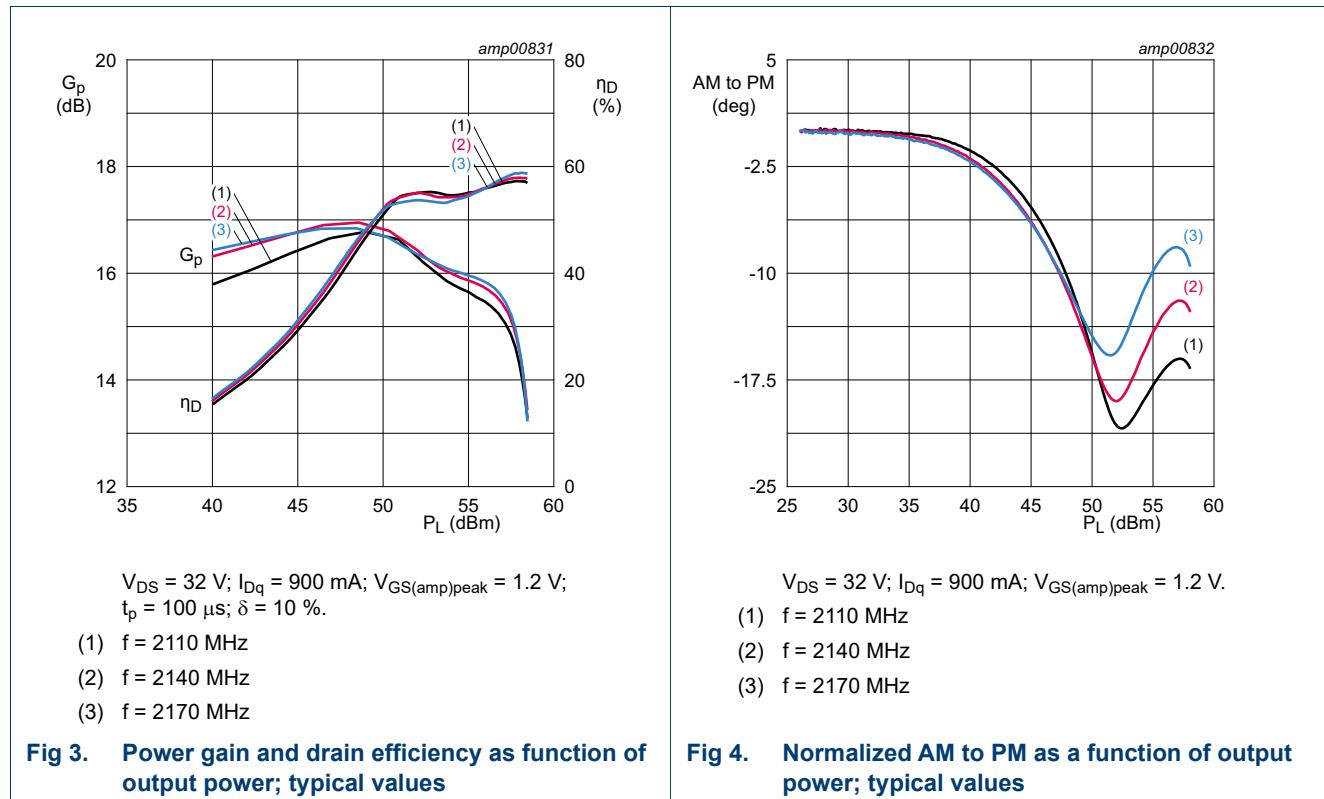
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C11, C12, C14, C15, C19, C21, C22	multilayer ceramic chip capacitor	10 μF , 100 V	X7S
C2, C4, C8, C10, C13, C18, C20	multilayer ceramic chip capacitor	10 pF	[1]
C3	multilayer ceramic chip capacitor	0.5 pF	[1]
C5	multilayer ceramic chip capacitor	0.8 pF	[1]
C6, C7	multilayer ceramic chip capacitor	1.0 pF	[1]
C9	multilayer ceramic chip capacitor	0.8 pF	[1]
C16	multilayer ceramic chip capacitor	2.2 pF	[1]
C17	multilayer ceramic chip capacitor	2.7 pF	[1]
C23, C24	electrolytic capacitor	470 μF , 63 V	EEVFK1J471M
R1, R2	resistor	4.7 Ω	
R3	resistor	50 Ω , 25 W	Anaren: C16A50Z4
X1	hybrid coupler	2 dB, 90°	Anaren: Xinger III, X3C20F1-02

[1] Murata: GQM21 series.

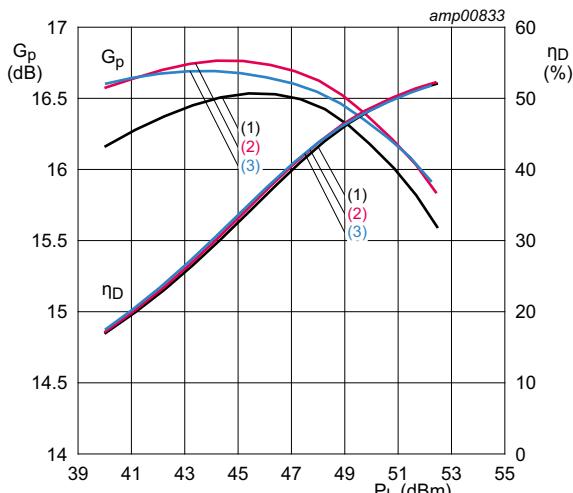
7.4 Graphical data

7.4.1 Pulsed CW



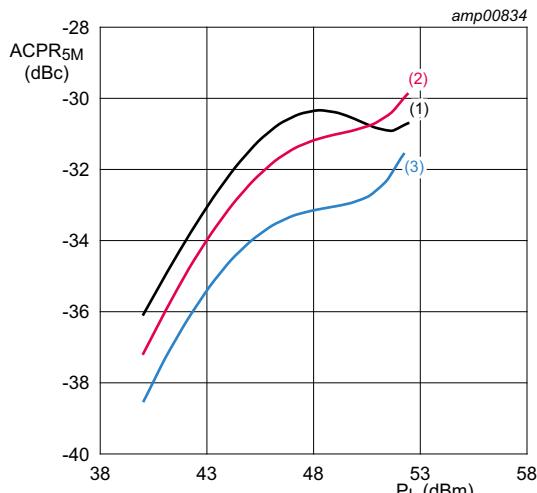
7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 1 to 64 DPCH (100 % clipping); PAR = 9.9 dB at 0.01 % probability on CCDF.



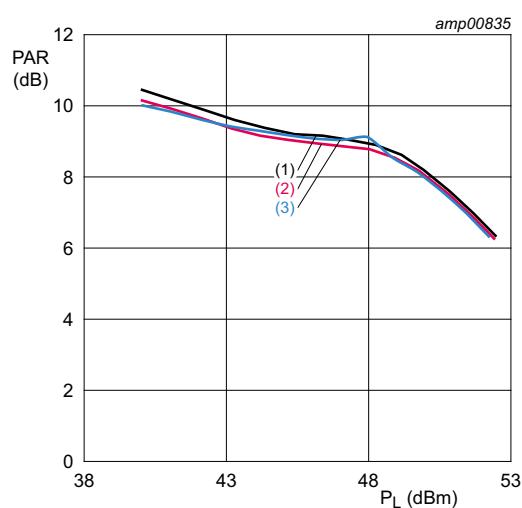
$V_{DS} = 32$ V; $I_{DQ} = 900$ mA; $V_{GS(amp)peak} = 1.2$ V.
 (1) $f = 2110$ MHz
 (2) $f = 2140$ MHz
 (3) $f = 2170$ MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 32$ V; $I_{DQ} = 900$ mA; $V_{GS(amp)peak} = 1.2$ V.
 (1) $f = 2110$ MHz
 (2) $f = 2140$ MHz
 (3) $f = 2170$ MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

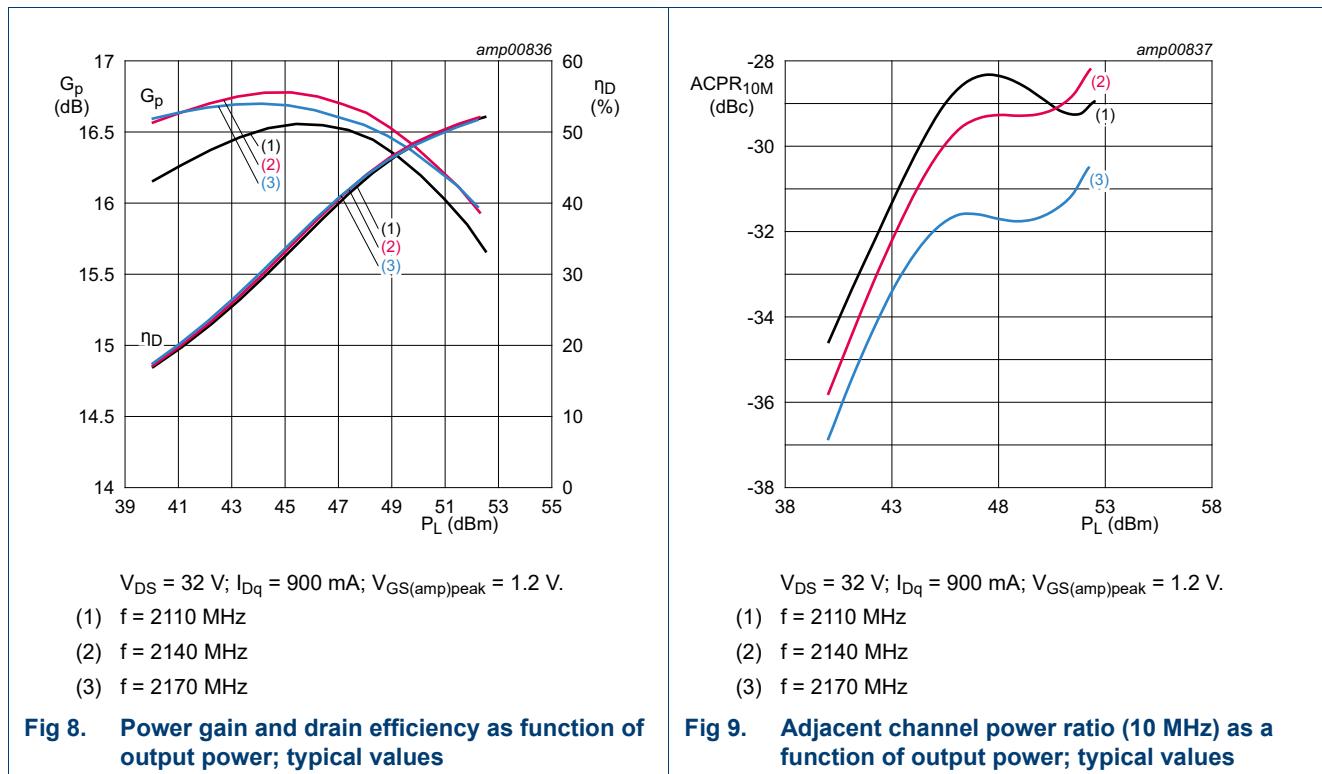


$V_{DS} = 32$ V; $I_{DQ} = 900$ mA; $V_{GS(amp)peak} = 1.2$ V.
 (1) $f = 2110$ MHz
 (2) $f = 2140$ MHz
 (3) $f = 2170$ MHz

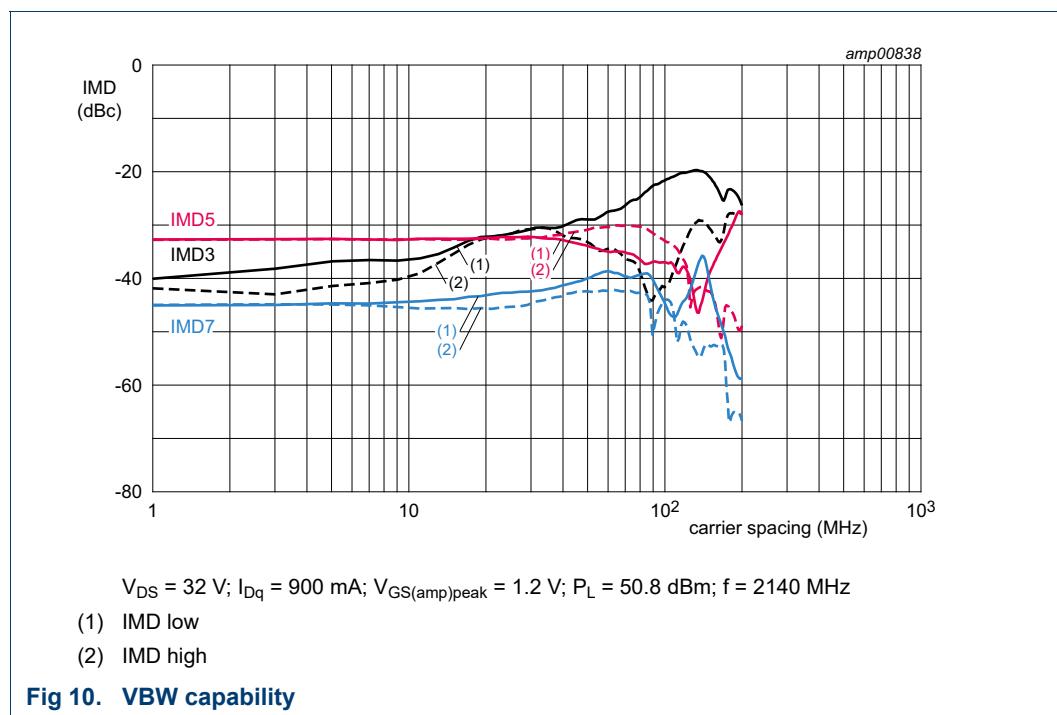
Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.4.3 1-Carrier LTE

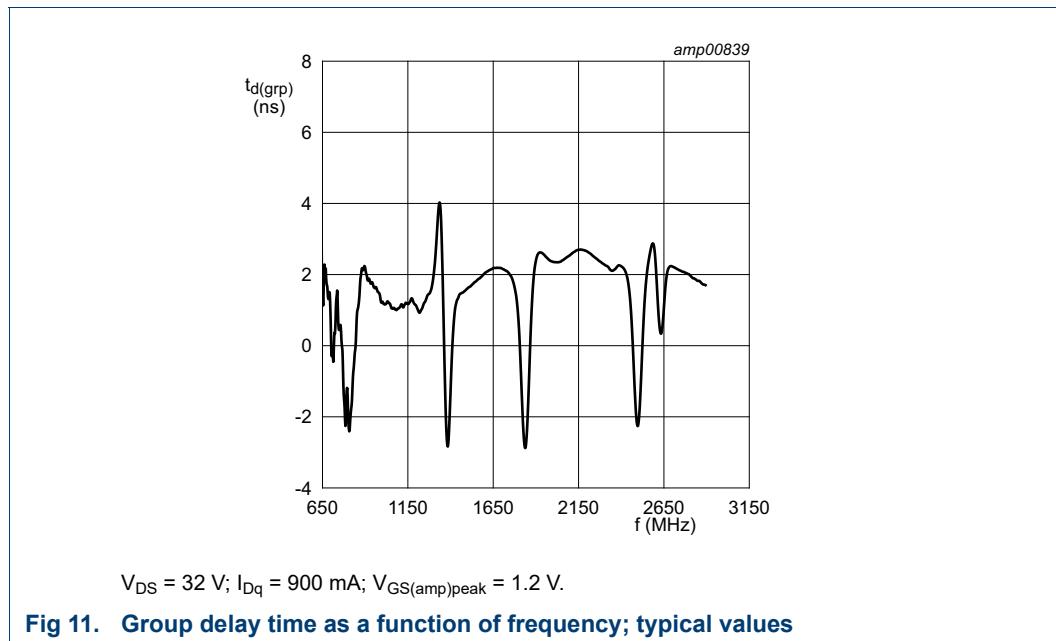
Test signal: 1-carrier LTE 10 MHz; PAR = 6.8 dB at 0.01 % probability on CCDF.



7.4.4 2-Tone VBW



7.4.5 Group delay



8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1258-4

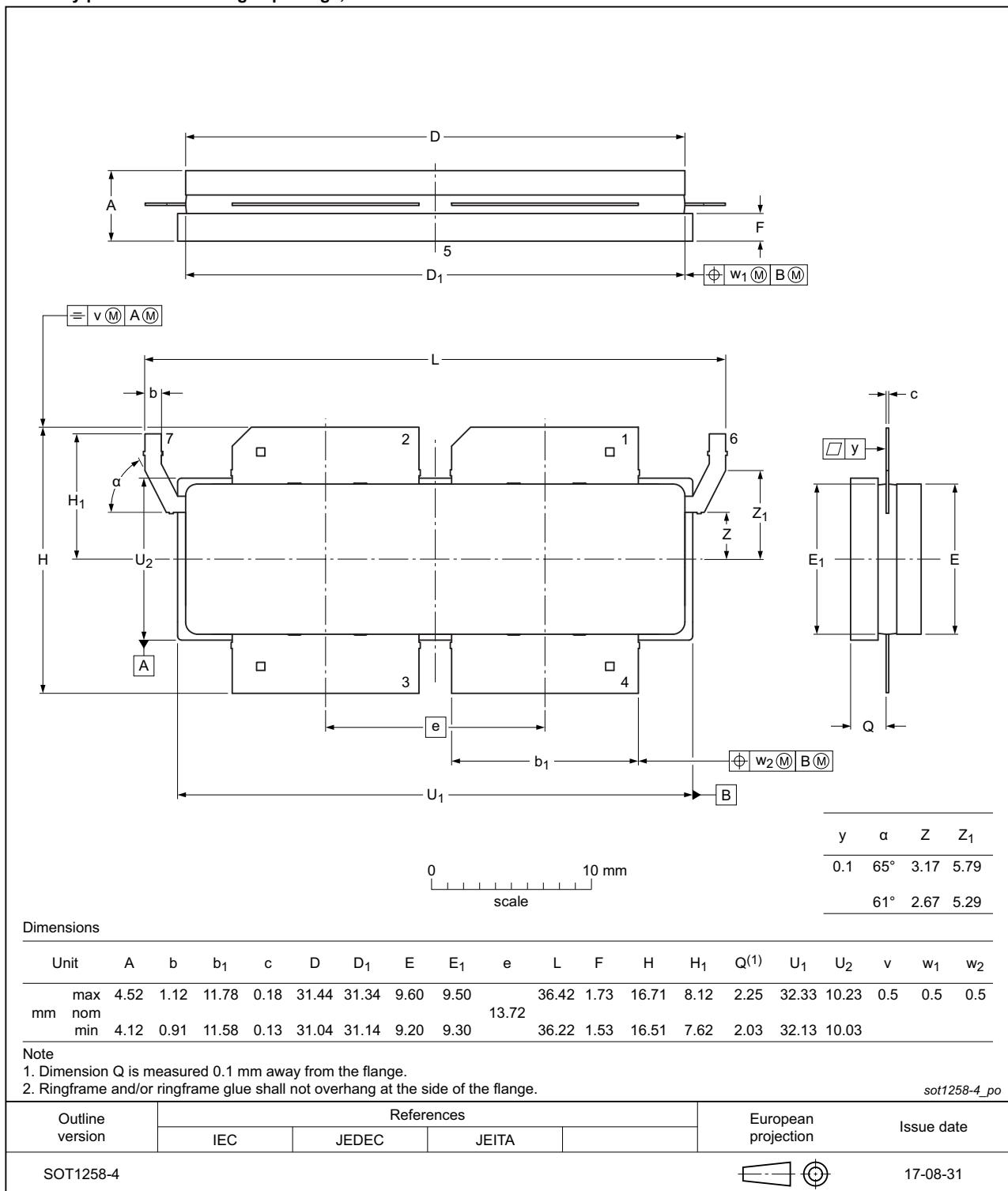


Fig 12. Package outline SOT1258-4

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
RoHS	Restriction of Hazardous Substances
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G22XS-551AVT v.2	20191107	Product data sheet	-	BLC10G22XS-551AVT v.1
Modifications:	<ul style="list-style-type: none"> Section 7.3 on page 6: added section 			
BLC10G22XS-551AVT v.1	20190307	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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