# HC2M0650170D

SiC Power MOSFET N-Channel Enhancement Mode

## Features

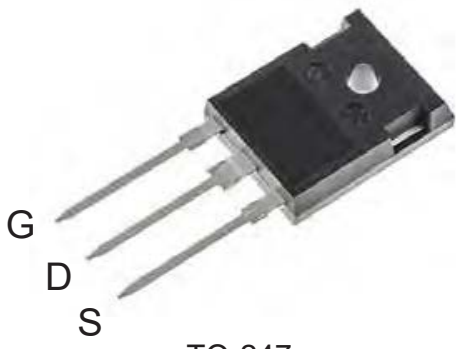
- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ($Q_{rr}$)
- Halogen free, RoHS compliant

## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch Mode Power Supplies

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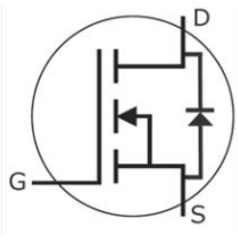
**Package**




| Ordering Part Number | Package | Marking |
|---|---|---|
| HC2M0650170D | TO-247 | HC2M0650170D |

## Maximum Ratings ($T_C$ = 25 ˚C unless otherwise specified)

| Symbol | Parameter | Value | Unit | Test Conditions | Note |
|---|---|---|---|---|---|
| $V_{DSmax}$ | Drain-Source Voltage | 1700 | V | $V_{GS}$ = 0 V, $I_D$ = 100 A | |
| $V_{GSmax}$ | Gate-Source Voltage | -10/+25 | V | Absolute maximum values | |
| $V_{GSop}$ | Gate-Source Voltage | -5/+20 | V | Recommend operationaled values | |
| $I_D$ | Continuous Drain Current | 7.0 | A | $V_{GS}$=20V, $T_c$=25˚C | Fig. 19 |
| | | 4.5 | | $V_{GS}$=20V, $T_c$=100˚C | |
| $I_{D(pulse)}$ | Pulsed Drain Current | 9.0 | A | Pulse width $t_p$ limited by $T_{Jmax}$ | Fig. 22 |
| $P_D$ | Power Dissipation | 62 | W | $T_c$=25˚C, $T_J$=150˚C | Fig. 20 |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperature | -55 to+150 | ˚C | | |
| $T_L$ | Solder Temperature, 1.6mm from case for 10S | 260 | ˚C | | |
| $M_d$ | Mounting Torque, (M3 or 6-32 screw) | 18.8 | Nmlbf-in | | |

## Electrical Characteristics ($T_C$=25℃ unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Train-SourceBreakdown Voltage | 1700 | / | / | V | $V_{SG}$=0V, $I_D$=100μA | |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | 2.6 | 4.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=1.0mA | Fig. 11 |
| | | / | 1.8 | / | | $V_{DS}$=$V_{GS}$, $I_D$=1.0mA, $T_J$=150℃ | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | / | 1 | 100 | μA | $V_{DS}$=1700V, $V_{GS}$=0V | |
| $I_{GSS+}$ | Gate-Source Leakage Current | / | 10 | 250 | nA | $V_{DS}$=0V, $V_{GS}$=25V | |
| $I_{GSS-}$ | Gate-Source Leakage Current | / | 10 | 250 | nA | $V_{DS}$=0V, $V_{GS}$=25V | |
| $R_{DS(on)}$ | Drain-Source On-State Resistance | / | 650 | 850 | mΩ | $V_{DS}$=0V, $V_{GS}$=-10V | Fig. 4,5,6 |
| | | / | 950 | / | | $V_{GS}$=20V, $I_D$=2A, $T_J$=150℃ | |
| $g_{fs}$ | Transconductance | / | 1.06 | / | S | $V_{DS}$=20V, $I_D$=2A | Fig. 7 |
| | | / | 1.14 | / | | $V_{DS}$=20V, $I_D$=2A, $T_J$=150℃ | |
| $C_{iss}$ | Input Capacitance | / | 198 | / | pF | $V_{GS}$=0V<br>$V_{DS}$=1000V<br>f=1MHz<br>$V_{AC}$=25mV | Fig. 17,18 |
| $C_{oss}$ | Output Capacitance | / | 13 | / | | | |
| $C_{rss}$ | Reverse Transfer Capacitance | / | 2.1 | / | | | |
| $E_{oss}$ | $C_{oss}$ Stored Energy | / | 6.6 | / | μJ | | Fig. 16 |
| $E_{ON}$ | Turn-On Switching Energy | / | 5 | / | mJ | $V_{DS}$=1200V, $V_{GS}$=-5V/20V<br>$I_D$=2A, $R_{G(ext)}$=2.5Ω, | |
| $E_{OFF}$ | Turn-Off Switching Energy | / | 9.2 | / | | | |
| $t_{d(on)}$ | Turn-On Delay Time | / | 13.8 | / | ns | L=1500μH<br>$V_{DS}$=1200V,<br>$V_{GS}$=-5V/20V<br>$I_D$=2A,$R_{G(ext)}$=2.5Ω,$R_L$=20Ω | |
| $t_r$ | Rise Time | / | 22.8 | / | | | |
| $t_{d(off)}$ | Turn-Off Delay Time | / | 38 | / | | | |
| $t_f$ | Fall Time | / | 14 | / | | | |
| $R_{G(int)}$ | Internal Gate Resistance | / | 18 | / | Ω | f=1MHz, $V_{AC}$=25mV | |
| $Q_{GS}$ | Gate to Source Charge | / | 5.4 | / | nC | $V_{DS}$=1200V<br>$V_{GS}$=-5V/20V<br>$I_D$=2A | Fig. 12 |
| $Q_{GD}$ | Gate to Drain Charge | / | 7.6 | / | | | |
| $Q_G$ | Total Gate Charge | / | 23 | / | | | |

## Reverse Diode Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Diode Forward Voltage | 4.2 | / | V | $V_{GS}$=-5V, $I_{SD}$=3.5A | Fig. 8,9,10 |
| | | 3.9 | / | | $V_{GS}$=-5V, $I_{SD}$=3.5A, $T_J$=150°C | |
| $I_S$ | Continuous Diode Forward Current | / | 7.0 | A | $T_C$=25°C | |
| $t_{rr}$ | Reverse Recover Time | 25 | / | ns | $V_R$=1200V, $I_{SD}$=2A | |
| $Q_{rr}$ | Reverse Recovery Charge | 15 | / | nC | | |
| $I_{rrm}$ | Peak Reverse Recovery Current | 2.8 | / | A | | |

## Thermal Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance from Junction to Case | 1.8 | / | °C/W | | |
| $R_{\theta JA}$ | Thermal Resistance from Junction to Ambient | / | 40 | | | |

## Typical Performance

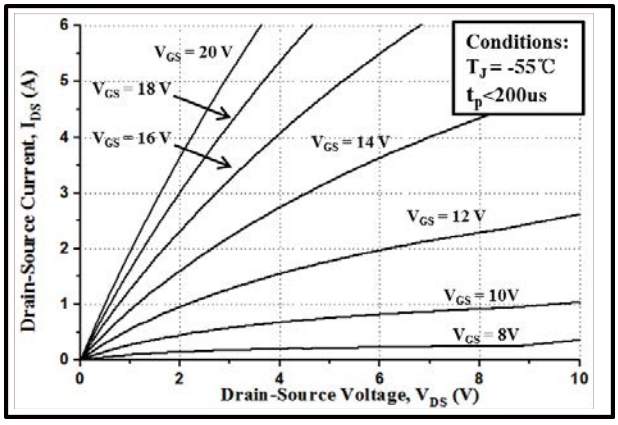



Figure 1. Output Characteristics $T_J$= -55℃

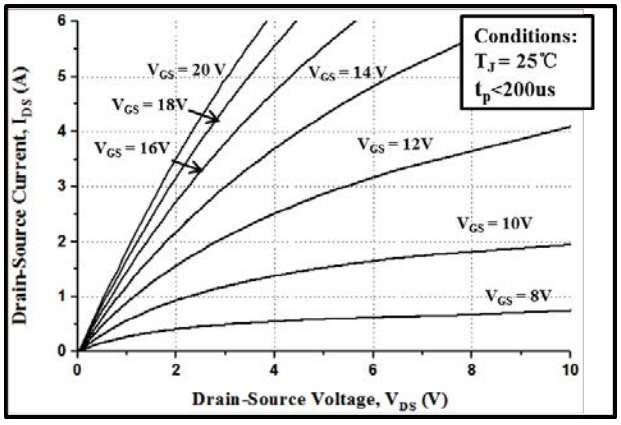



Figure 2. Output Characteristics $T_J$= 25℃

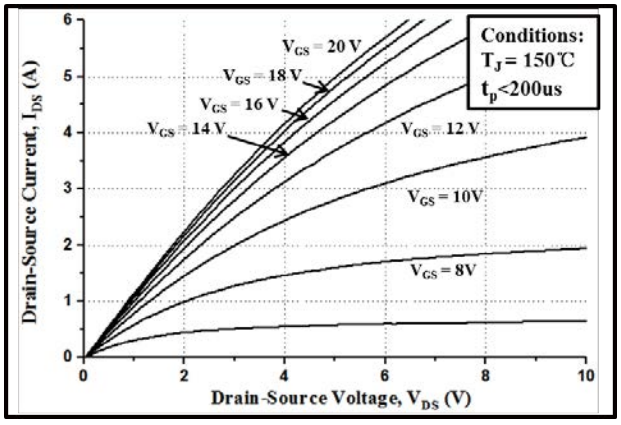



Figure 3. Output Characteristics $T_J$=150℃

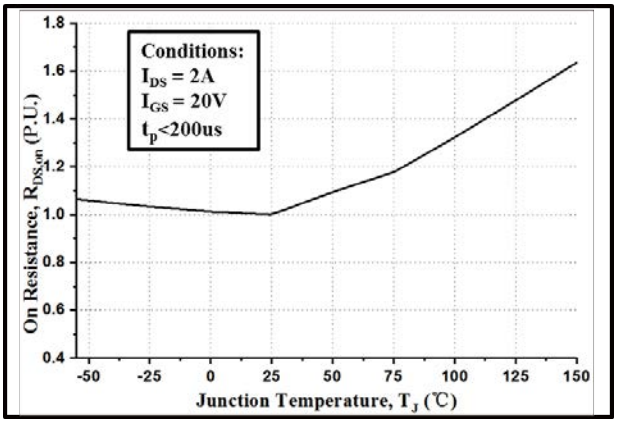



Figure 4. Normalized On-Resistance vs. Temperature

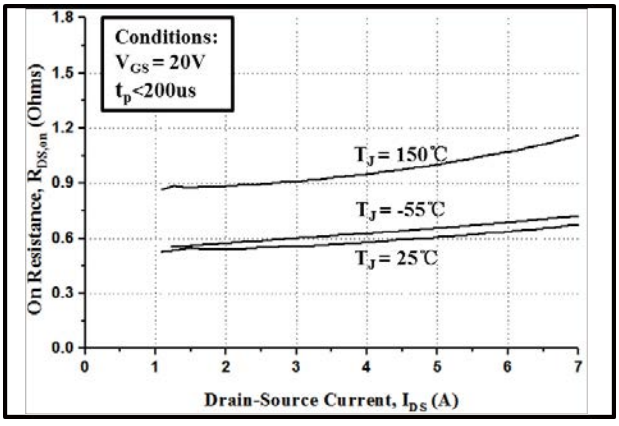



Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

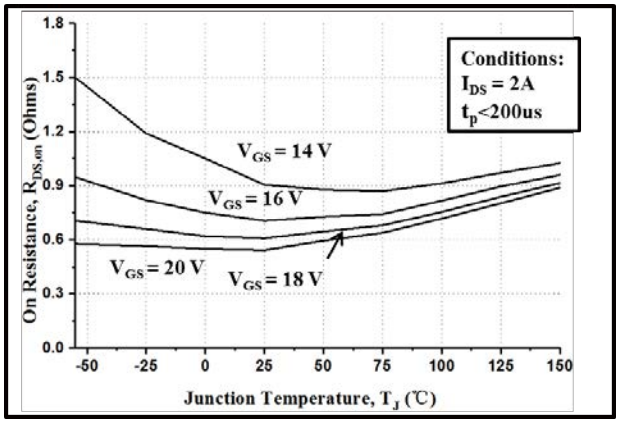



Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

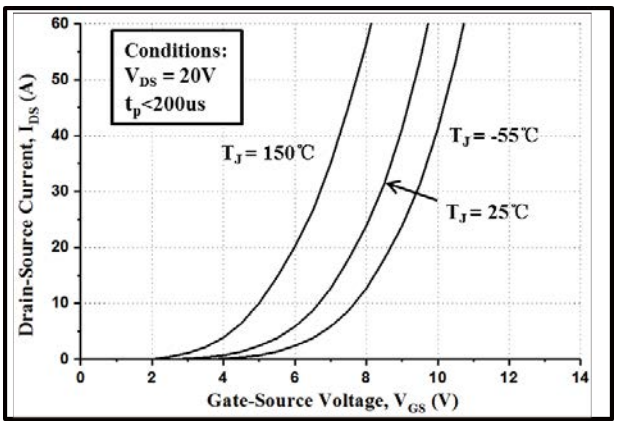



**Figure 7. Transfer Characteristic for Various Junction Temperatures**

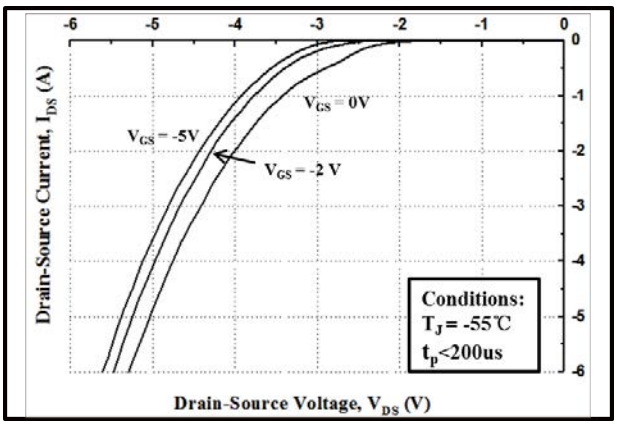



**Figure 8. Body Diode Characteristic at -55℃**

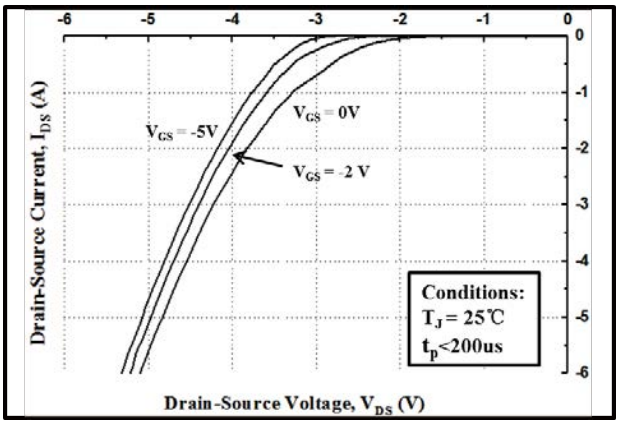



**Figure 9. Body Diode Characteristics at 25℃**

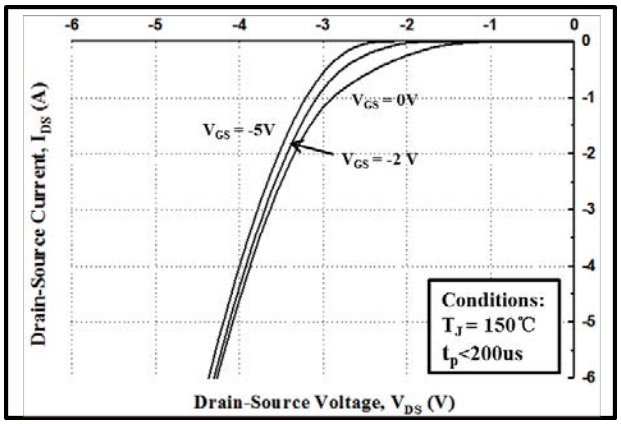



**Figure 10. Body Diode Characteristics at 150℃**

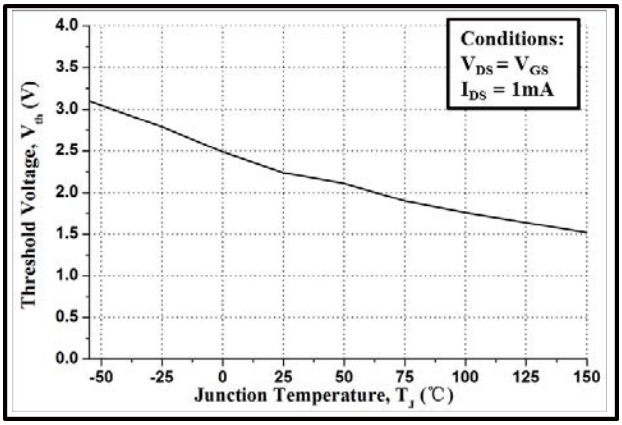



**Figure 11. Threshold Voltage vs. Temperature**

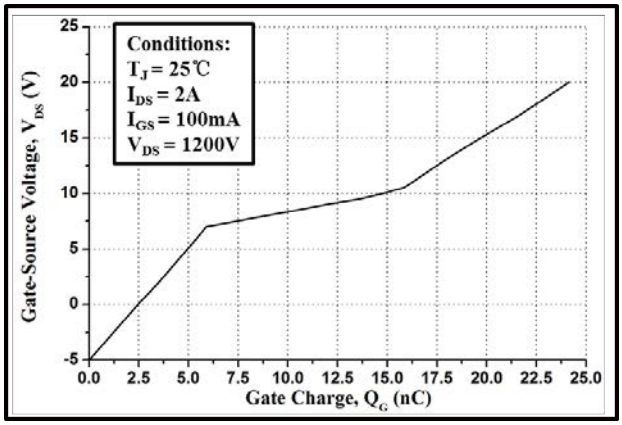



**Figure 12. Gate Charge Characteristic**

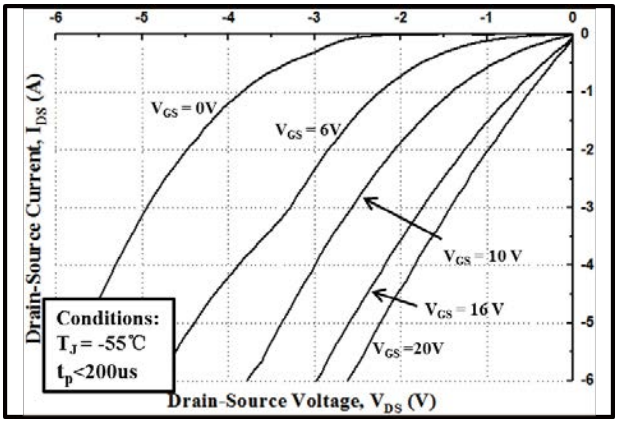



**Figure 13. 3rd Quadrant Characteristics at -55℃**

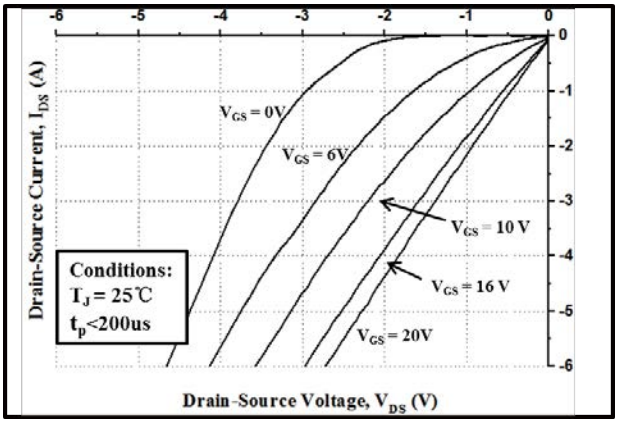



**Figure 14. 3rd Quadrant Characteristics at 25℃**

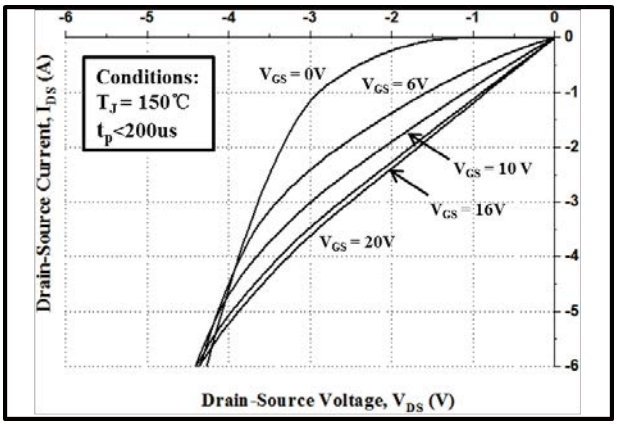



**Figure 15. 3rd Quadrant Characteristics at 150℃**

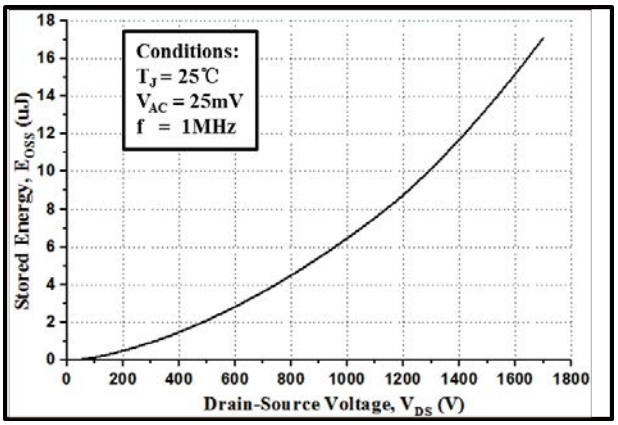



**Figure 16. Output Capacitor Stored Energy**

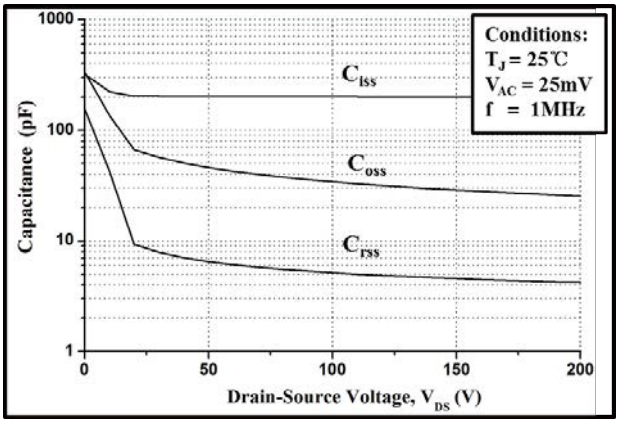



**Figure 17. Capactances vs. Drain-Source Voltage (0 - 200V)**

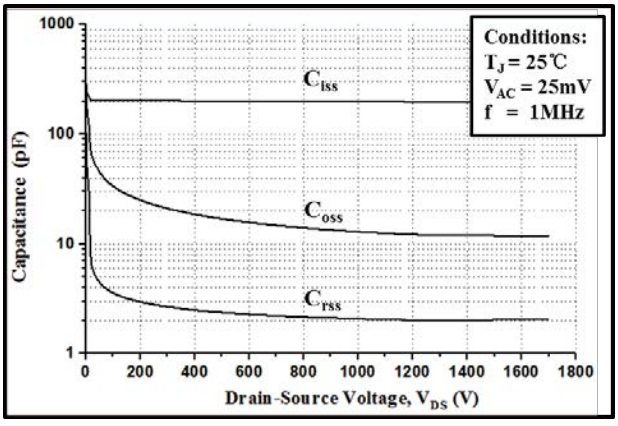



**Figure 18. Capactances vs. Drain-Source Voltage (0 - 1700V)**

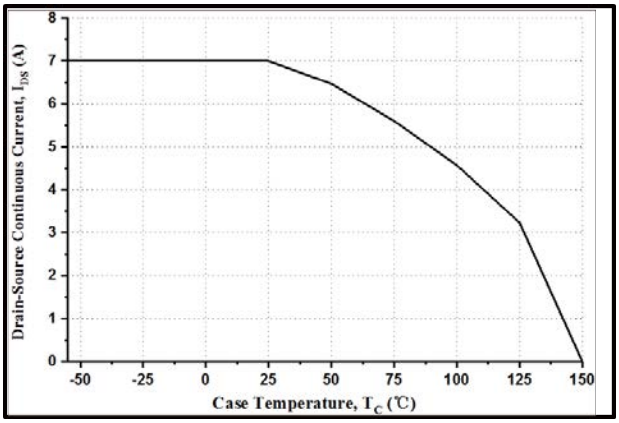



**Figure 19. Continuous Drain Current Derating vs. Case Temperature**

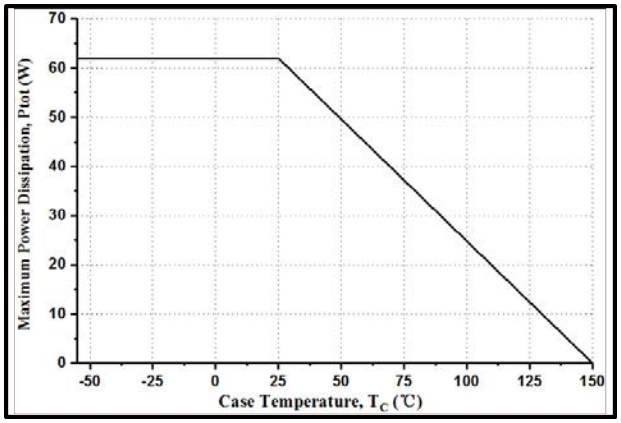



**Figure 20. Maximum Power Dissipation Derating vs. Case Temperature**

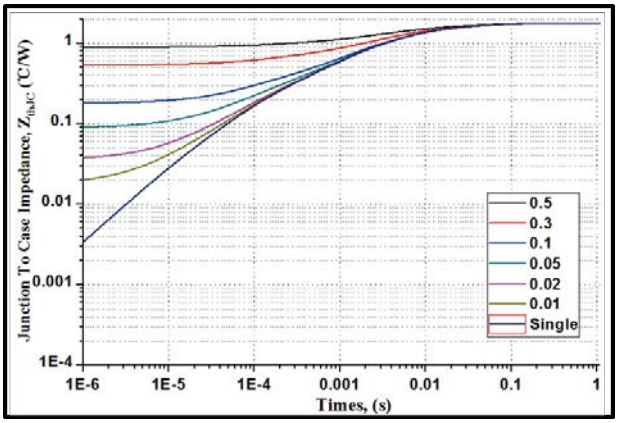



**Figure 21. Transient Thermal Impedance (Junction - Case)**

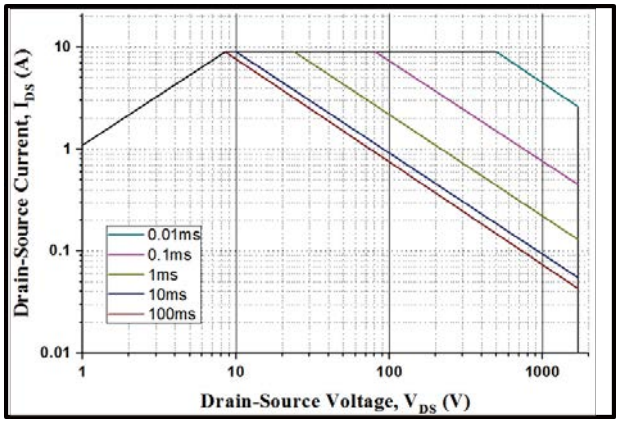
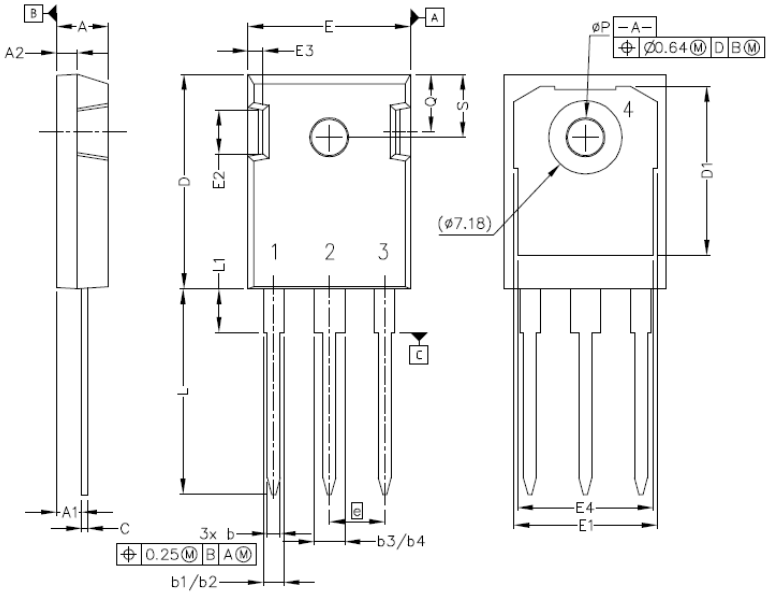



**Figure22. Safe Operating Area**

## Package Dimensions

Package TO-247



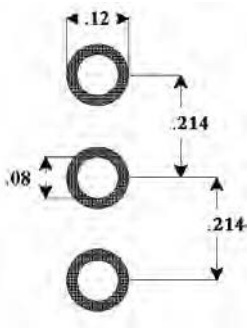


Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

| POS | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | .190 | .205 | 4.83 | 5.21 |
| A1 | .090 | .100 | 2.29 | 2.54 |
| A2 | .075 | .085 | 1.91 | 2.16 |
| b | .042 | .052 | 1.07 | 1.33 |
| b1 | .075 | .095 | 1.91 | 2.41 |
| b2 | .075 | .085 | 1.91 | 2.16 |
| b3 | .113 | .133 | 2.87 | 3.38 |
| b4 | .113 | .123 | 2.87 | 3.13 |
| c | .022 | .027 | 0.55 | 0.68 |
| D | .819 | .831 | 20.80 | 21.10 |
| D1 | .640 | .695 | 16.25 | 17.65 |
| D2 | .037 | .049 | 0.95 | 1.25 |
| E | .620 | .635 | 15.75 | 16.13 |
| E1 | .516 | .557 | 13.10 | 14.15 |
| E2 | .145 | .201 | 3.68 | 5.10 |
| E3 | .039 | .075 | 1.00 | 1.90 |
| E4 | .487 | .529 | 12.38 | 13.43 |
| e | .214 BSC | | 5.44 BSC | |
| N | 3 | | 3 | |
| L | .780 | .800 | 19.81 | 20.32 |
| L1 | .161 | .173 | 4.10 | 4.40 |
| ØP | .138 | .144 | 3.51 | 3.65 |
| Q | .216 | .236 | 5.49 | 6.00 |
| S | .238 | .248 | 6.04 | 6.30 |
| T | 9° | 11° | 9° | 11° |
| U | 9° | 11° | 9° | 11° |
| V | 2° | 8° | 2° | 8° |
| W | 2° | 8° | 2° | 8° |

### Recommended Solder Pad Layout

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