

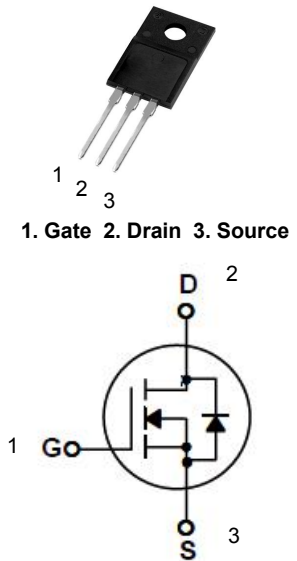
TO-220F Package

Features

- $R_{DS(on)}$ (Typical 0.7Ω)@ $V_{GS}=10V$
- Improved dv/dt Capability, High Ruggedness
- 100% Avalanche Tested
- Maximum Junction Temperature Range ($150^{\circ}C$)

General Description

This Power MOSFET is produced by WPM using its own advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.



Absolute Maximum Ratings

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter	Rating	Unit
Common Ratings (T _J =25°C Unless Otherwise Noted)			
V _{GS}	Gate-Source Voltage	±30	V
V _{(BR)DSS}	Drain-Source Breakdown Voltage	650	V
T _J	Maximum Junction Temperature	-50 to 150	°C
T _{STG}	Storage Temperature Range	-50 to 150	°C
I _S	Diode Continuous Forward Current	10	A
Mounted on Large Heat Sink (T _J =25°C Unless Otherwise Noted)			
I _{DM}	Pulse Drain Current Tested (Silicon Limit) (Note		40A
I _D	Continuous Drain current@V _{GS} =10V	T _C =25°C	10A
P _D	Maximum Power Dissipation		39W
E _{AS}	Sing Pulsed Avalanche Energy (Note2)		900mJ
R _{θJC}	Thermal Resistance Junction-to-Case		3.2°C/W
R _{θJA}	Thermal Resistance Junction-to-Ambient		65°C/W

Note :

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $IL=18mH, I_{AS}=10A, V_{DD}=50V, R_G=25\Omega, T_J=25^{\circ}C$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	650	--	--	V
I _{DSS}	Zero Gate Voltage Drain current(Tc=25°C)	VDS=650V,VGS=0V	--	--	1	μA
I _{GSS}	Gate-Body Leakage Current	VGS=±30V,VDS=0V	--		±100	nA
V _{GS(TH)}	Gate Threshold Voltage	VDS=VGS,ID=250μA	2	3	4	V
R _{DS(ON)}	Drain-Source On-State Resistance note A	VGS=10V,ID=5A	--	0.7	1.0	Ω
Dynamic Electrical Characteristics @ T _J = 25°C (unless otherwise stated) ^{note B}						
C _{iss}	Input Capacitance	VDS=25V,VGS=0V, f=1MHz	--	1120	--	pF
C _{oss}	Output Capacitance		--	130	--	pF
C _{rss}	Reverse Transfer Capacitance		--	4.9	--	pF
Q _g	Total Gate Charge	VDS=520V,ID=10A VGS=10V	--	21	--	nC
Q _{gs}	Gate-Source Charge		--	7.5	--	nC
Q _{gd}	Gate-Drain Charge		--	6	--	nC
Switching Characteristics ^{note B}						
t _{d(on)}	Turn-on Delay Time	VDS=300V ID=10A RG=25Ω VGS=10V	--	38	--	nS
t _r	Turn-on Rise Time		--	70	--	nS
t _{d(off)}	Turn-Off Delay Time		--	53	--	nS
t _f	Turn-Off Fall Time		--	35	--	nS
Source- Drain Diode Characteristics@ T _J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	IS= 10 A,VGS=0V	--	0.85	1.4	V

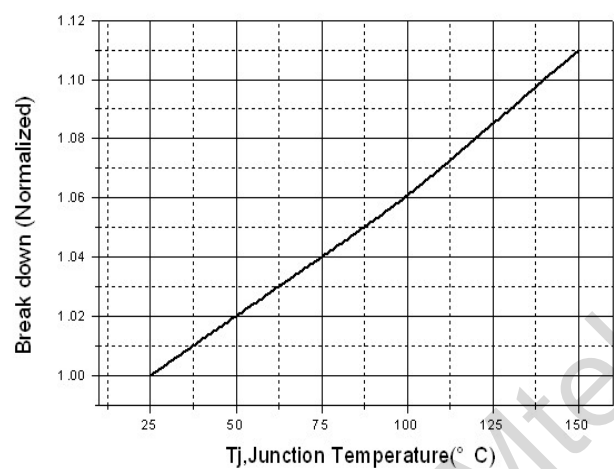
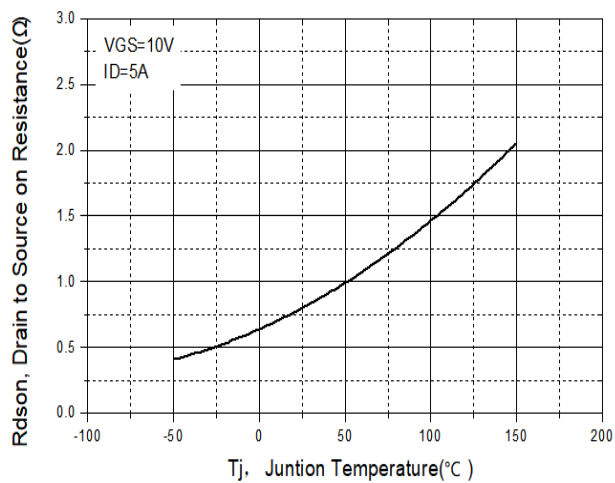
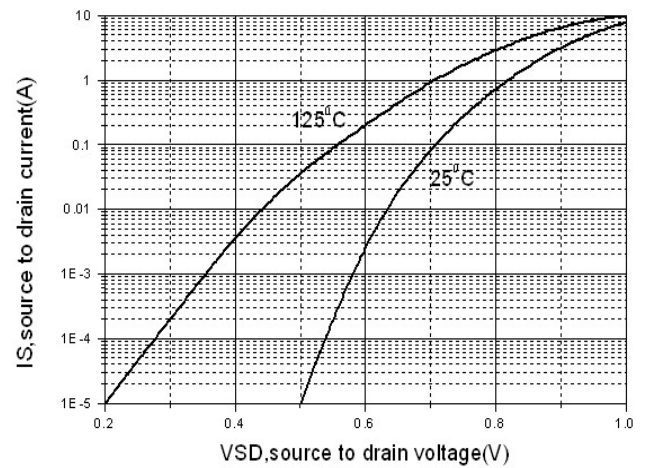
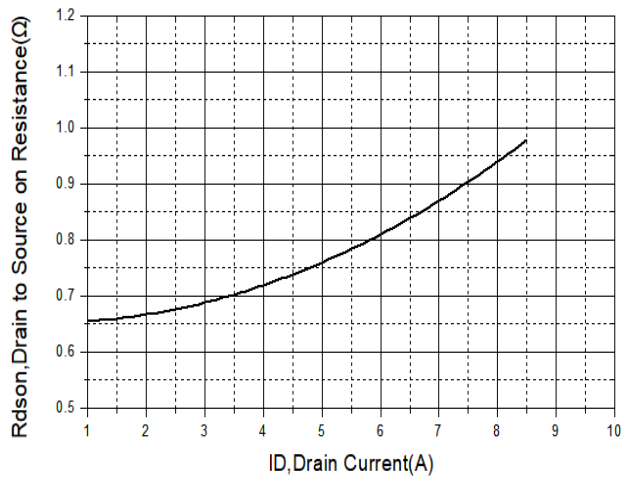
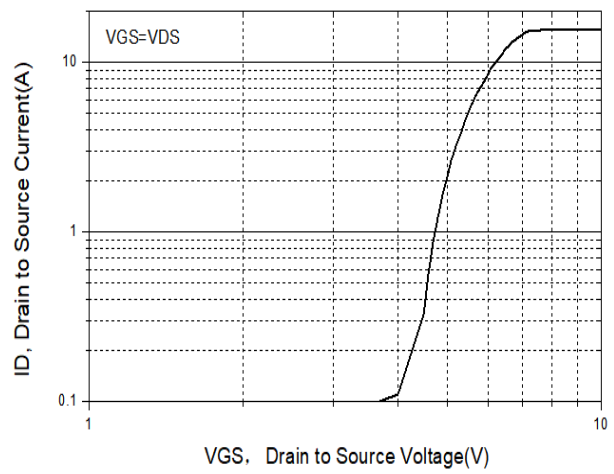
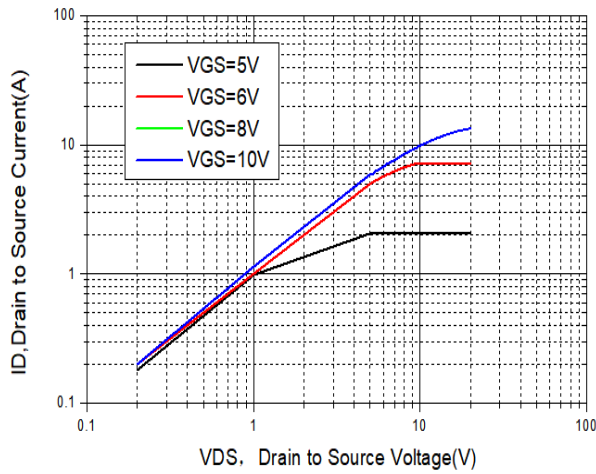
Note:

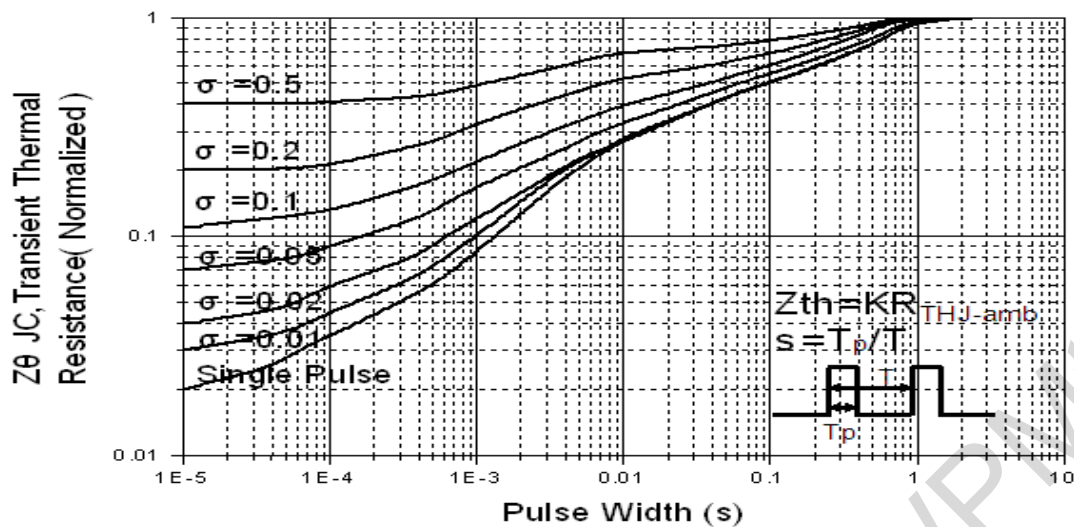
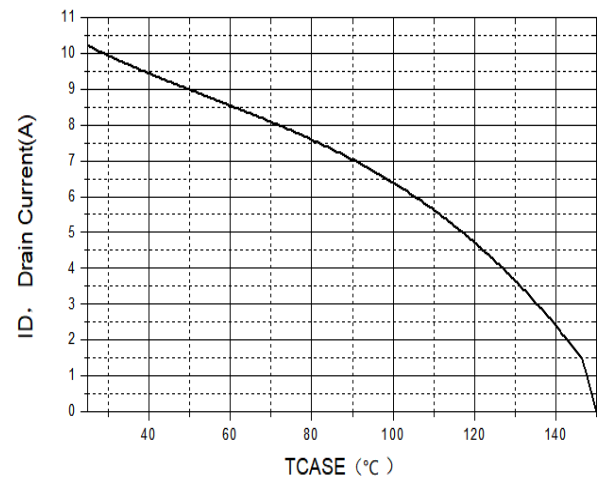
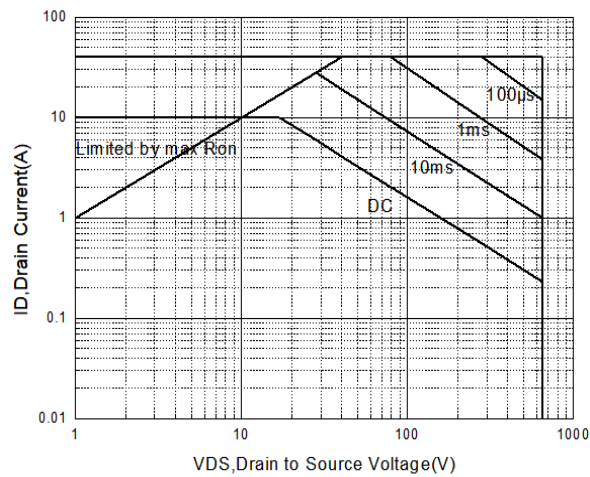
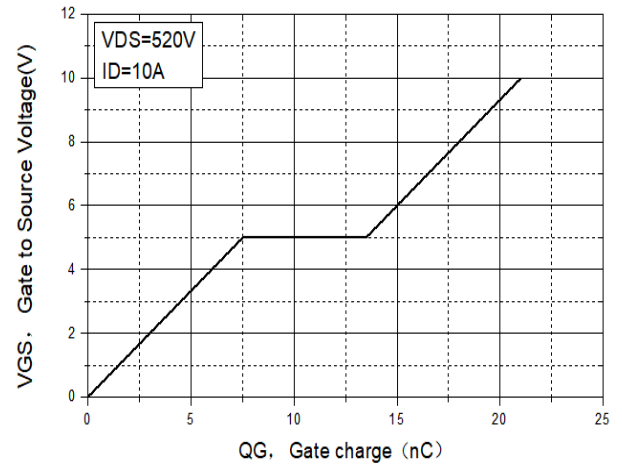
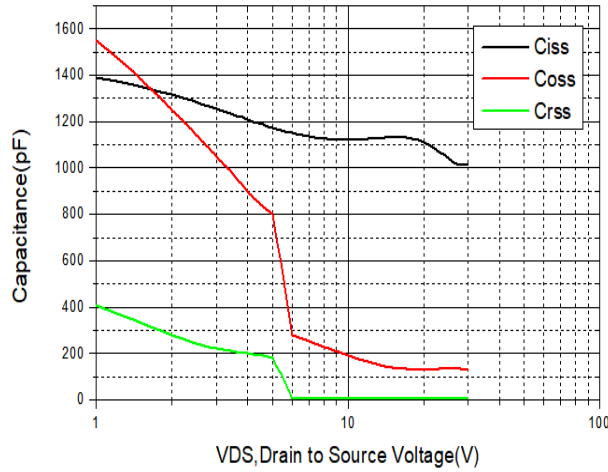
A: Pulse Test: pulse width ≤ 300 us, duty cycle ≤ 2%

B:Guranteed by design, not subject to production testing.

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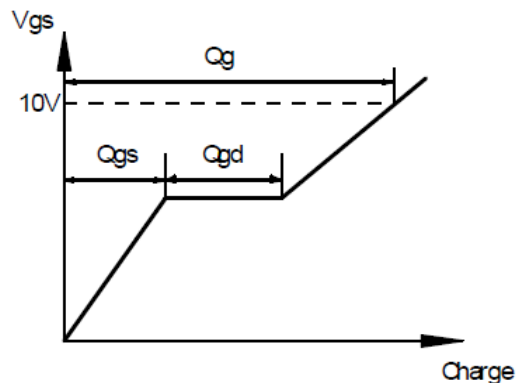
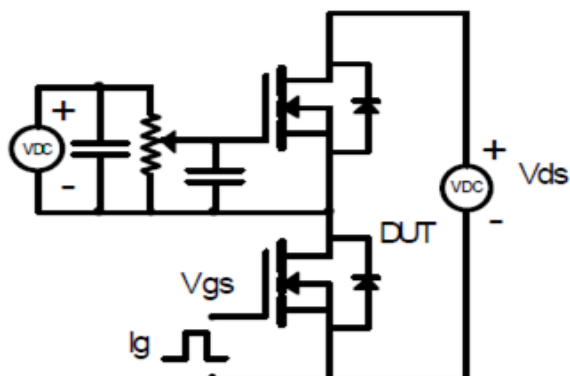
Typical characteristic curve:



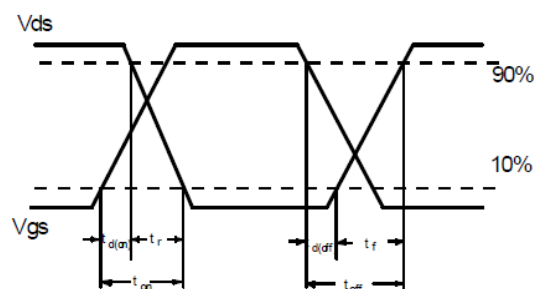
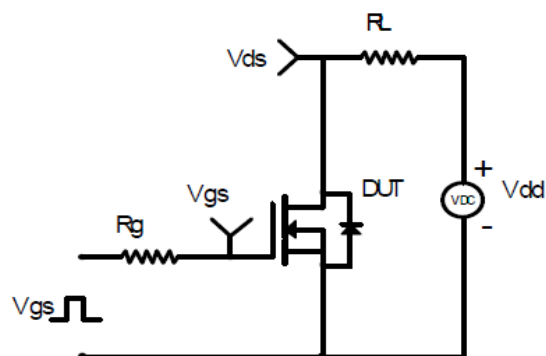


Test Circuit and Waveform

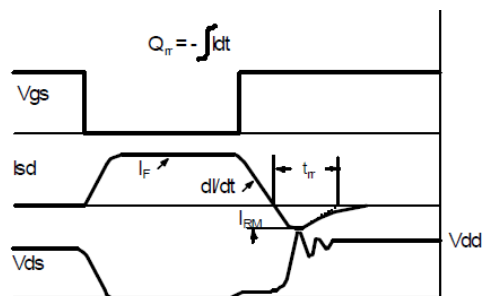
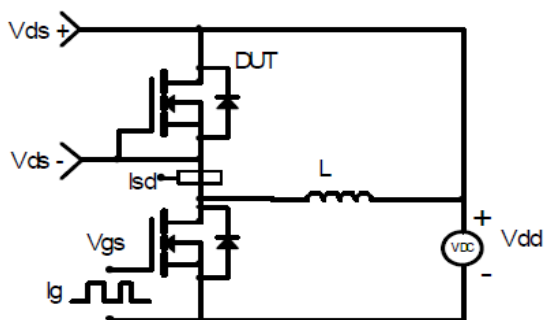
Gate Charge Test Circuit and Waveform



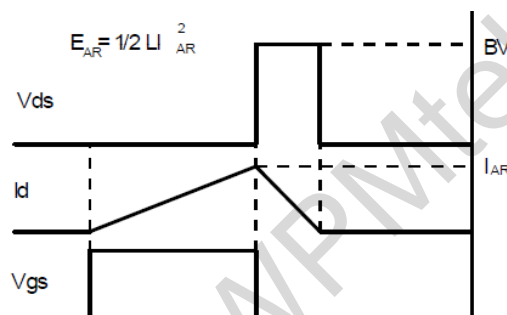
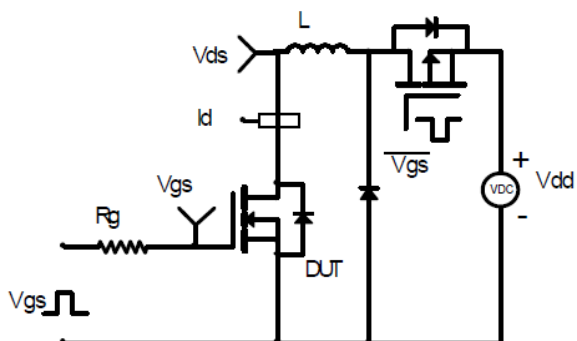
Switching time test circuit and waveform



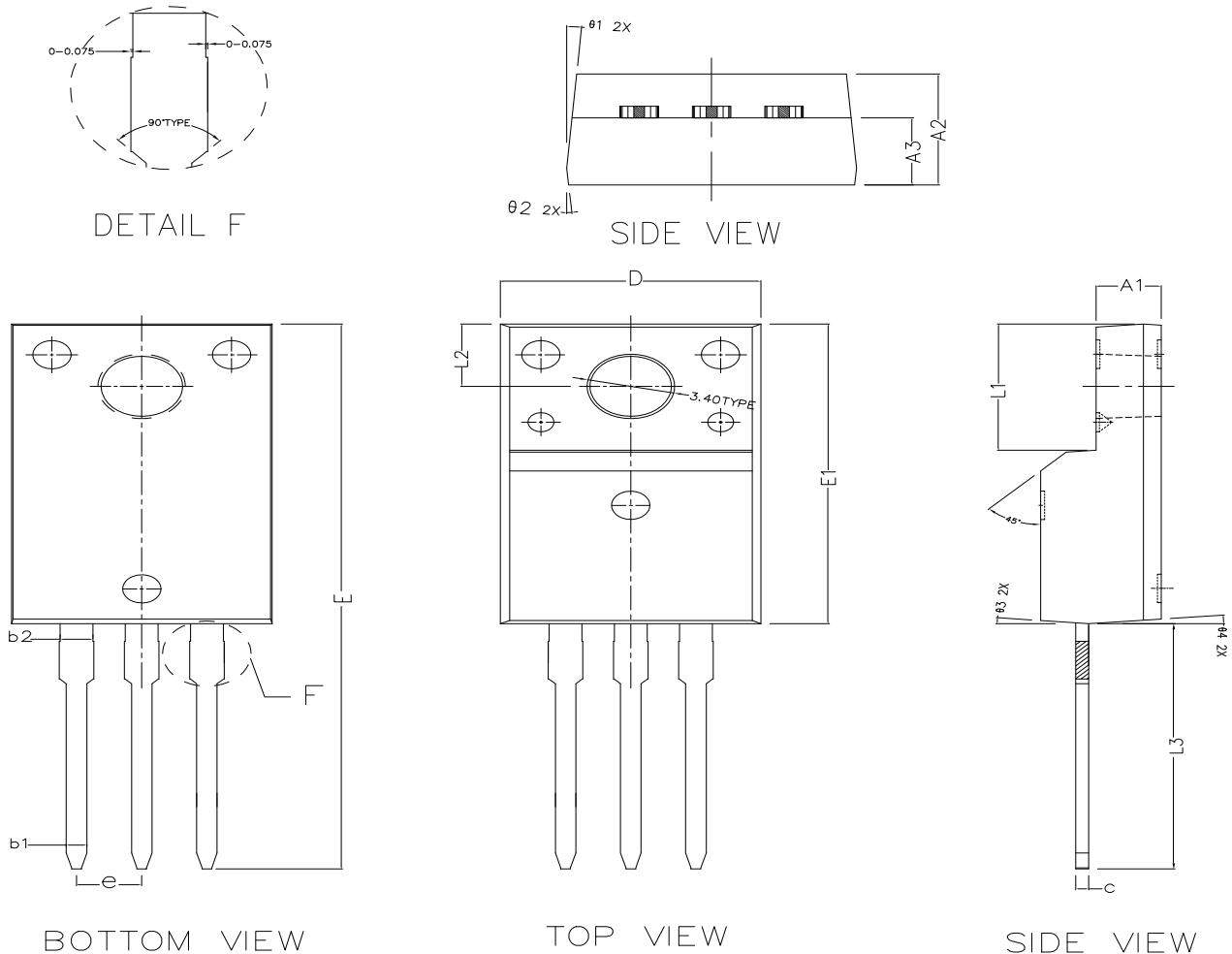
Reverse Recovery Test Circuit and Waveform



Avalanche Test Circuit and Waveform

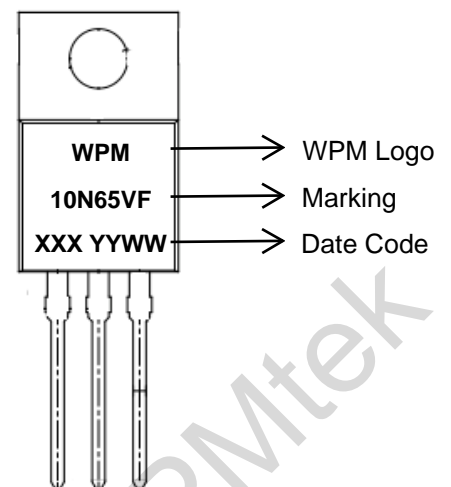


TO-220F Package Outline Dimensions (Units: mm)



COMMON DIMENSIONS (UNITS OF MEASURE IS mm)			
	MIN	NORMAL	MAX
A1	2.440	2.540	2.640
A2	4.600	4.700	4.800
A3	2.730	2.830	2.930
b1	0.750	0.800	0.850
b2	1.230	1.280	1.330
c	0.450	0.500	0.550
D	10.060	10.160	10.260
E	28.650	28.850	29.050
E1	15.770	15.870	15.970
e	2.54TYPE		
L1	6.68REF		
L2	3.30REF		
L3	12.830	12.980	13.130
θ1	5° TYPE		
θ2	5° TYPE		
θ3	5° TYPE		
θ4	5° TYPE		

Marking



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