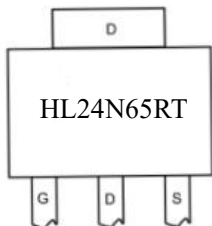
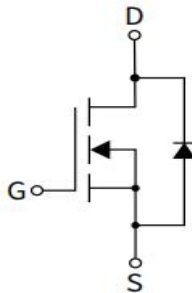


Features ➤ Much lower $R_{on} \cdot A$ performance for On-state efficiency ➤ Better efficiency due to very low FOM ➤ Qualified for industrial grade applications according to JEDEC ➤ Advanced trench gate super junction technology	<i>Bvdss</i>	<i>Rdson</i>	<i>ID</i>
	650V	110mΩ	24A
	Application ➤ Power factor correction (PFC) ➤ Switching power supply (SMPS) ➤ LED driver		

Package

Marking and pin assignment

TO-220 top view

Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
HL24N65RT	HL24N65RT	TO220	50

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current $V_{GS}@10V^{1,6}$	$I_D@T_C = 25^\circ\text{C}$	I_D	24	A
	$I_D@T_C = 100^\circ\text{C}$		12	A
Pulsed Drain Current ²		I_{DM}	96	A
Single Pulsed Avalanche Energy ³		EAS	300	mJ
Avalanche Current		I_{AS}	-	A
Total Power Dissipation ⁴	$T_C = 25^\circ\text{C}$	P_D	89	W
Operating Junction Temperature Range		T_J	-55 ~ 150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	67	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	1.4	$^\circ\text{C}/\text{W}$



Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL24N65RT	TO220	1	2	3	Tube

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	650	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	-	-	5	μA
		$V_{DS}=650V, V_{GS}=0V, T_J=150^{\circ}\text{C}$	-	220	-	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	3.2	-	4.6	V
Static Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=16A$	-	110	140	m Ω
Forward Transconductance	g_{fs}	$V_{DS}=20V, I_D=16A$	-	16.5	-	S
Gate Resistance	R_g	$V_{GS}=0V, V_{DS}=0V, f=1\text{MHz}$	-	10	-	Ω
Total Gate Charge	Q_g	$V_{DS}=480V, V_{GS}=10V, I_D=16A$	-	46	-	nC
Gate Source Charge	Q_{gs}		-	14	-	
Gate Drain Charge	Q_{gd}		-	24	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DD}=400V, I_D=16A, R_G=27\Omega$	-	60	-	ns
Rise Time	T_r		-	61	-	
Turn-Off Delay Time	$T_{d(off)}$		-	140	-	
Fall Time	T_f		-	31	-	
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$	-	1595	-	pF
Output Capacitance	C_{oss}		-	90	-	
Reverse Transfer Capacitance	C_{rss}		-	1.5	-	
Diode Continuous Current ^{1,4}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	24	A
Diode Forward Voltage ²	V_{SD}	$I_S=16A, V_{GS}=0V, T_J=25^{\circ}\text{C}$	0.7	0.86	1.1	V
Reverse Recovery Time	t_{rr}	$I_F=16A, di/dt=100A/\mu s, T_J=25^{\circ}\text{C}$	-	120	-	ns
Reverse Recovery Charge	Q_{rr}		-	0.63	-	nC

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $T_J=25^{\circ}\text{C}, V_{DD}=200V, V_{GS}=10V, L=60\text{mH}$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

Fig 1. Output Characteristics ($T_J=25^\circ\text{C}$)

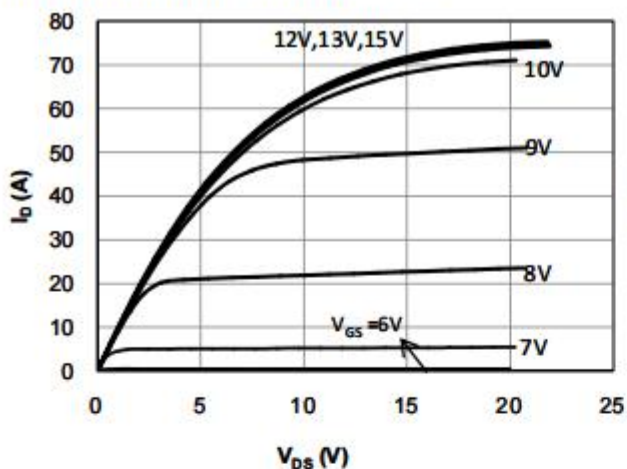


Fig 2. Output Characteristics ($T_J=150^\circ\text{C}$)

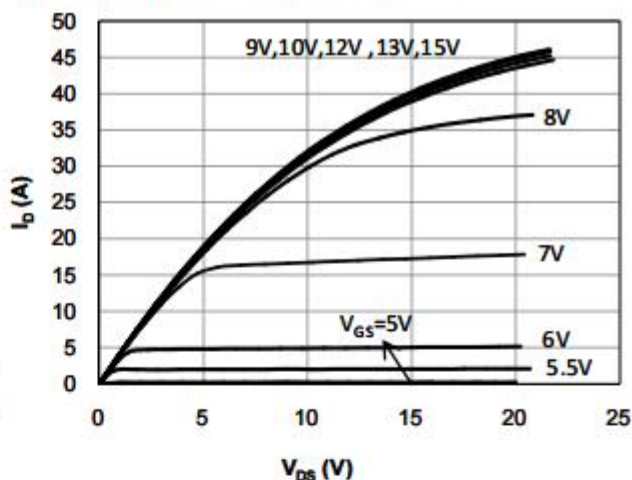


Fig 3: Transfer Characteristics

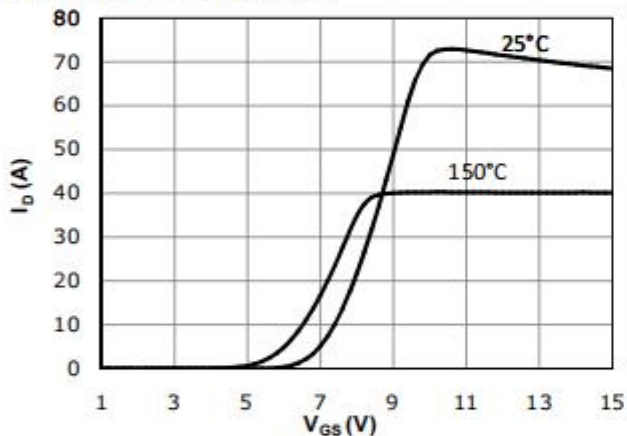


Fig 4: V_{TH} vs. T_J Temperature Characteristics

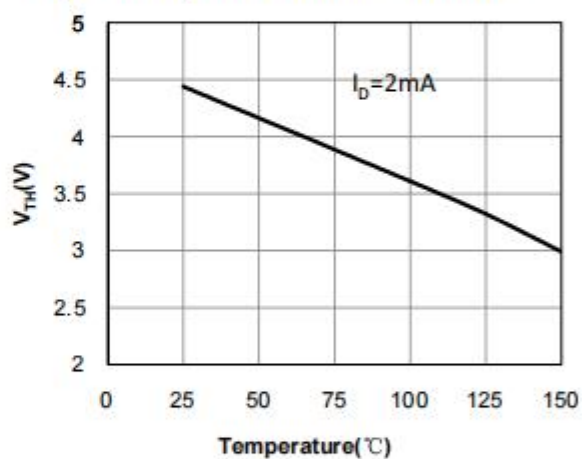


Fig 5: $R_{DS(on)}$ vs. I_{DS} Characteristics ($T_J=25^\circ\text{C}$)

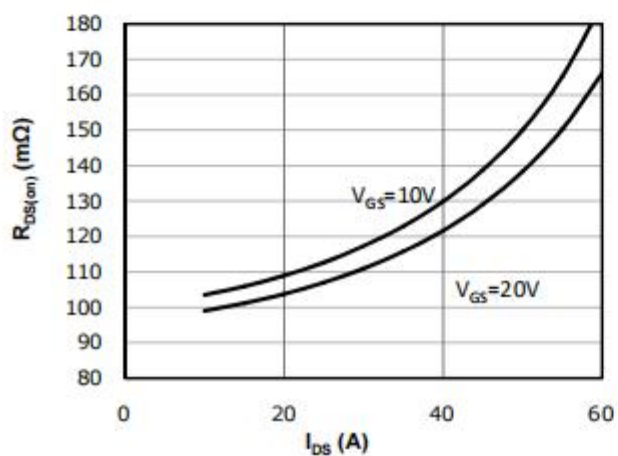


Fig 6: $R_{DS(on)}$ vs. Temperature

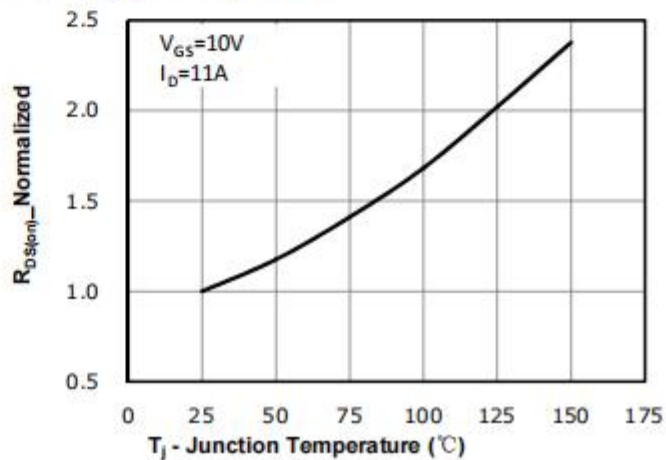


Fig 7: BV_{DSS} vs. Temperature

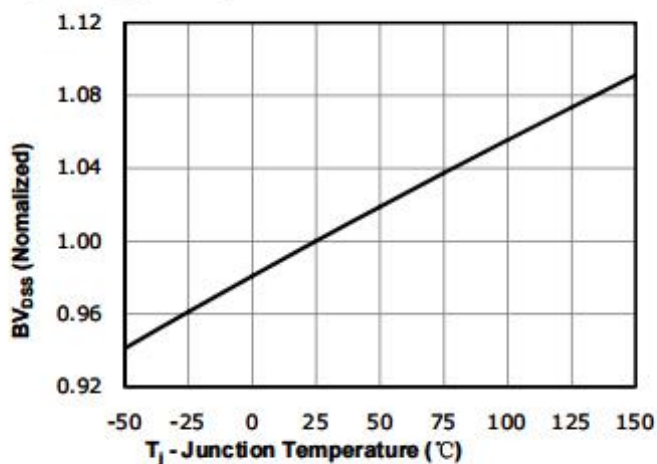


Fig 8: $R_{DS(on)}$ vs. Gate Voltage

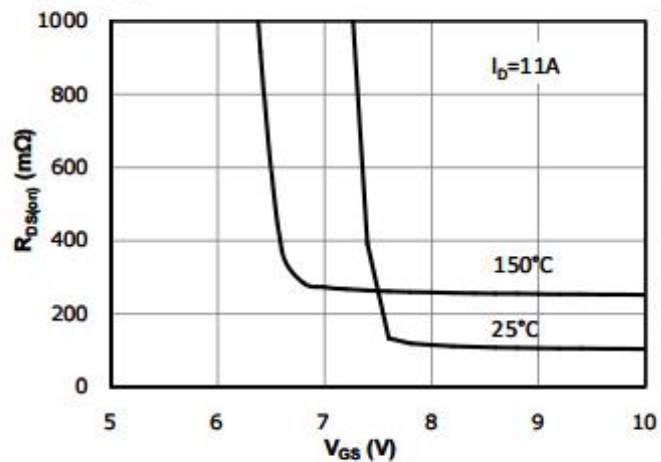


Fig 9: Body-diode Forward Characteristics

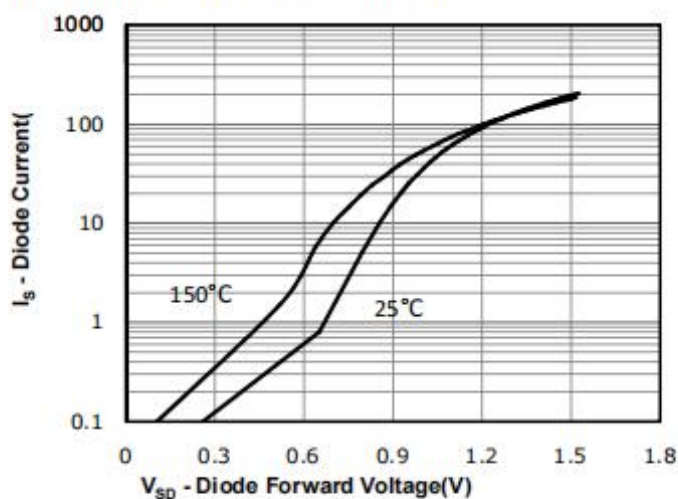


Fig 10: Gate Charge Characteristics

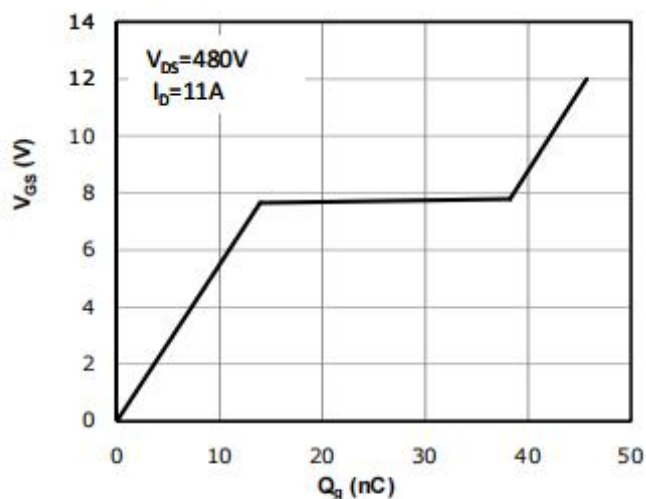


Fig 11: Capacitance Characteristics

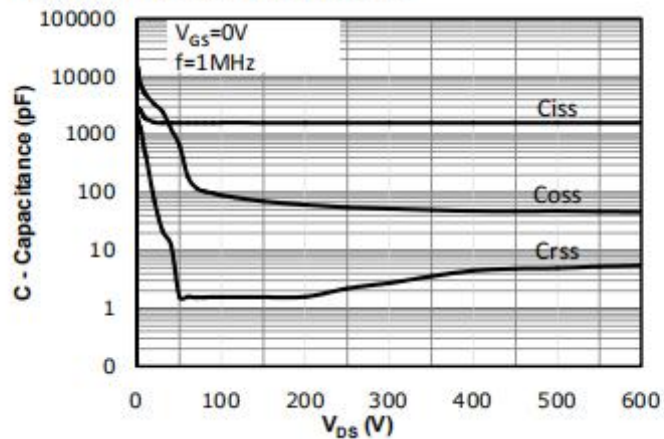


Fig 12: Safe Operating Area

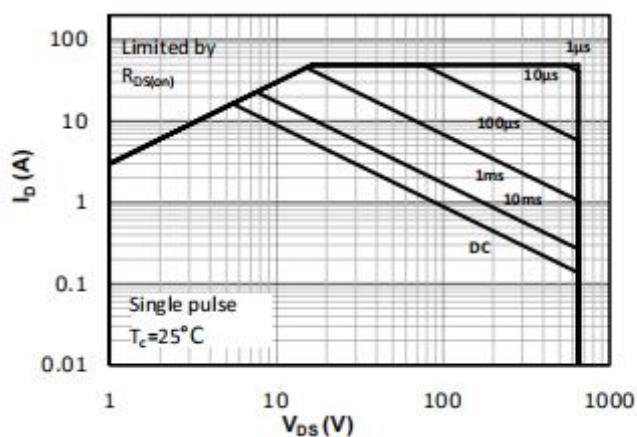
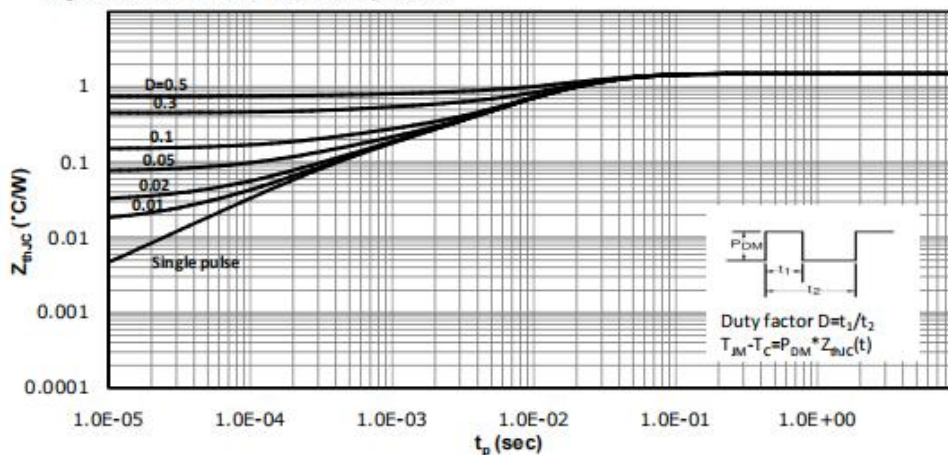
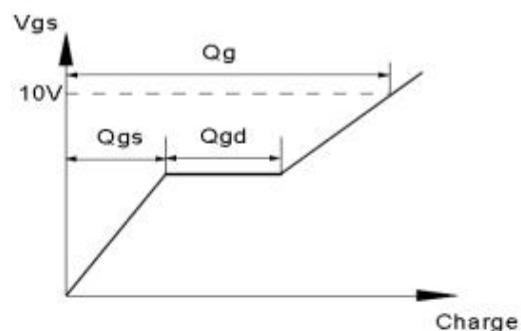
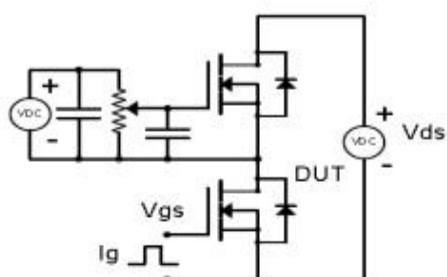


Fig 13: Max. Transient Thermal Impedance

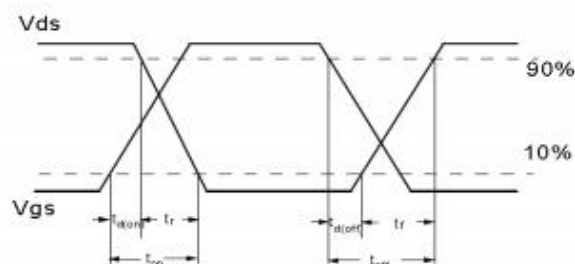
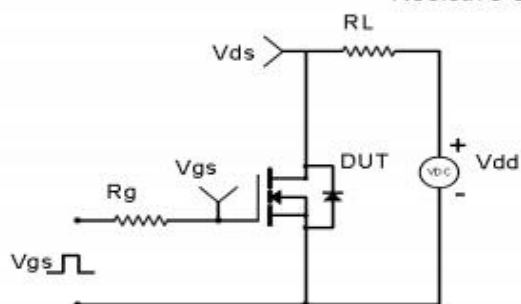


Test Circuit and Waveform

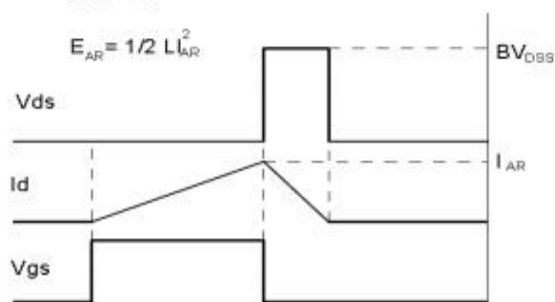
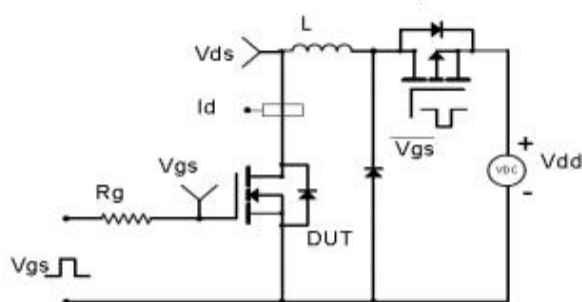
Gate Charge Test Circuit & Waveform



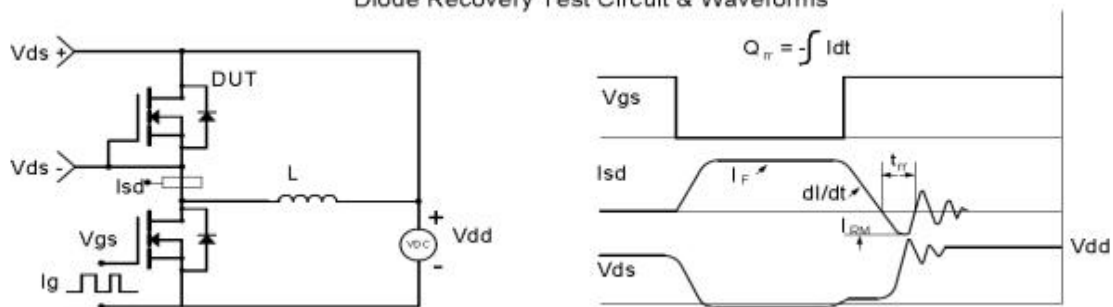
Resistive Switching Test Circuit & Waveforms



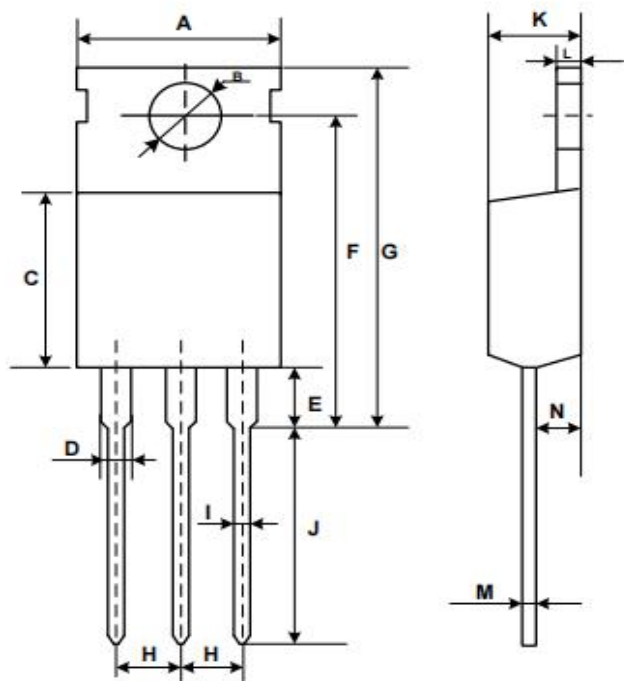
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Dimensions TO-220



SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60



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