Features

- Super Junction technology
- Much lower Ron*A performance for On-state efficiency High density cell design for low
- Better efficiency due to very low FOM
- Qualified for industrial grade applications according to JEDEC

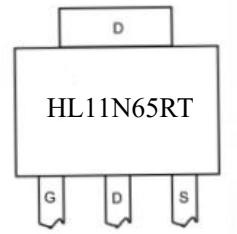
Bvdss	Rdson	ID
650V	360mΩ	11A

Application

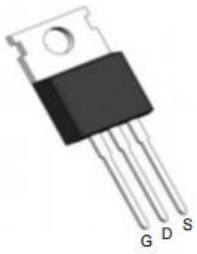
RoHS

- Power factor correction (PFC)
- Switching power supply (SMPS)
- LED driver

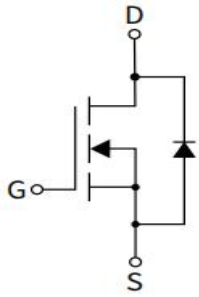
Package



Marking and pin assignment



TO-220 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
HL11N65RT	HL11N65RT	TO220	50

Absolute Maximum Ratings (T_C=25℃unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{Gs}	±30	V
Continuous Drain Current V_{GS}@10V[1,6]	I_D@T_C = 25℃	I_D	11	A
	I_D@T_C = 100℃	I_D	7	A
Pulsed Drain Current[2]		I_{DM}	44	A
Single Pulsed Avalanche Energy[3]		E_{As}	120	mJ
Avalanche Current		I_{AS}	11	A
Power Dissipation[4]	T_C = 25℃	P_D	29	W
Junction Temperature		T_J	-55~+150	℃
Storage Temperature		T_{STG}	-55~+150	℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient[1]	$R_{\theta JA}$	78	℃/W
Thermal Resistance Junction-Case[1]	$R_{\theta JC}$	4.3	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL11N65RT	TO220	1	2	3	Tube

Electrical Characteristics (T_J=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	650	-	-	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS}=10V, I_D=5.5A	-	360	450	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D=250uA	3.5	-	4.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V T_J=25°C	-	-	1	μA
		V_{DS}=650V,V_{GS}=0V T_J=100°C	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	-	-	±80	nA
Forward Transconductance	gfs	V_{DS}=20V,I_D=5.5A	-	12	-	S
Gate Resistance	R_g	V_{GS}=0V,V_{DS}=0V, f=1MHz	-	2	-	Ω
Total Gate Charge	Q_g	V_{DS}=480V,V_{GS}=10V, I_D=5.5A	-	22	-	nC
Gate Source Charge	Q_{gs}		-	5.3	-	
Gate Drain Charge	Q_{gd}		-	8.8	-	
Turn-On Delay Time	$T_{d(on)}$	V_{GS}=10V,V_{DD}= 400V I_D=5.5A,R_{GEN}=25Ω	-	20	-	ns
Rise Time	T_r		-	15	-	
Turn-Off Delay Time	$T_{d(off)}$		-	74	-	
Fall Time	T_f		-	43	-	
Input Capacitance	C_{iss}	V_{GS}=100V,V_{DS}=0V, f=1MHz	-	790	-	pF
Output Capacitance	C_{oss}		-	32	-	
Reverse Transfer Capacitance	C_{rss}		-	2	-	
Diode Continuous Current[1,4]	I_S	V_G=V_D=0V,Force Current	-	-	11	A
Diode Forward Voltage[2]	V_{SD}	I_S=5.5A,V_{GS}=0V, T_J=25°C	-	-	1.2	V
Reverse Recovery Time	t_{rr}	IF=5.5A,di/dt=100A/μs, T_J=25°C	-	218	-	ns
Reverse Recovery Charge	Q_{rr}		-	2.35	-	nC

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is T_J = 25°C,V_{DD}=200V,V_{GS}=10V,L=60mH

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

Fig 1. Output Characteristics (Tj=25℃)

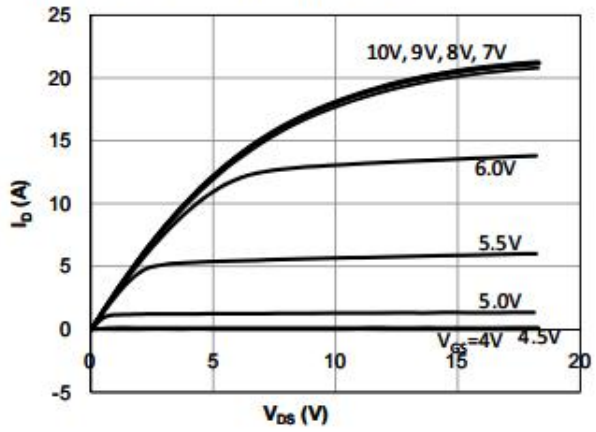


Fig 2. Output Characteristics (Tj=150℃)

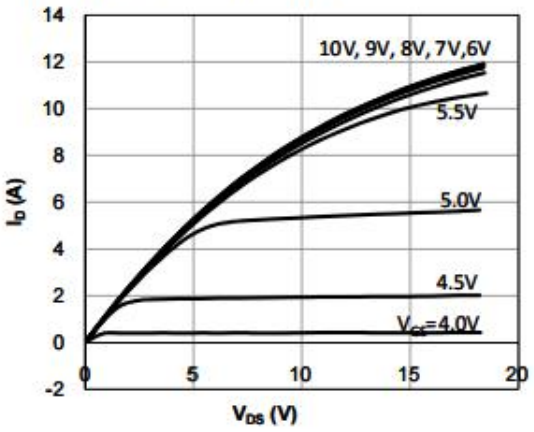


Fig 3: Transfer Characteristics

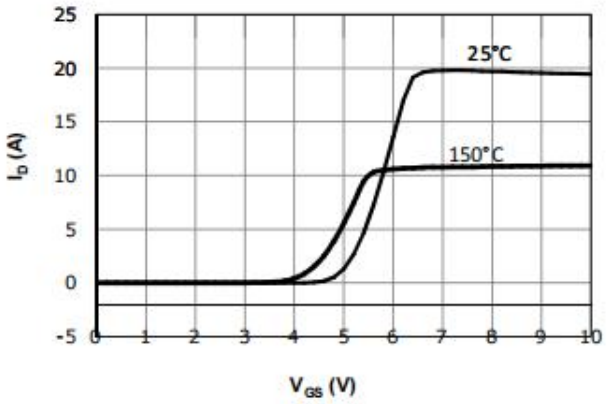


Fig 4: V_{TH} Vs Tj Temperature Characteristics

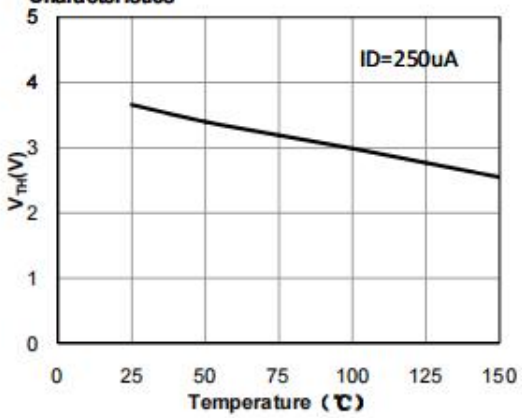


Fig 5: Rdson Vs Ids Characteristics(Tc=25℃)

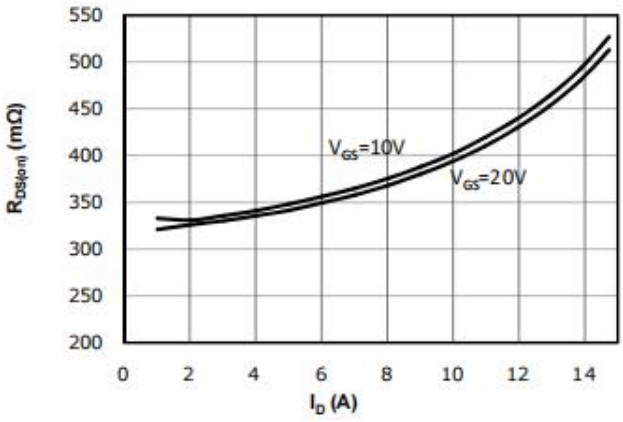


Fig 6: Rds(on) vs. Temperature

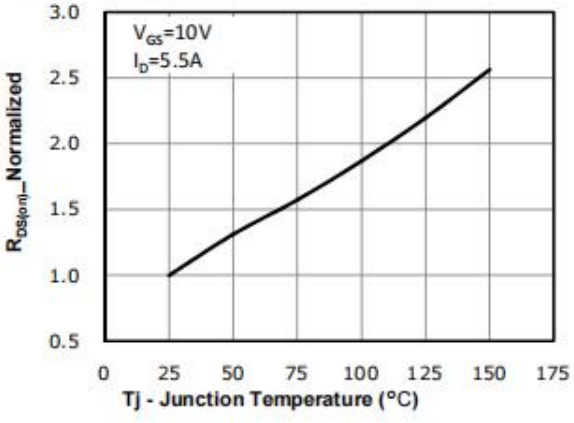


Fig 7: BVDSS vs. Temperature

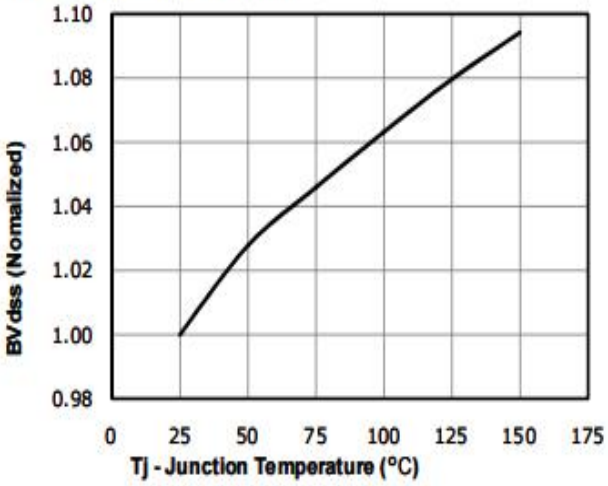


Fig 8: Rds(on) vs Gate Voltage

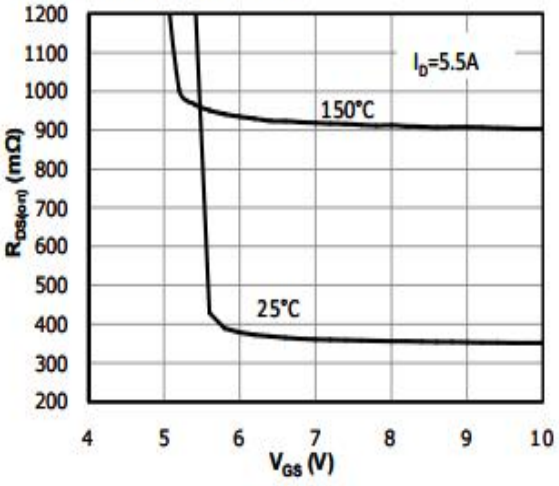


Fig 9: Body-diode Forward Characteristics

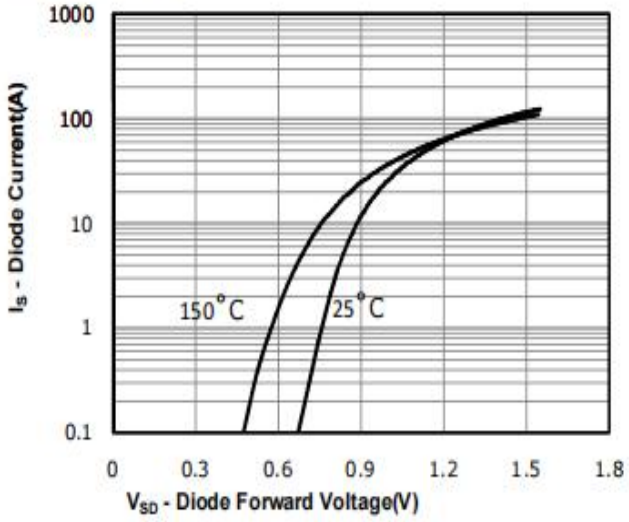


Fig 10: Gate Charge Characteristics

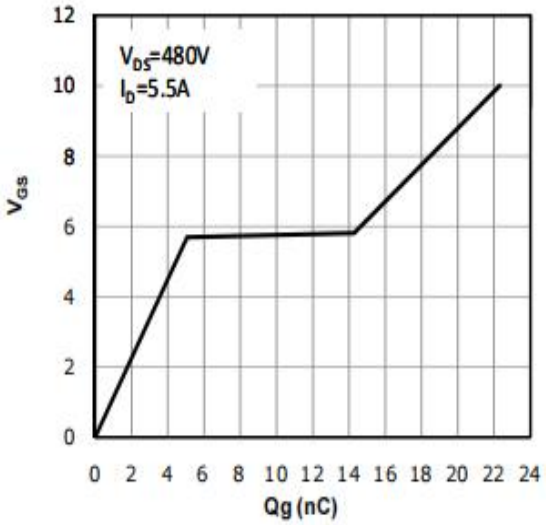


Fig 11: Capacitance Characteristics

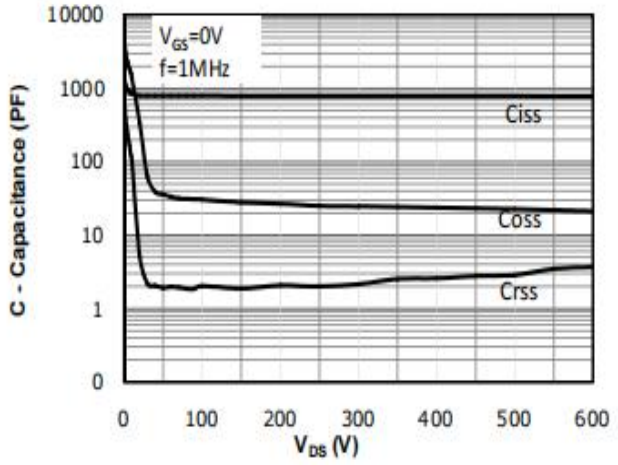


Fig 12: Safe Operating Area

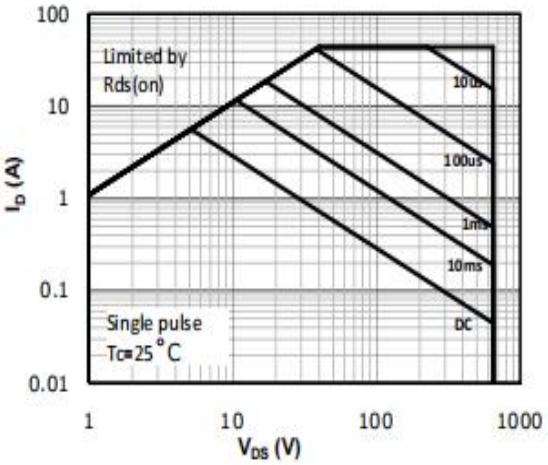
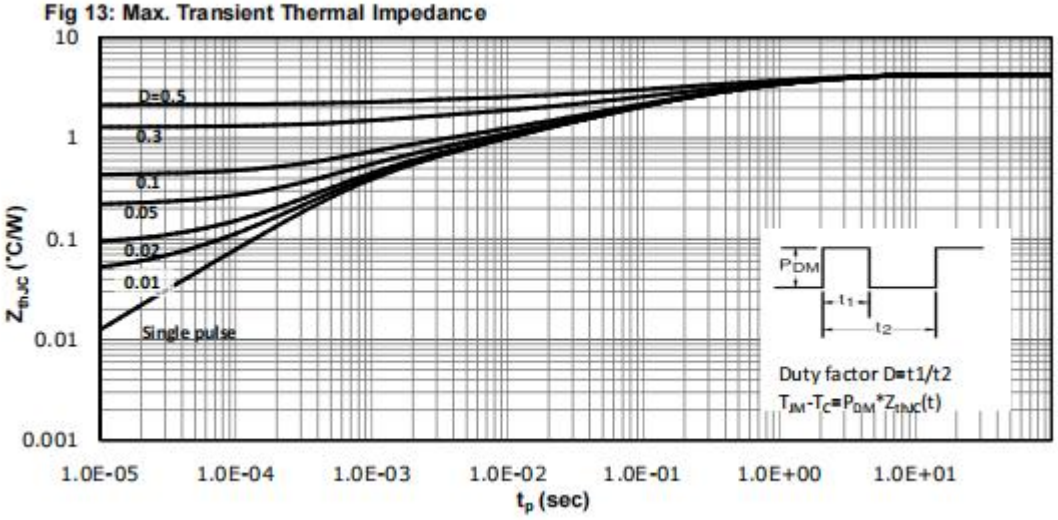
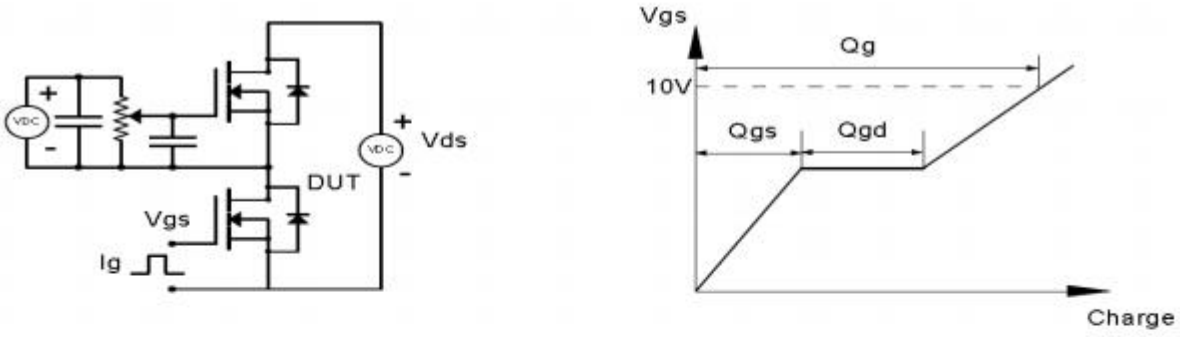


Fig 13: Max. Transient Thermal Impedance

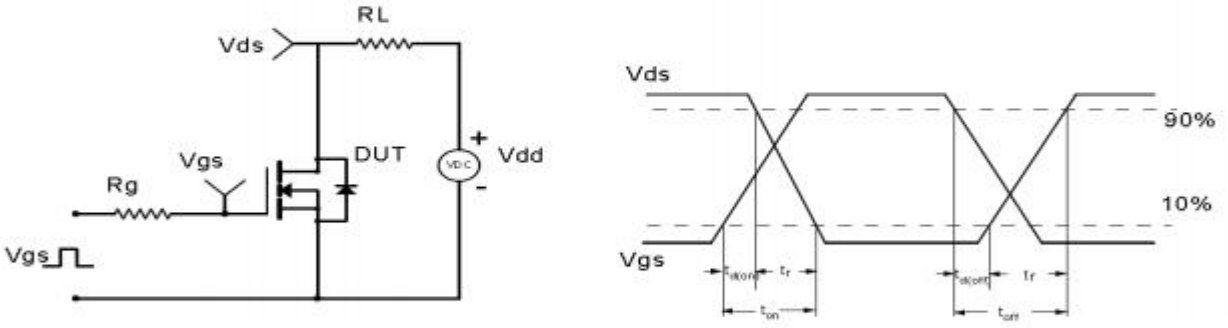


Test Circuit and Waveform

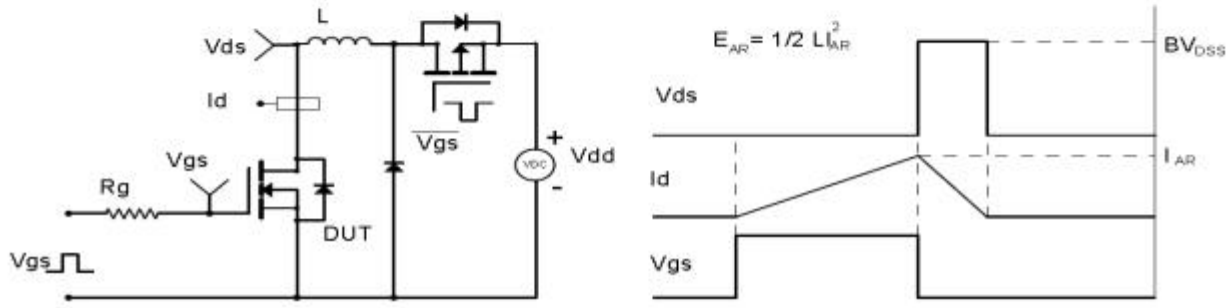
Gate Charge Test Circuit & Waveform



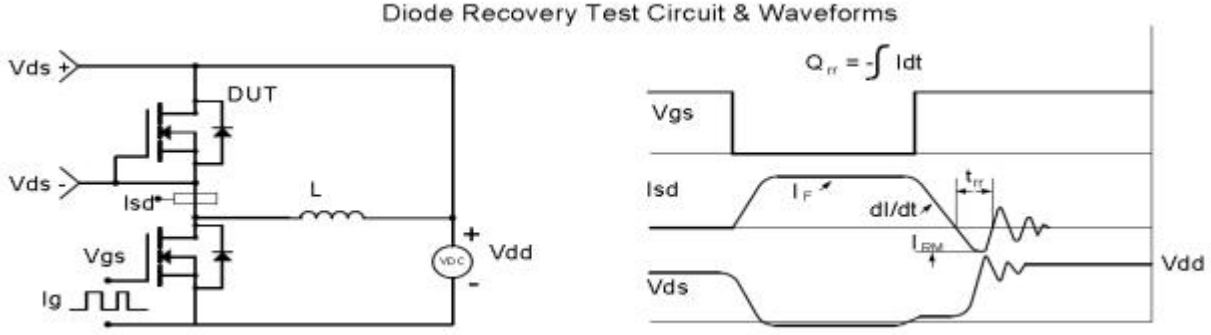
Resistive Switching Test Circuit & Waveforms



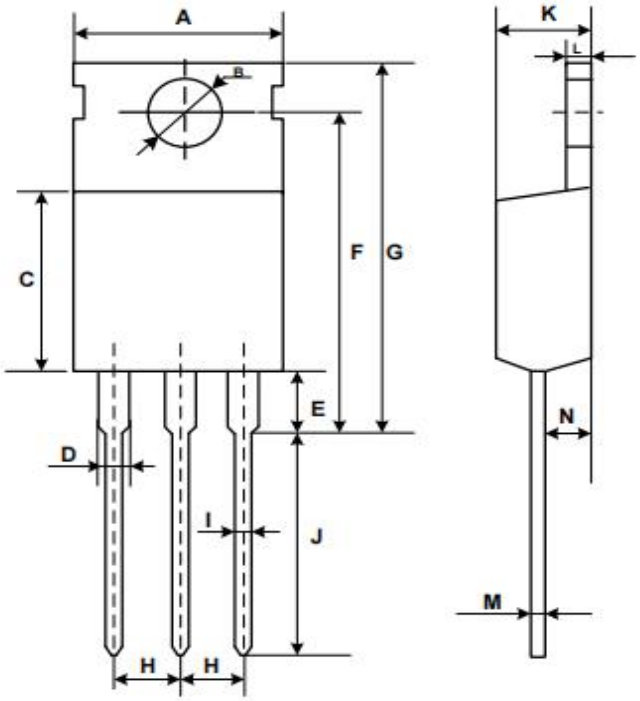
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Dimensions TO-220



SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60

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