DESCRIPTION

The PCF8563T/5,518-CN is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption. A programmable clock output, interrupt output, and voltage-low detector are also provided. All addresses and data are transferred serially via a two-line bidirectional I^2C-bus. Maximum bus speed is 400 Kbit/s. The register address is incremented automatically after each written or read data byte.

FEATURES

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768KHz quartz crystal
- Low backup current: typical 0.25μA(V_{DD} = 3.0V@25℃)
- 400KHz two-wire I^2C-bus interface (V_{DD} = 1.8V to 5.5V)
- Programmable clock output for peripheral devices : 32.768KHz, 1.024KHz, 32Hz, and 1Hz
- Integrated oscillator capacitor
- Alarm and timer functions
- Internal Power-On Reset (POR)
- Open-drain interrupt pin
- I^2C-bus slave address: read 0A3h and write 0A2h
- PACKAGE: SOP8

APPLICATIONS

- Mobile telephones
- Portable instruments
- Electronic metering
- Battery powered products

BLOCK DIAGRAM

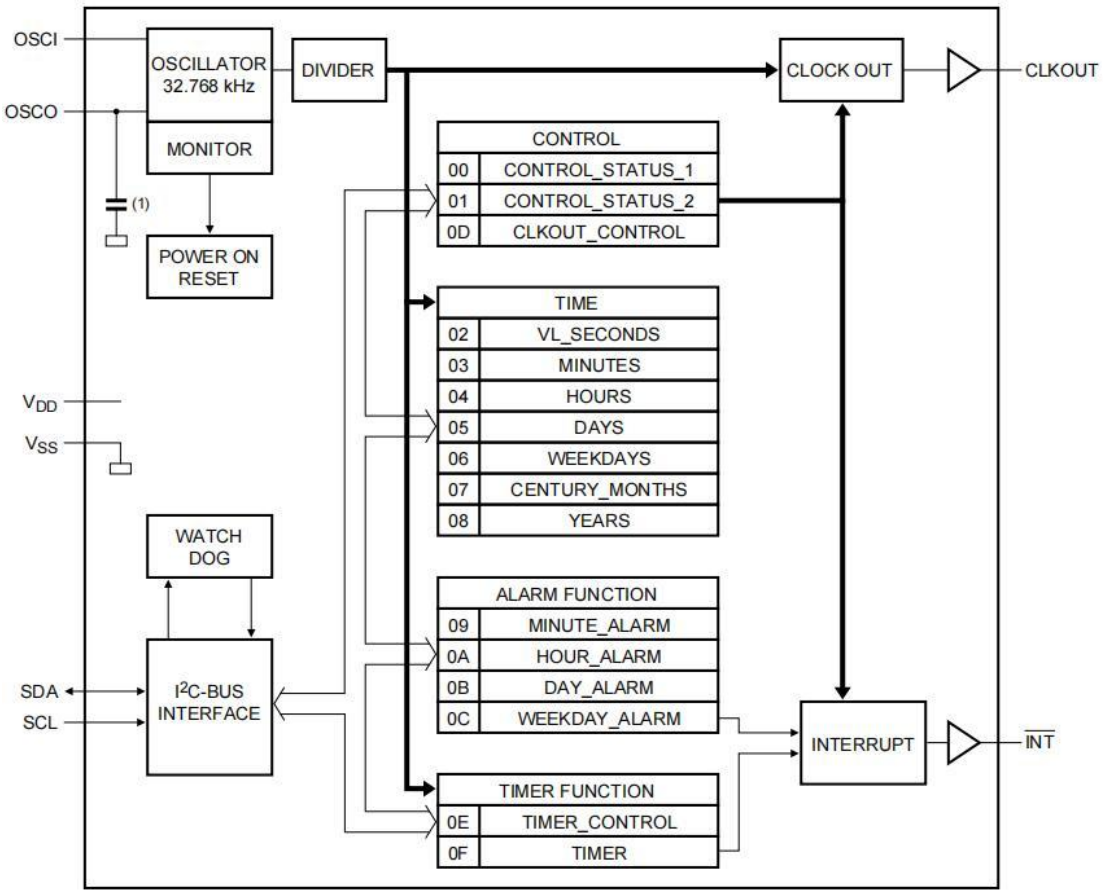


Fig 1. Block diagram

INTERNAL CIRCUITRY

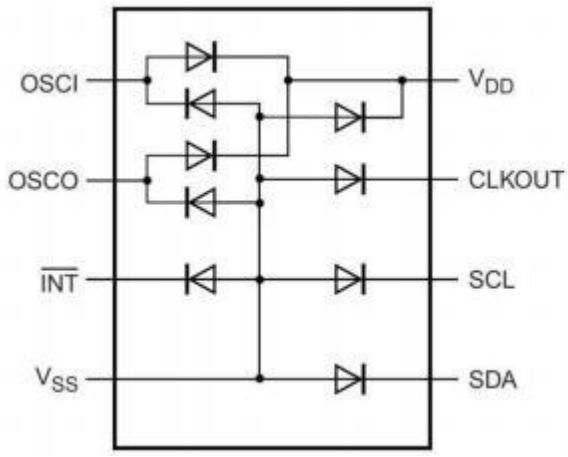


Fig 2. Device diode protection diagram

PIN DESCRIPTION

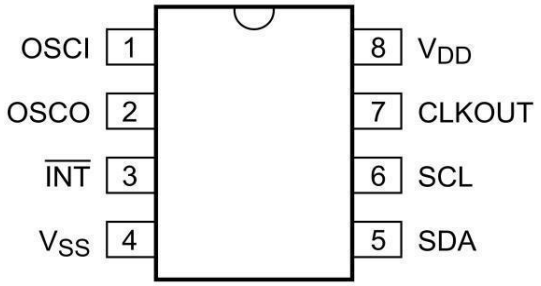


Fig 3. Pin configuration

PIN	NAME	FUNCTION
1	OSCI	Oscillator input
2	OSCO	Oscillator output
3	$\overline{INT}$	Interrupt output (open-drain; active LOW)
4	V_{SS}	Ground
5	SDA	Serial data input and output
6	SCL	Serial clock input
7	CLKOUT	Clock output, open-drain
8	V_{DD}	Supply voltage

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply Voltage	-	-0.5	+6.5	V
I_{DD}	Supply Current	-	-50	+50	mA
V_I	Input Voltage	on pins SCL, SDA, and OSCI	-0.5	+6.5	V
V_O	Output Voltage	on pins CLKOUT and $\overline{INT}$	-0.5	+6.5	V
I_I	Input Current	at any input	-10	+10	mA
I_O	Output Current	at any output	-10	+10	mA
P_D	Total Power Dissipation	-	-	300	mW
T_{amb}	Ambient Temperature	operating device	-20	85	℃
T_{stg}	Storage Temperature	-	-65	150	℃
V_{ESD}	Electrostatic Discharge Voltage	HBM	-4000	+4000	V

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

STATIC CHARACTERISTICS

(V_{DD} = 1.8V to 5.5V, V_{SS} = 0V, T_{amb} = -20 to +85℃, Fosc = 32.768KHz, quartz R_S = 40KΩ, C_L = 8pF, unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLIES							
V_{DD}	Supply Voltage	T_{amb} = +25℃	Interface inactive	1.0	-	5.5	V
		f_{SCL} = 400KHz	interface active	1.8	-	5.5	V
	Data Retention Voltage	T_{amb} = +25℃	clock data integrity	V_{LOW}	-	5.5	V
I_{DD} 1	Supply Current 1	f_{SCL} = 400KHz	interface active V_{DD}=5V	-	-	800	μA
		f_{SCL} = 100KHz		-	-	200	μA
I_{DD} 2	Supply Current 2 (CLKOUT Disabled)	interface inactive f_{SCL} = 0Hz T_{amb} = +25℃	V_{DD}=5V	-	275	550	nA
			V_{DD}=3V	-	250	500	nA
			V_{DD}=2V	-	225	450	nA
		interface inactive f_{SCL} = 0Hz T_{amb} = -20 to +85℃	V_{DD}=5V	-	500	750	nA
			V_{DD}=3V	-	400	650	nA
			V_{DD}=2V	-	400	600	nA
I_{DD} 3	Supply Current 3 (CLKOUT Enabled@32K)	interface inactive f_{SCL} = 0Hz, T_{amb} = 25℃	V_{DD}=5V	-	825	1600	nA
			V_{DD}=3V	-	550	1000	nA
			V_{DD}=2V	-	425	800	nA
		interface inactive f_{SCL} = 0Hz, T_{amb} = -20 to +85℃	V_{DD}=5V	-	950	1700	nA
			V_{DD}=3V	-	650	1100	nA
			V_{DD}=2V	-	500	900	nA
INPUTS							
V_{IL}	LOW-level Input Voltage	-		V_{SS}	-	0.3V_{DD}	V
V_{IH}	HIGH-level Input Voltage	-		0.7V_{DD}	-	V_{DD}	V
I_{LI}	Input Leakage Current	V_I=V_{DD} 或 V_{SS}		-1	0	+1	μA
C_I	Input Capacitance	-		-	-	7	pF
OUTPUTS							
I_{OL}	LOW-level Output Current	output sink current; V_{DD}=5V, V_{OL}=0.4V	on pins SDA	3	-	-	mA
			on pins $\overline{INT}$	1	-	-	mA
			on pins CLKOUT	1	-	-	mA
I_{LO}	Output Leakage Current	V_O=V_{DD} 或 V_{SS}		-1	0	+1	μA
VOLTAGE DETECTOR							
V_{LOW}	Low Voltage	TA= 25℃, sets bit VL		-	1.0	1.2	V

(1) For reliable oscillator start-up at power-up: $V_{DD(min)power-up}$ = $V_{DD(min)}$ + 0.3 V.

(2) Timer source clock = 1⁄60Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.

DYNAMIC CHARACTERISTICS

(V_{DD} = 1.8V to 5.5V, V_{SS} = 0V, T_{amb} = -20 to +85℃, Fosc = 32.768KHz, quartz R_S =40KΩ, C_L = 8pF, unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
C_{OSCO}	Capacitance on Pin OSCO	-	15	25	35	pF
Δf_{OSC}	Relative Cscillator Frequency Variation	ΔV_{DD}=200mV,T_{amb}=+25℃	-	0.2	-	ppm
QUARTZ CRYSTAL PARAMETERS （FOSC=32.768KHz）						
R_S	Series Resistance	-	-	-	40	KΩ
C_L	Load Capacitance	parallel	-	10	-	pF
C_T	Trimmer Capacitance	external, on pin OSCI	5	-	25	pF
CLKOUT OUTPUT						
δ_{CLKOUT}	Duty Cycle on Pin CLKOUT	-	-(1)	50	-	%
I²C-bus timing characteristics (2)						
f_{SCL}	SCL Clock Frequency	-	-(3)	-	400	KHz
$T_{HD;STA}$	Hold Time (respect) START Condition	-	0.6	-	-	μs
$T_{SU;STA}$	Set-up Time for a Repeated START Condition	-	0.6	-	-	μs
T_{LOW}	LOW Period of the SCL Clock	-	1.3	-	-	μs
T_{HIGH}	HIGH Period of the SCL Clock	-	0.6	-	-	μs
T_R	Rise Time of both SDA and SCL Signals	-	-	-	0.3	μs
T_F	Fall Time of both SDA and SCL Signals	-	-	-	0.3	μs
T_{BUF}	Bus Free Time between a STOP and START Condition	-	1.3	-	-	μs
C_b	Capacitive Load for each Bus Line	-	-	-	400	pF
$T_{SU;DAT}$	Data Set-up Time	-	100	-	-	ns
$T_{HD;DAT}$	Data Hold Time	-	0	-	-	ns
$T_{SU;STO}$	Set-up Time for STOP Condition	-	4.0	-	-	ns
T_{SW}	Spike Pulse Width	on bus	-	-	50	ns

(1) Unspecified for f_{CLKOUT} = 32.768KHz.

(2) All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

(3) I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

FUNCTIONAL DESCRIPTION

The PCF8563T/5,518-CN contains sixteen 8-bit registers with an auto-incrementing register address, an on-chip32.768KHz oscillator with one integrated capacitor, a frequency divider which provides the sourceclock for the Real-Time Clock (RTC) and calender, a programmable clock output, a timer, an alarm, avoltage-low detector, and a 400KHz I^2C-bus interface.

All 16registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm. Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the Timer_control and Timer registers, respectively.

The Seconds, Minutes, Hours, Days, Months, Years as well as the Minute_alarm, Hour_alarm, and Day_alarm registers are all coded in Binary Coded Decimal (BCD) format.

When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

1. REGISTER ORGANIZATION

Table 1. Formatted registers overview

ADDRESS	REGISTER NAME	BIT							
		7	6	5	4	3	2	1	0
CONTROL AND STATUS REGISTERS									
00h	Control_status_1	TEST1	0	STOP	0	TESTC	0	0	0
01h	Control_status_2	0	0	0	TI_IP	AF	TE	AIE	TIE
TIME AND DATE REGISTERS									
02h	VL_seconds	VL	SECONDS (00 ~ 59)						
03h	Minutes	×	MINUTES (00 ~ 59)						
04h	Hours	×	×	HOURS (00 ~ 23)					
05h	Days	×	×	DAYS (01 ~ 31)					
06h	Weekdays	×	×	×	×	×	WEEKDAYS (0 ~ 6)		
07h	Century_months	C	×	×	MONTHS (01 ~ 12)				
08h	Years	YEARS (00 ~ 99)							
ALARM REGISTERS									
09h	Minute_alarm	AE_M	MINUTE_ALARM (00 ~ 59)						
0Ah	Hour_alarm	AE_H	×	HOUR_ALARM (00 ~ 23)					
0Bh	Day_alarm	AE_D	×	DAY_ALARM (01 ~ 31)					
0Ch	Weekday_alarm	AE_W	×	×	×	×	WEEKDAY_ALARM (00 ~ 59)		
CLKOUT CONTROL REGISTER									
0Dh	CLKOUT_control	FE	×	×	×	×	×	FD1	FD0
TIMER REGISTERS									
0Eh	Timer_control	TE	×	×	×	×	×	TD1	TD0
0Fh	Timer	TIMER							

(1) Bit positions labelled as × are not relevant. Bit positions labelled with 0 should always be written with logic 0; if read they could be either logic 0 or logic 1.

1.1. CONTROL REGISTERS 1

Table 2. Control_status_1 - control and status register 1 (address 00h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	TEST1	TEST1=0	Normal mode
		TEST1=1	EXT_CLK test mode
5	STOP	STOP=0	RTC source clock runs
		STOP=1	all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768KHz is still available)
3	TESTC	TESTC=0	Power-On Reset (POR) override facility is disabled (set to logic 0 for normal operation)
		TESTC=1	Power-On Reset (POR) override may be enabled
6, 4, 2, 1, 0	0	0	Unused (set to logic 0)

1.2. CONTROL REGISTERS 2

Table 3. Control_status_2 - control and status register 2 (address 01h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7, 6, 5	0	0	Unused (set to logic 0)
4	TI_TP	TI_TP=0	$\overline{INT}$ is active when TF is active (subject to the status of TIE)
		TI_TP=1	$\overline{INT}$ pulses active according to Table 4 (subject to the status of TIE)
3	AF	0/1	When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten using the interface. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. AF and TF are according to Table 5.
2	TF	0/1	
1	AIE	AIE=0	alarm interrupt disabled
		AIE=1	alarm interrupt enabled
0	TIE	TIE=0	timer interrupt disabled
		TIE=1	timer interrupt enabled

(1) If AF and AIE are enabled, $\overline{INT}$ is always enabled.

Table 4. $\overline{INT}$ operation (bit TI_TP = 1)

SOURCE CLOCK (Hz)	$\overline{INT}$ PERIOD	
	n=1	N>1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

(1) TF and $\overline{INT}$ become active simultaneously.

(2) n = loaded countdown value. Timer stops when n = 0.

1.3. TIMER AND DATE REGISTERS

Table 5. VL_seconds - seconds and clock integrity status register (address 02h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	VL	0	Clock integrity is guaranteed
		1	Integrity of the clock information is not guaranteed
6-0	秒	00 ~ 59	Actual seconds coded in BCD format

VOLTAGE-LOW DETECTOR AND CLOCK MONITOR

The PCF8563T/5,518-CN has an on-chip voltage-low detector. When V_{DD} drops below V_{Low}, bit VL in the VL_seconds register is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by using the interface.

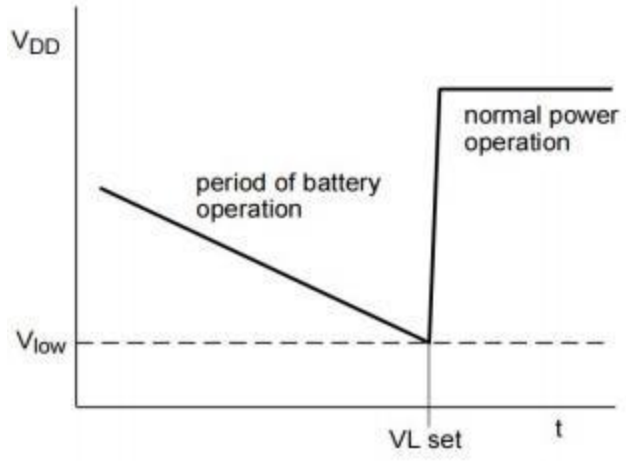


Fig 4. Voltage-low detection

Table 6. Minutes - minutes register (address 03h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	—	—	Unused
6-0	MINUTES	00 ~ 59	Actual minutes coded in BCD format

Table 7. Hours - hours register (address 04h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7-6	—	—	Unused
5-0	HOURS	00 ~ 23	Actual minutes coded in BCD format

Table 8. Days - days register (address 05h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7-6	—	—	Unused
5-0	DAYS	01 ~ 31	Actual minutes coded in BCD format

(1) The PCF8563T/5,518-CN compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

Table 9. Weekdays - weekdays register (address 06h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7-3	—	—	Unused
2-0	WEEKDAYS	0 ~ 6	Actual weekday values, see Table 10

Table 10. Weekday assignments

DAY	BIT		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 11. Century_months - century flag and months register (address 07h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	C	0	Indicates the century is X
		1	Indicates the century is X+1
6-5	—	—	Unused
4-0	MONTHS	01 ~ 12	Actual month coded in BCD format

Table 12. Month assignments in BCD format

BIT	SYMBOL	VALUE	DESCRIPTION
7-0	YEARS	0 ~ 9	Actual year coded in BCD format

(1) When the register Years overflows from 99 to 00, the century bit C in the register Century_months is toggled.

1.4. ALARM REGISTERS

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day or weekday, and its corresponding AE_X is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the alarm flag (AF in register Control_2) is set to logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{\text{INT}}$ pin follows the condition of bit AF. AF will remain set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_X bit at logic 1 are ignored.

Table 13. Minute_alarm - minute alarm register (address 09h) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	AE_M	0	Minute alarm is enabled
		1	Minute alarm is disabled
6-0	MINUTE_ALARM	00 ~ 59	Minute alarm information coded in BCD format

Table 14. Hour_alarm - hour alarm register (address 0Ah) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	AE_H	0	Hour alarm is enabled
		1	Hour alarm is disabled
6	—	—	Unused
5-0	HOUR_ALARM	00 ~ 23	Hour alarm information coded in BCD format

Table 15. Day_alarm - day alarm register (address 0Bh) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	AE_D	0	Day alarm is enabled
		1	Day alarm is disabled
6	—	—	Unused
5-4	DAY_ALARM	00 ~ 31	Day alarm information coded in BCD format

Table 16. Weekday_alarm - weekday alarm register (address 0Ch) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	AE_W	0	Weekday alarm is enabled
		1	Weekday alarm is disabled
6-3	—	—	Unused
2-0	WEEKDAY_ALARM	0 ~ 6	Weekday alarm information, see Table 10

1.5. RESGISTER CLKOUT_CONTROL AND CLOCK OUTPUT

Frequencies of 32.768KHz (default), 1.024KHz, 32Hz, and 1Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Table 17. CLKOUT_control - CLKOUT control register (address 0Dh) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7	FE	0	The CLKOUT output is inhibited and CLKOUT output is set high-impedance
		1	The CLKOUT output is activated
6-2	—	—	Unused
1-0	FD[1:0]	Frequency output at pin CLKOUT	
		00	32.768KHz
		01	1024Hz
		10	32Hz
		11	1Hz

1.6. TIMER REGISTERS

The 8-bit countdown timer at address 0Fh is controlled by the Timer_control register at address 0Eh. The Timer_control register determines one of 4 source clock frequencies for the timer (4096Hz, 64Hz, 1Hz, or 1⁄60Hz), and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF(see Table 3). The TF may only be cleared by using the interface. The asserted TF can be used to generate an interrupt on pin $\overline{INT}$. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the state of TF. Bit TI_TP(see Table 3) is used to control this mode selection. When reading the timer, the current countdown value is returned.

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

Table 18. Timer_control - timer control register (address 0Eh) bit description

BIT	SYMBOL	VALUE	DESCRIPTION	
7	TE	0	Timer is disabled	
		1	Timer is enabled	
6-2	—	—	Unused	
1-0	TD[1:0]		Timer source clock frequency select	
		00	4069Hz	
		01	64Hz	
		10	1Hz	
		11	1/60Hz	

(1) These bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to 1⁄60Hz for power saving.

Table 19. Timer - timer value register (address 0Fh) bit description

BIT	SYMBOL	VALUE	DESCRIPTION
7-0	TIMER[7:0]	00h-FFh	countdown period in seconds: *CountdownPeriod =n /SourceClockFrequency* where n is the countdown value

Table 20. Timer register bits value range

BIT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
128	64	32	16	8	4	2	1

2. EXT_CLK TEST MODE

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in register Control_status_1. Then pin CLKOUT becomes an input. The test mode replaces the internal 64Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300ns and a maximum period of 1000ns. The internal 64Hz clock, now sourced from CLKOUT, is divided down to 1Hz by a 26 divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0 (STOP must be cleared before the prescaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a one-second increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

OPERATION EXAMPLE

(1) Set EXT_CLK test mode (Control_status_1, bit TEST1 = 1).
(2) Set STOP (Control_status_1, bit STOP = 1).
(3) Clear STOP (Control_status_1, bit STOP = 0).
(4) Set time registers to desired value.
(5) Apply 32 clock pulses to CLKOUT.

(6) Read time registers to see the first change.
(7) Apply 64 clock pulses to CLKOUT.
(8) Read time registers to see the second change. Repeat steps 7 and 8 for additional increments.

3. RESET

The PCF8563T/5,518-CN includes an internal reset circuit which is active whenever the oscillator is stopped. Inthe reset state the I^2C-bus logic is initialized including the address pointer and all registers are set according to Table 27. I^2C-bus communication is not possible during reset.

Table 21. Register reset value

ADDRESS	REGISTER NAME	BIT							
		7	6	5	4	3	2	1	0
00h	Control_status_1	0	×	0	×	1	×	×	×
01h	Control_status_2	×	×	×	0	0	0	0	0
02h	VL_seconds	1	×	×	×	×	×	×	×
03h	Minutes	×	×	×	×	×	×	×	×
04h	Hours	×	×	×	×	×	×	×	×
05h	Days	×	×	×	×	×	×	×	×
06h	Weekdays	×	×	×	×	×	×	×	×
07h	Century_months	×	×	×	×	×	×	×	×
08h	Years	×	×	×	×	×	×	×	×
09h	Minute_alarm	1	×	×	×	×	×	×	×
0Ah	Hour_alarm	1	×	×	×	×	×	×	×
0Bh	Day_alarm	1	×	×	×	×	×	×	×
0Ch	Weekday_alarm	1	×	×	×	×	×	×	×
0Dh	CLKOUT_control	1	×	×	×	×	×	0	0
0Eh	Timer_control	0	×	×	×	×	×	1	1
0Fh	Timer	×	×	×	×	×	×	×	×

(1) Registers marked x are undefined at power-up and unchanged by subsequent resets.

3.1. POWER-ON RESET (POR) OVERRIDE

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I^2C-bus pins, SDA and SCL, are toggled in a specific order . All timings are required minimums.

Once the override mode has been entered, the device immediately stops, being reset, and normal operation may commence i.e. entry into the EXT_CLK test mode via I^2C-bus access. The override mode may be cleared by writing logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the override mode is possible. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.

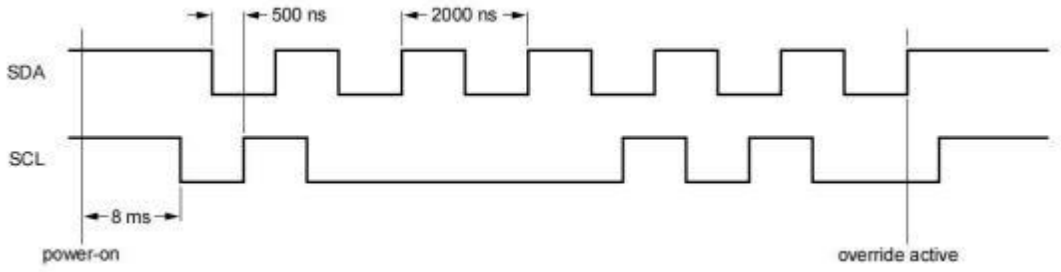


Fig 5. POR override sequence

4. THE I²C-BUS

4.1. CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

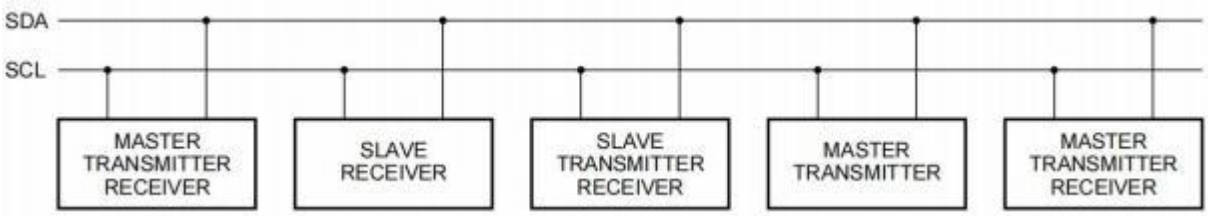


Fig 6. System configuration

4.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 7).

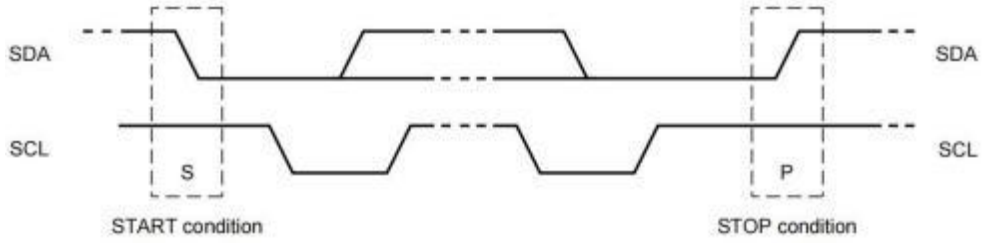


Fig 7. Definition of START and STOP conditions

4.3. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal

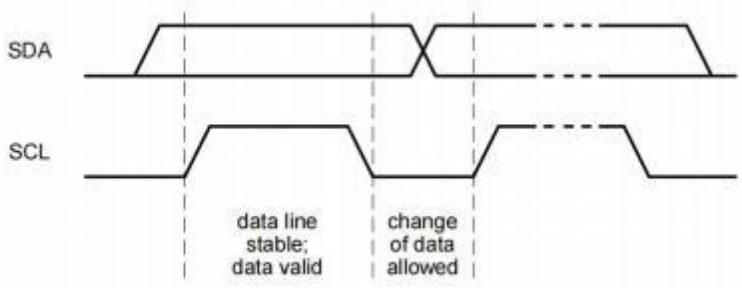


Fig 8. Bit transfer

4.4. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that

has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

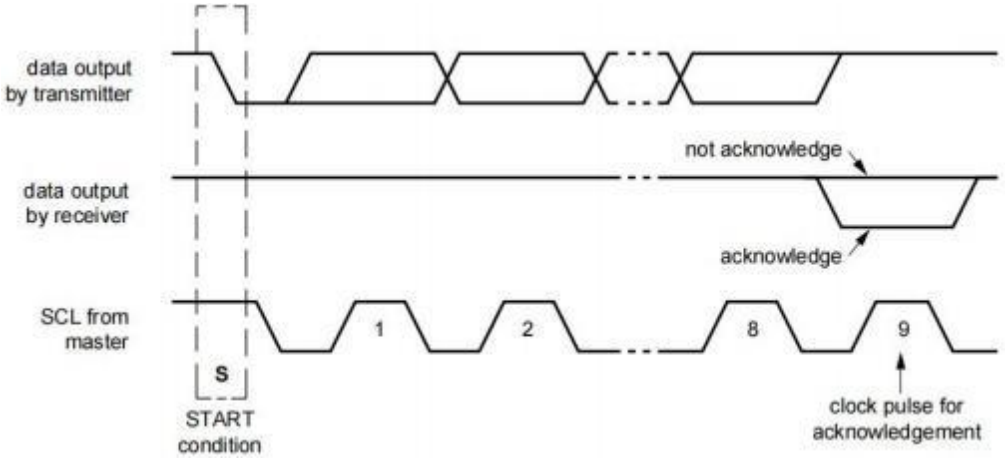


Fig 9. Acknowledgement on the I²C-bus

4.5. I²C-BUS PROTOLCO

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563T/5,518-CN acts as a slave receiver or slave transmitter.

Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

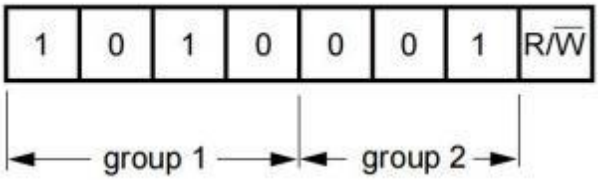


Fig 10. Slave address

The I²C-bus configuration for the different PCF8563T/5,518-CN READ and WRITE cycles is shown in Figure 11,Figure 12 and Figure 13. The register address is a 4-bit value that defines which register is to beaccessed next. The upper four bits of the register address are not used.

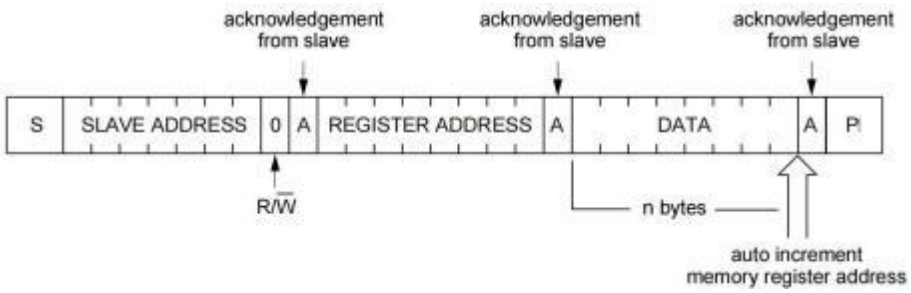


Fig 11. Master transmits to slave receiver (WRITE mode)

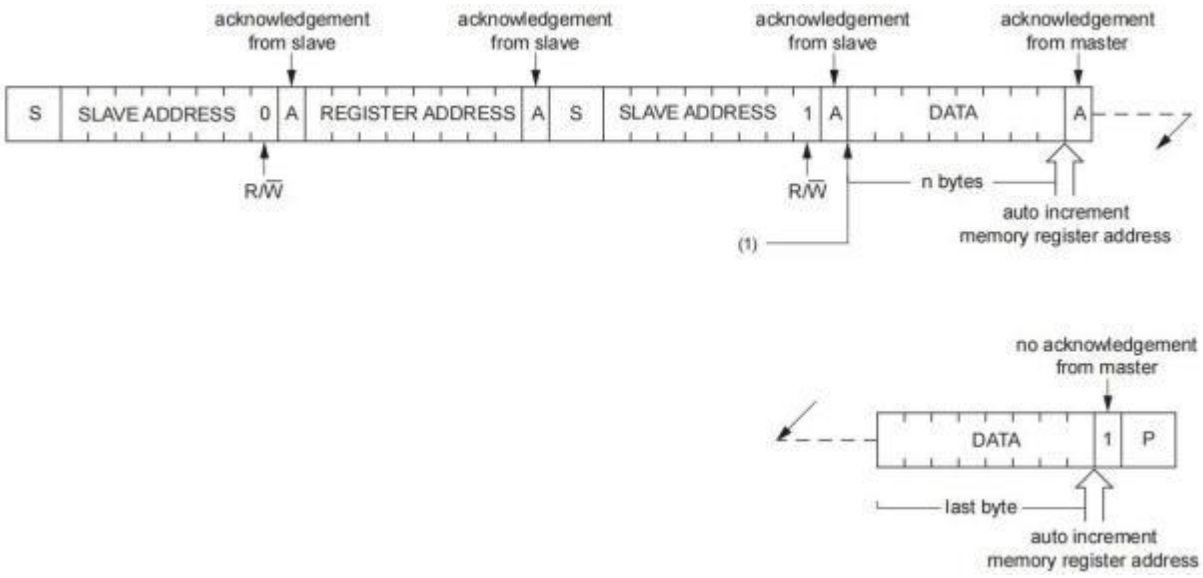


Fig 12. Master reads after setting register address (write register address; READ data)

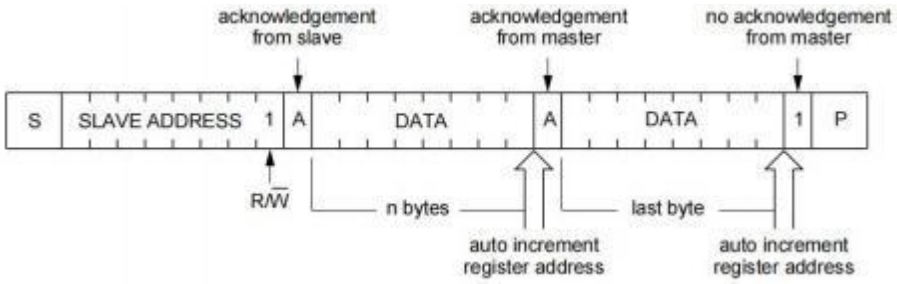


Fig 13. Master reads slave immediately after first byte (READ mode)

5. APPLICATION INFORMATION

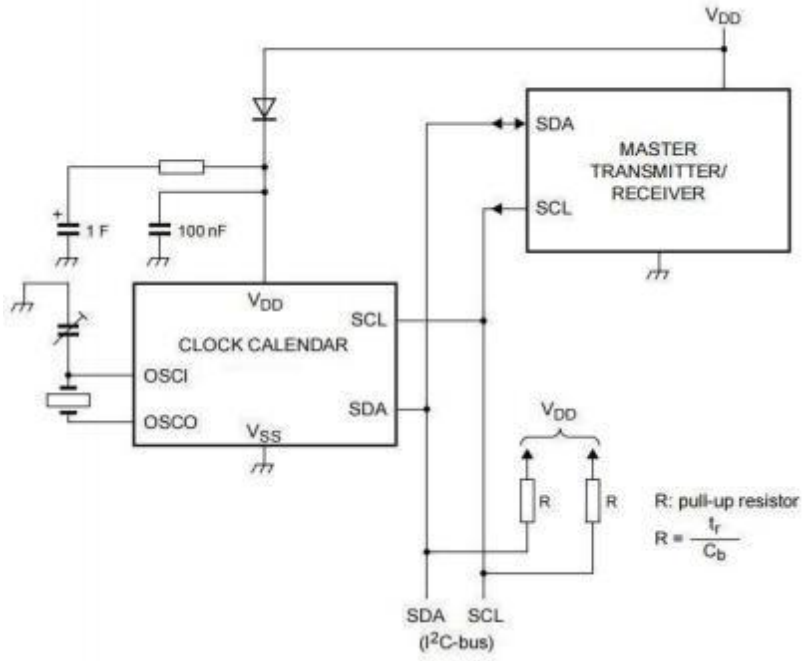
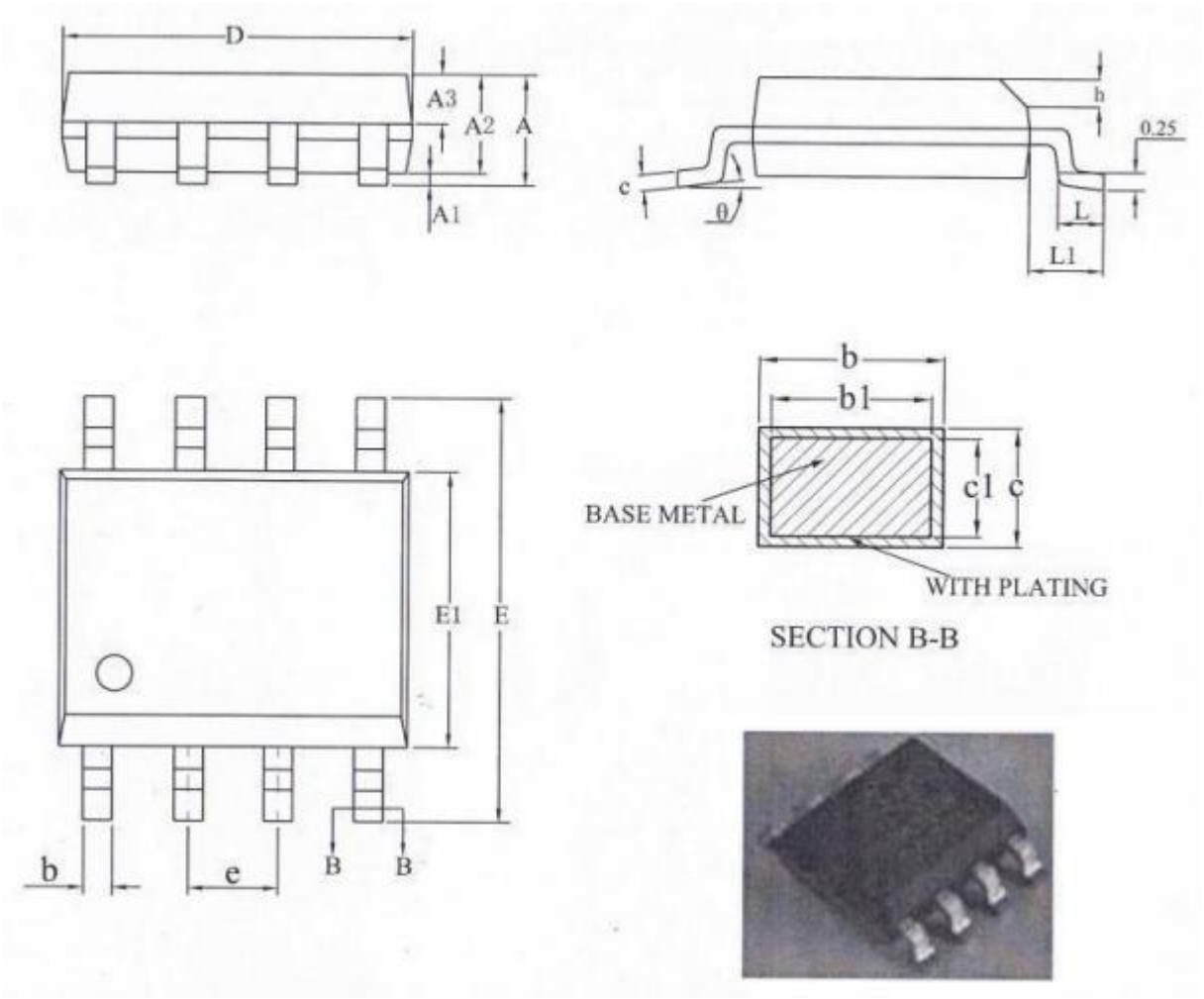


Fig 14. Application diagram

PACKAGE OUTLINE DIMENSIONS

SOP8



SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	-	-	1.75	D	4.80	4.90	5.00
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.80	3.90	4.00
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.47	h	0.25	-	0.50
b1	0.38	0.41	0.44	L	0.50	-	0.80
c	0.20	-	0.24	L1	1.05REF		
c1	0.19	0.20	0.21	θ	0°	-	8°

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