

TK62N60W-VB Datasheet

N-Channel 600V (D-S) Super Junction Power MOSFET

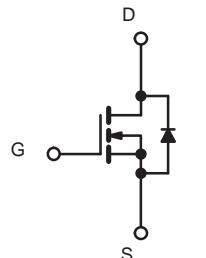
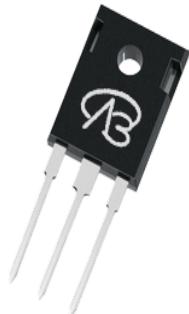
PRODUCT SUMMARY		
V_{DS} (V) at T_J max.		600
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.034

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



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N-Channel MOSFET

Top View

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	600	V	
Gate-Source Voltage		V_{GS}	± 30		
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	67	A	
		$T_C = 100$ °C	54		
Pulsed Drain Current ^a		I_{DM}	201		
Linear Derating Factor			1.67	W/°C	
Single Pulse Avalanche Energy ^b		E_{AS}	845	mJ	
Maximum Power Dissipation		P_D	500	W	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	$T_J = 125$ °C	dV/dt	50	V/ns	
Reverse Diode dV/dt ^d			15		
Soldering Recommendations (Peak Temperature) ^c			260	°C	
for 10 s					

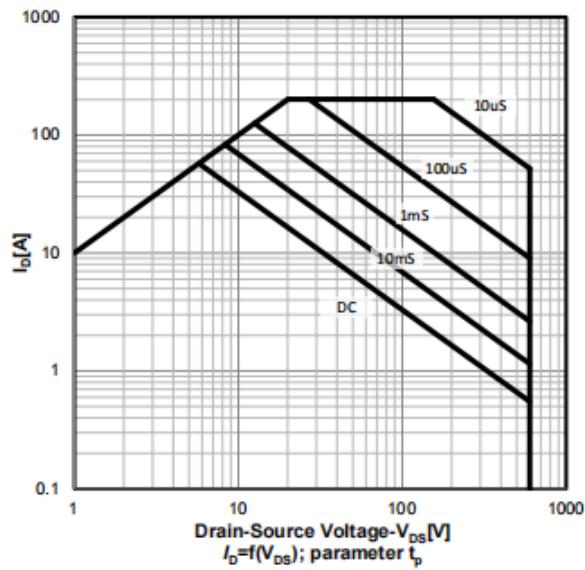
Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 100$ V, starting $T_J = 25$ °C, $L = 30\text{mH}$, $R_g = 25$ Ω, $I_{AS} = 24$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/μs, starting $T_J = 25$ °C.

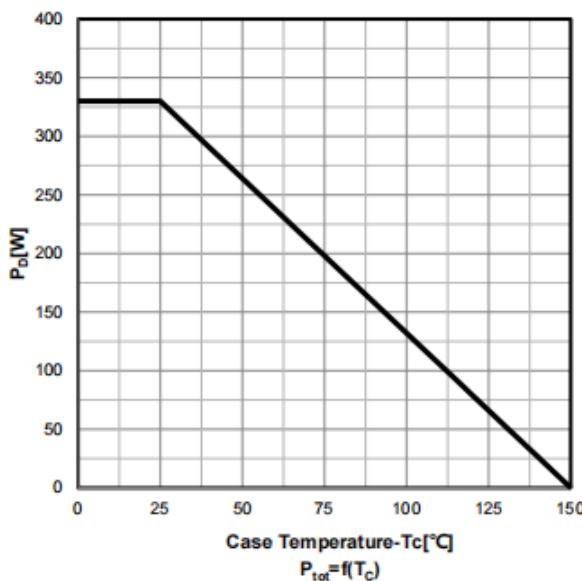
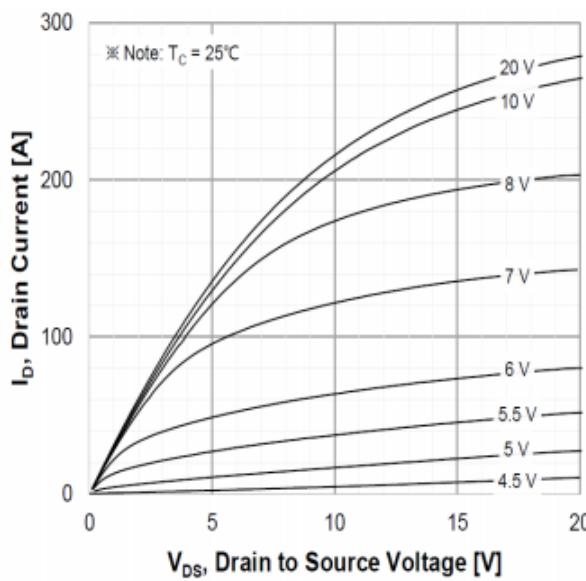
THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYP.	MAX.	UNIT			
Maximum Junction-to-Ambient	R_{thJA}	-	62	$^{\circ}\text{C}/\text{W}$			
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0 . 3 8				
SPECIFICATIONS ($T_J = 25^{\circ}\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 1 \text{ mA}$		600	-	-	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	0.70	-	
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.5	-	4.5	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	
		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 480 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	1	
		$V_{DS} = 480 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 16 \text{ A}$	-	0.034	-	
Forward Transconductance	g_{fs}	$V_{DS} = 30 \text{ V}$, $I_D = 16 \text{ A}$		-	5.6	-	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$		-	4600	-	
Output Capacitance	C_{oss}			-	330	-	
Reverse Transfer Capacitance	C_{rss}			-	4	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to 480 V , $V_{GS} = 0 \text{ V}$		-	63	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	213	-	
Total Gate Charge	Q_g			-	370	-	
Gate-Source Charge	Q_{gs}	$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$, $V_{DS} = 520 \text{ V}$	-	3.8	-	
Gate-Drain Charge	Q_{gd}			-	4.7	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480 \text{ V}$, $I_D = 20 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_g = 9.1 \Omega$		-	18	24	
Rise Time	t_r			-	24	55	
Turn-Off Delay Time	$t_{d(off)}$			-	8.0	-	
Fall Time	t_f			-	1.2	-	
Gate Input Resistance	R_g	$f = 1 \text{ MHz}$, open drain		-	0.8	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	67	
Pulsed Diode Forward Current	I_{SM}			-	-	201	
Diode Forward Voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = 8 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	-	1.5	
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = I_S = 8 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$, $V_R = 400 \text{ V}$		-	230	-	
Reverse Recovery Charge	Q_{rr}			-	5.8	-	
Reverse Recovery Current	I_{RRM}			-	4.5	-	

Notes

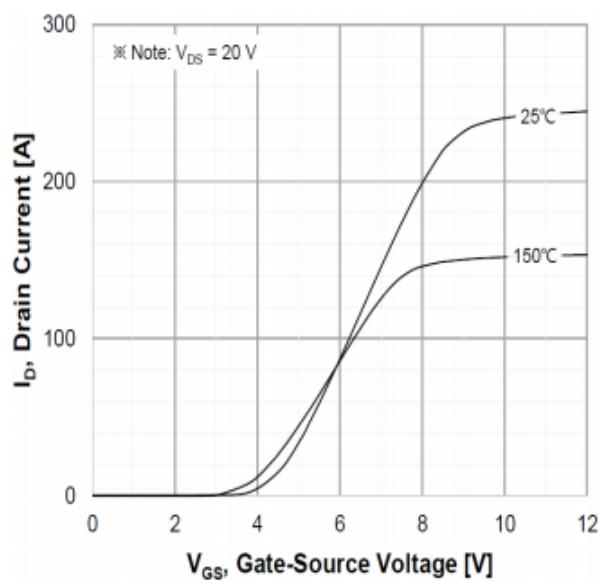
a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

Safe operating area $T_C=25\text{ }^\circ\text{C}$
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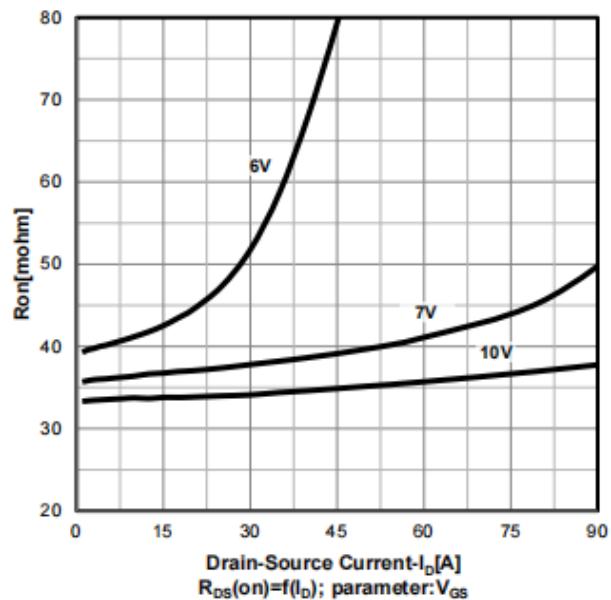
Power dissipation

Typ. output characteristics $T_J=25\text{ }^\circ\text{C}$ 

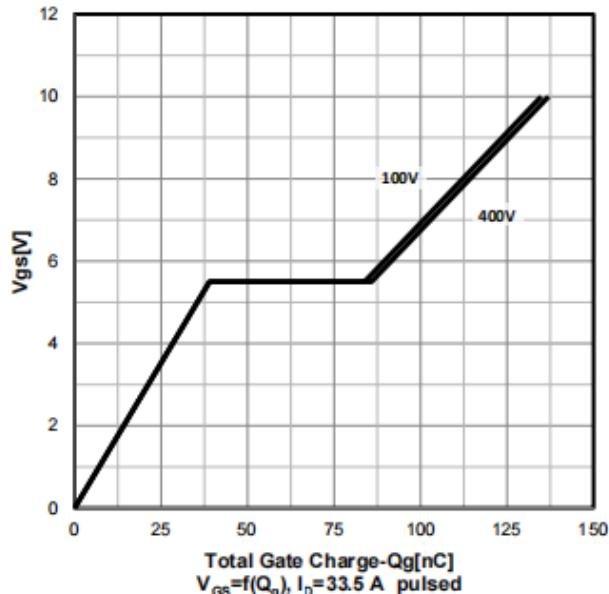
Transfer characteristics



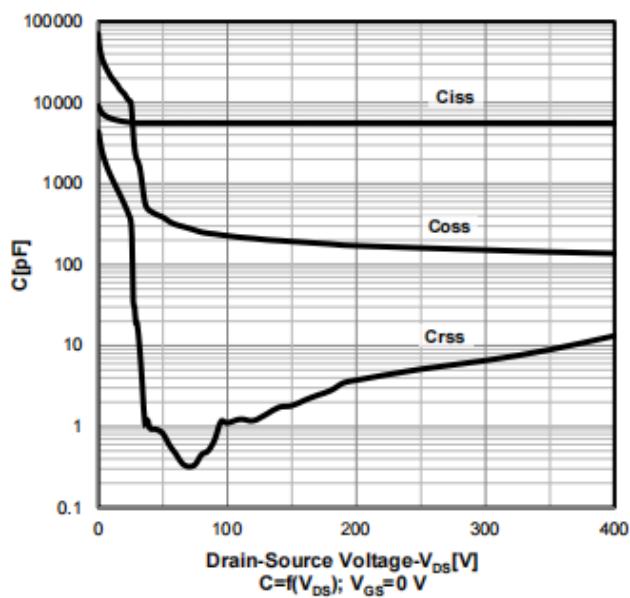
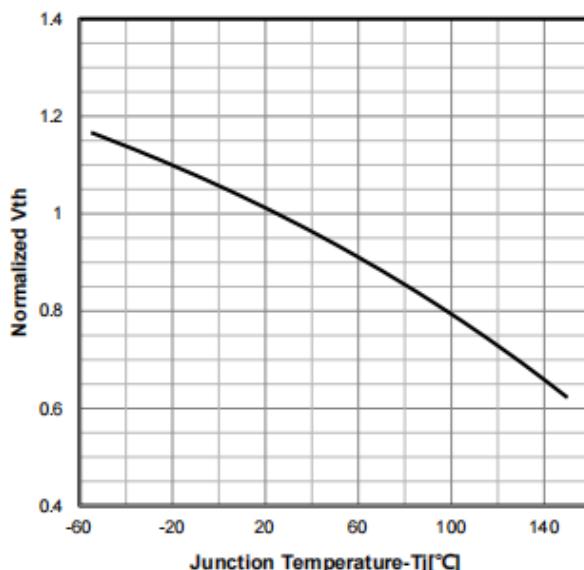
Typ. drain-source on-state resistance



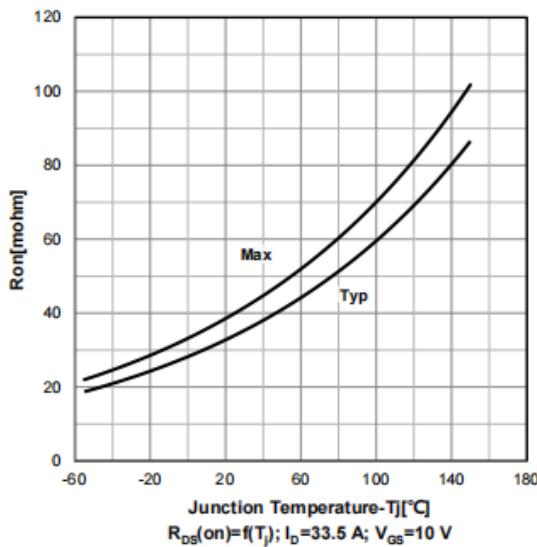
Typ. gate charge characteristics



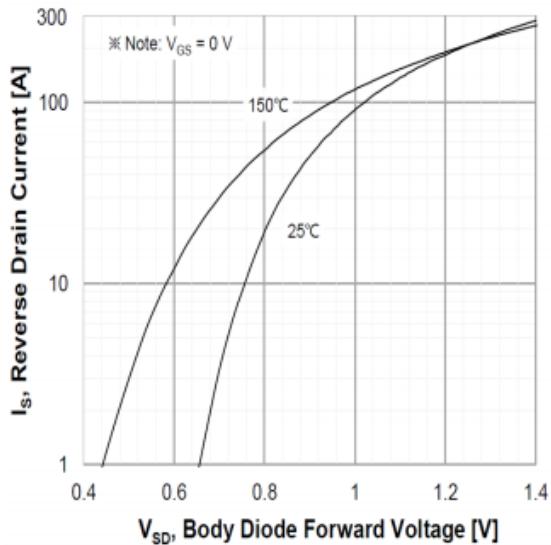
Typ. capacitances

Normalized $V_{GS(th)}$ characteristics

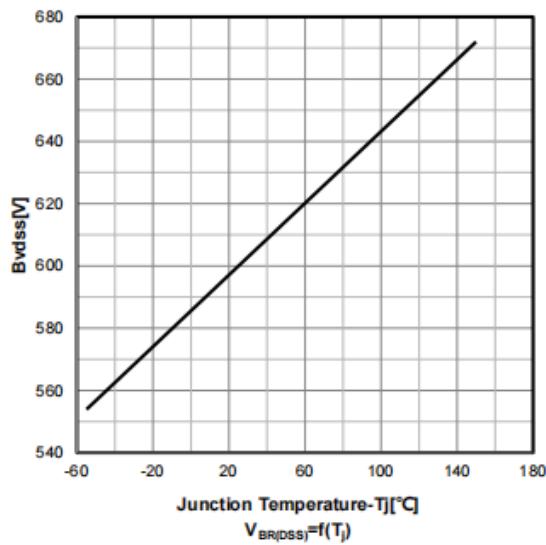
On-resistance vs temperature



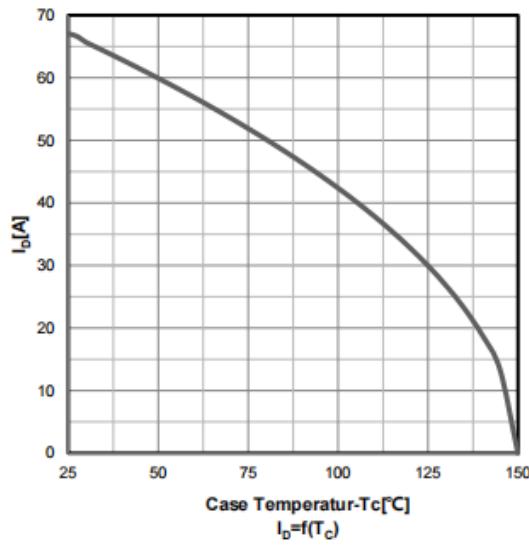
Forward characteristics of reverse diode



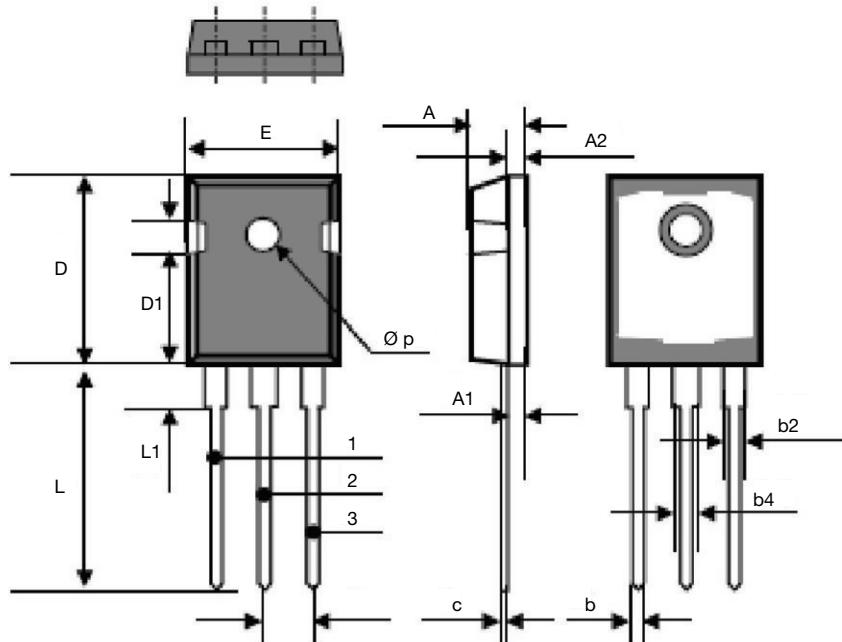
Drain-source breakdown voltage



Drain current vs temperature



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DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.31	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.41	0.065	0.095
b4	2.59	3.43	0.102	0.135
c	0.61 BSC		0.024 BSC	
D	20.80	21.46	0.819	0.845
D1	3.68	5.49	0.145	0.216
(e)	5.46 BSC		0.215 BSC	
E	15.49	16.26	0.610	0.640
L	19.81	20.32	0.780	0.800
L1	4.06	4.50	0.160	0.177
Ø p	3.51	3.66	0.138	0.144

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