

## IRFR234BTM-VB Datasheet

### N-Channel 250 V (D-S) 175 °C MOSFET

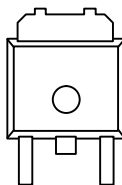
PRODUCT SUMMARY		
V <sub>DS</sub> (V)	250	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.176
Q <sub>g</sub> max. (nC)	68	
Q <sub>gs</sub> (nC)	11	
Q <sub>gd</sub> (nC)	35	
Configuration	Single	

#### FEATURES

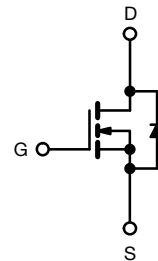
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements



TO-252



G D S  
Top View



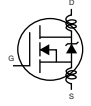

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	250	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current	V <sub>GS</sub> at 10 V	I <sub>D</sub>	T <sub>C</sub> = 25 °C	17	A
			T <sub>C</sub> = 100 °C	11	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	56		
Linear Derating Factor			1.0	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>		E <sub>AS</sub>	550	mJ	
Repetitive Avalanche Current <sup>a</sup>		I <sub>AR</sub>	17	A	
Repetitive Avalanche Energy <sup>a</sup>		E <sub>AR</sub>	13	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	125	W	
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	4.8	V/ns	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s		300		
Mounting Torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 4.5 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 14 A (see fig. 12).
- I<sub>SD</sub> ≤ 14 A, dI/dt ≤ 150 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.

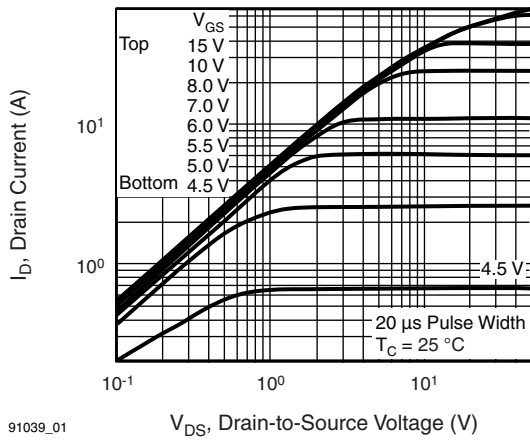
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		250	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.34	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 8.4\text{ A}^b$	-	0.176	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 8.4\text{ A}^b$		6.7	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5		-	1300	-	pF
Output Capacitance	$C_{oss}$			-	330	-	
Reverse Transfer Capacitance	$C_{rss}$			-	85	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 7.9\text{ A}, V_{DS} = 200\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	68	nC
Gate-Source Charge	$Q_{gs}$			-	-	11	
Gate-Drain Charge	$Q_{gd}$			-	-	35	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, I_D = 7.9\text{ A},$ $R_g = 9.1\text{ }\Omega, R_D = 8.7\text{ }\Omega,$ see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	$t_r$			-	24	-	
Turn-Off Delay Time	$t_{d(off)}$			-	53	-	
Fall Time	$t_f$			-	49	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz},$ open drain		0.3	-	1.2	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	14	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	56	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 7.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	250	500	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	2.3	4.6	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

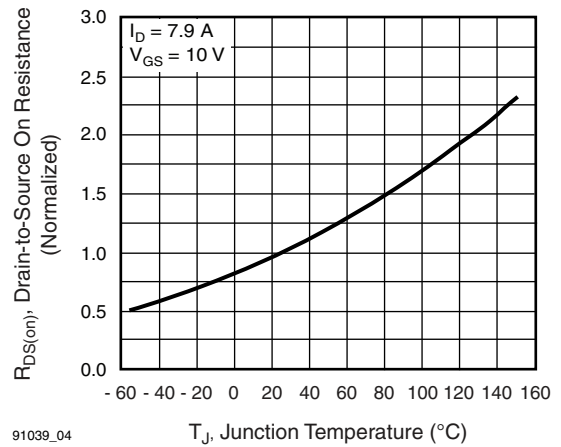
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

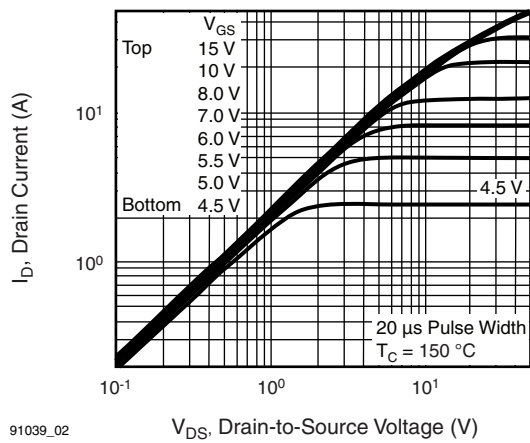
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



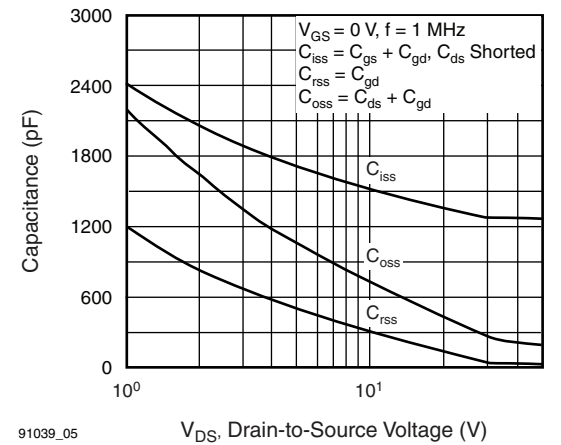
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



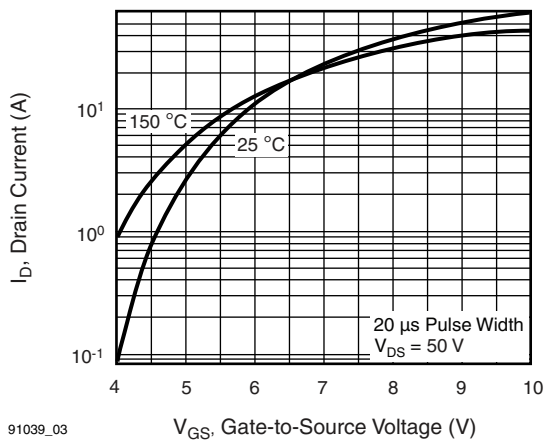
**Fig. 4 - Normalized On-Resistance vs. Temperature**



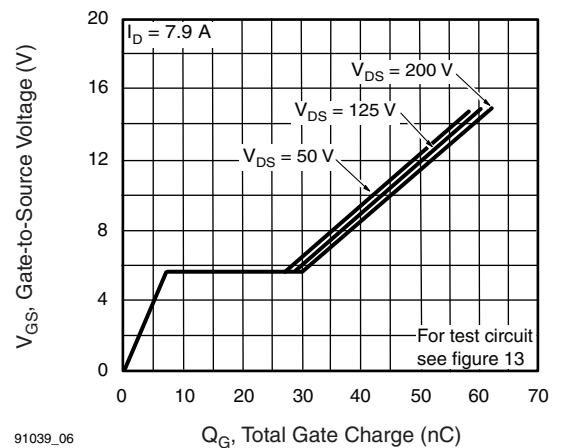
**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



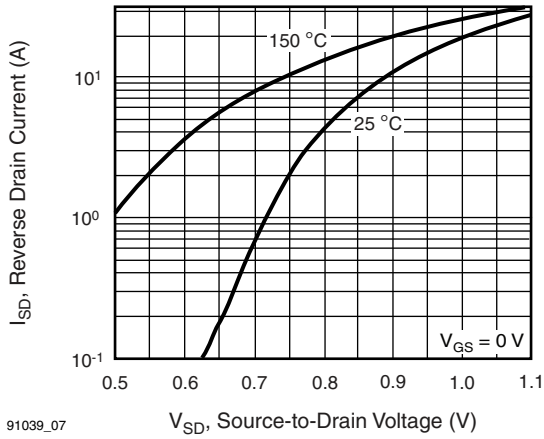
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**

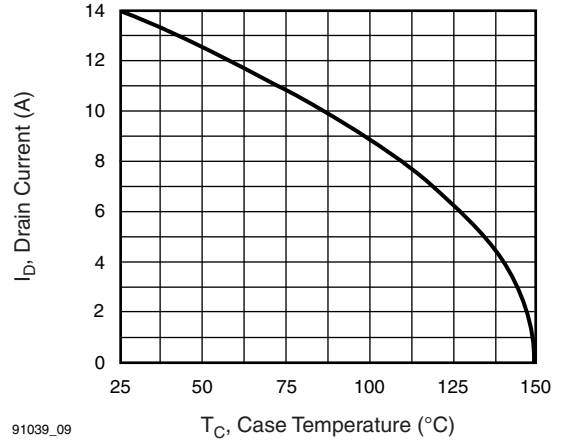


**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



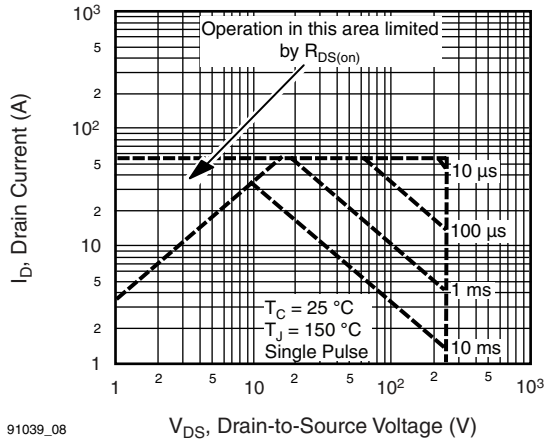
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**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



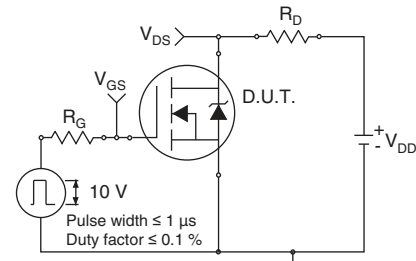
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**Fig. 9 - Maximum Drain Current vs. Case Temperature**

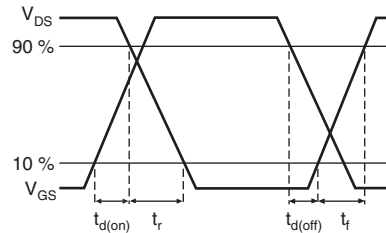


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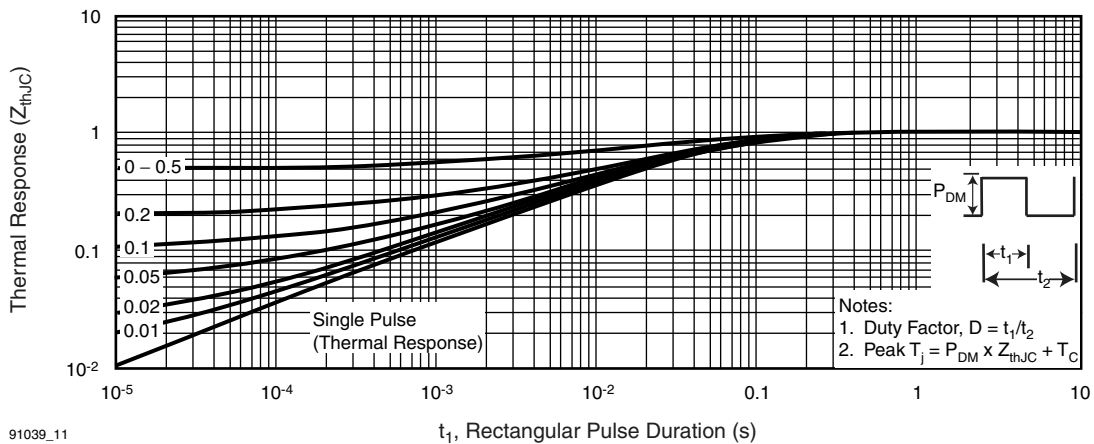
**Fig. 8 - Maximum Safe Operating Area**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



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**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

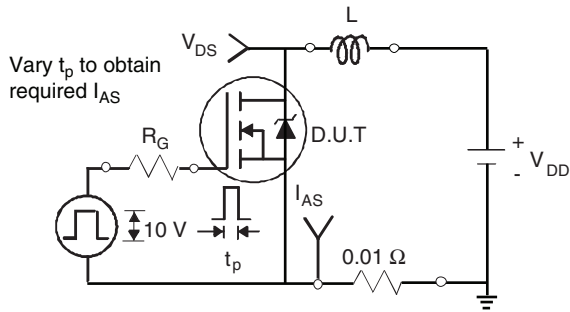


Fig. 12a - Unclamped Inductive Test Circuit

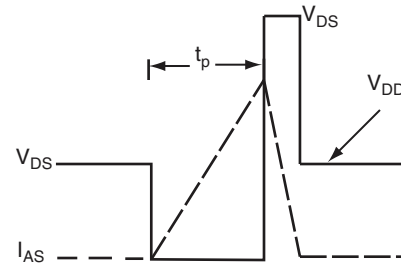
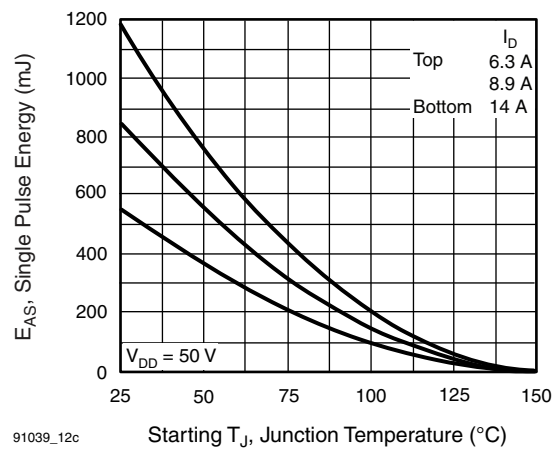


Fig. 12b - Unclamped Inductive Waveforms



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Fig. 12c - Maximum Avalanche Energy vs. Drain Current

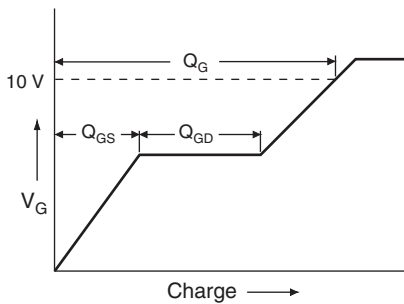


Fig. 13a - Basic Gate Charge Waveform

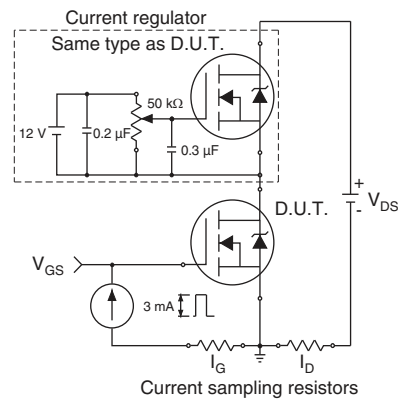
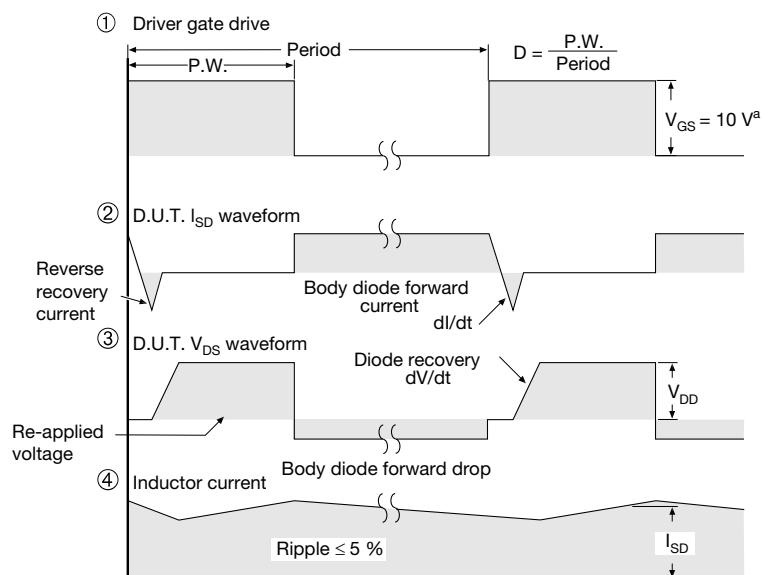
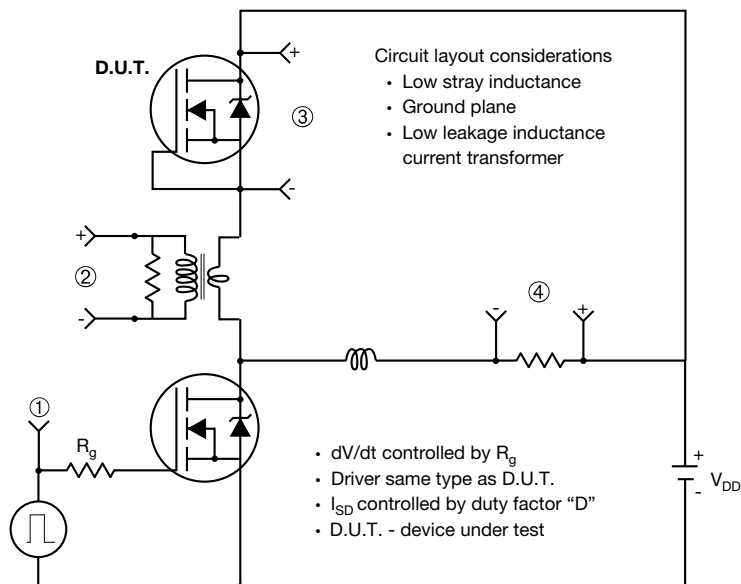


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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